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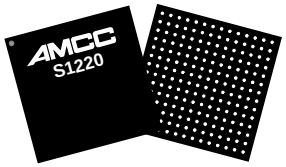


S1220

SONET/SDH/ATM Quad OC-3/12 with Clock Data Recovery (CDR)

Features

- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer, and jitter generation
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports Data Rates of 155.52 Mbps (OC-3) and 622.08 Mbps (OC-12)
- LVDS or LVPECL differential serial interface
- Internal termination of the optic's LVPECL driver renders a seamless power saving connection
- Typical 320 mW power in LVDS I/O mode
- Directly compatible with 2.5 V or 3.3 V LVDS, 3.3 V LVPECL (DC and AC)
- 196 PBGA Package,15x15 mm^2 with Green/RoHS compliant lead free option
- CMOS 0.13 micron technology
- 1.2 V and 3.3 V/2.5 V Power supply
- Receiver lock detect output for each channel
- Continued on next page...
- Signal detect input on each channel
- Selectable reference frequencies of 19.44, 77.76 or 155.52 MHz
- Quad configuration, mixed Mode OC-3/OC-12
- Independent power down of unused channels
- Drop-in-replacement for S1212

Applications

- SONET/SDH OC-3/OC-12
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

Description

The S1220 device consists of four CDR modules. Each of the modules can independently run at the OC-3 or OC-12 data rate. The S1220 can also be provisioned to mix and match OC-3 and OC-12 data streams within the same device.

The S1220 can be configured in Media Independent Interface (MII) mode or in Non-MII mode.

The S1220 minimizes the external components on the board: no external loop filter component, internally biased outputs, internally provided common mode bias for AC input, and internally provided bias for external LVPECL driver.

The S1220 offers significant advantages in power and real estate savings with high level of integration, and a small package.

The figure below, System Block Diagram, shows a typical network application.

Overview

The function of the S1220 clock and data recovery unit is to derive high speed timing signals for SONET/SDH-based equipment. The S1220 receives either an OC-12 or an OC-3 scrambled NRZ signal and recovers the clock from the data stream. The device outputs a differential bit clock and retimed data.

The Low Voltage LVDS or LVPECL interfaces guarantee compliance with the bit-error rate requirements of the Telcordia and ITU-T standards.

The S1221 is divided into four transmitter channels and four receiver channels.

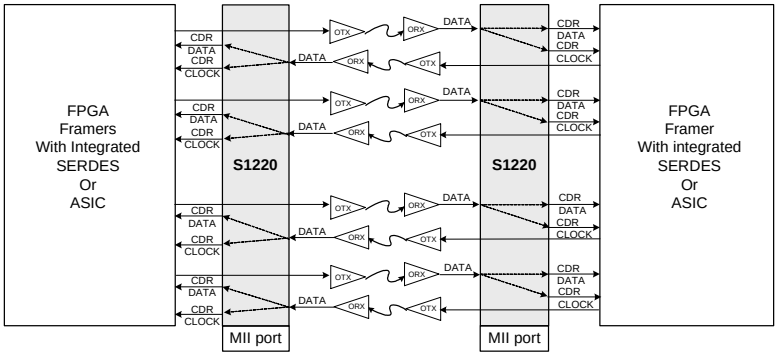
AMCC Suggested Interface Devices

AMCC S4805 (DANUBE)	SONET/SDH Mapper STS-48/STM-16, 4 x STS-12/STM, 4 x STS-3/STM-1
AMCC S4806 (OHIO)	OC-48/4 x OC-12 SONET/SDH Framer and channelized ATM/POS Mapper
AMCC S1208 (EVROS)	STS-12/STM-4 DS3/E3/DS1 E1/VT/TU SONET/SDH Mapper
Agilent HFBR-5908E	SFF Optical Transceiver
Sumitomo SCP6802-GL SCM6005	SFP & SFF Optical Transceiver
Finisar FTRJ1322P1xTR	SFP Optical Transceiver
OCP TRPN03 & TRPN12	SFP Optical Transceiver
JDS Uniphase CT2-P	SFP Optical Transceiver

The sequence of operations is as follows for each Channel:

- Serial data input
- Serial Data and recovered clock outputs

Internal clocking and control functions are transparent to the user.



System Block Diagram with the S1220

S1220

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