CONGO

PRODUCT BRIEF

STS-12c/STS-3c POS/ATM SONET MAPPER

Features

- Processes SONET/SDH STS-12c/(STM-4/AU-4-4c) or STS-3c/STM-1 data streams with full duplex mapping of ATM cells or packets (PPP or LAPS) into SONET/SDH payloads.
- Terminates & generates SONET/SDH section, line, & path layers, with transport/section E1, E2, F1 and DCC overhead interfaces in both transmit and receive directions.
- Provides an 8-bit parallel line-side interface operating at 19.44/77.76 MHz, and a 16-bit Utopia Level 2 or POS-PHY^{TM} Level 2 compatible system-side interface at 25/50 MHz.
- Generic 8-bit microprocessor interface for configuration, control, and status monitoring.
- Scrambling/descrambling ($1+X^6+X^7$) of SONET/SDH frame.
- Selectable self-synchronous scrambler implementing ($X^{43}+1$) polynomial for ATM and HDLC.
- Supports multiple devices sharing the same Utopia interface when used in a multi-PHY configuration.
- Provides an 8-bit General Purpose I/O (GPIO) register and associated hardware interface pins.
- Provides an IEEE 1149.1 JTAG (Boundary Scan) test port.
- Provides internal loopback paths for diagnostics.
- Implemented in 0.35um/3.3V CMOS process technology
- Packaged in 208 pin PQFP.

General Description

The S1201 is a highly-integrated VLSI device that provides full-duplex mapping of PPP/LAPS encapsulated packets or ATM cells into STS-12c/AU-4-4c or STS-3c/AU-4 payloads. The S1201 supports full-duplex processing of SONET/SDH data streams with full section, line, and path overhead processing. The device supports framing pattern, scrambling/descrambling, alarm signal insertion/detection, and bit interleaved parity (B1/B2/B3) processing. Serial interfaces for SONET/SDH TOH overhead bytes are also provided.

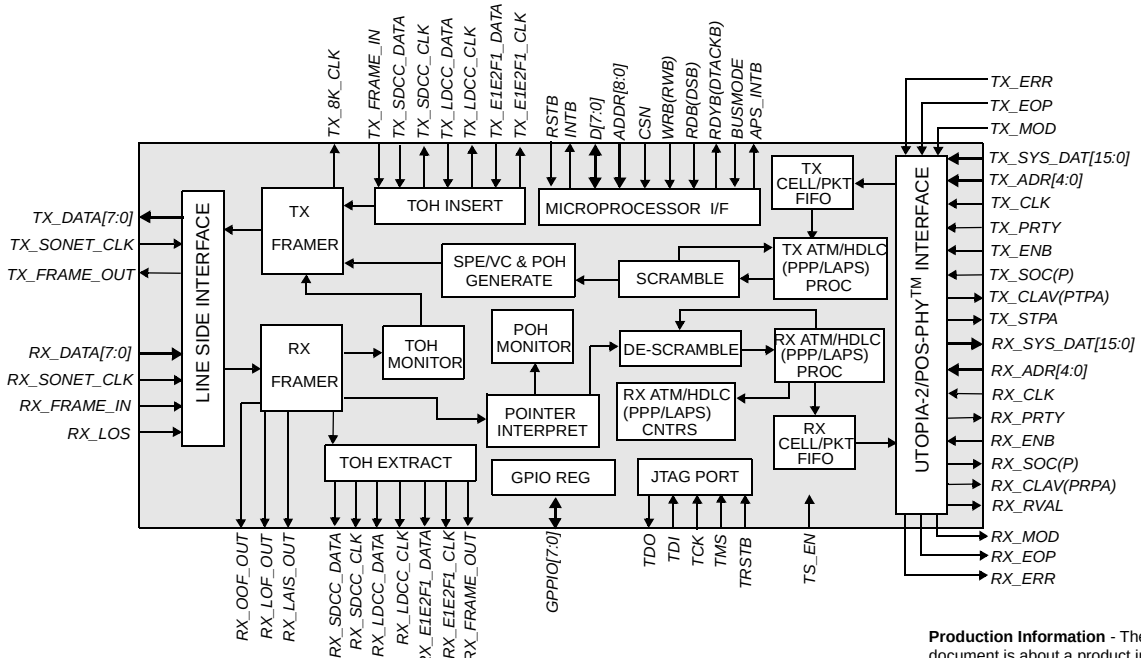
The S1201 provides a line-side interface that can operate at 622.08 Mb/s (8-bit bus at 77.76 MHz) or 155.52 Mb/s (8-bit bus at 19.44 MHz). For ATM applications, a UTOPIA Level 2 system interface, operating at either 25 or 50 MHz is provided. For Packet-over-SONET applications, a POS-PHY^{TM} Level 2 compatible interface is provided.

The S1201 is standards compliant with Bellcore GR-253, ITU G.707, ANSI T1.105 -1995, IETF RFCs 1619/1661/1662/2615 (PPP) and ITU-T COM 7-224-E/D307 (LAPS recommendation) protocols.

ATM support includes insertion and extraction of ATM cells into and out of the SONET/SDH SPE, scrambling/descrambling, header error control (HEC) detection and correction, idle cell generation and filtering, and generation of performance monitoring counts for TX, RX, ERR, dropped and idle cells.

HDLC support includes framing, transparency processing, optional 16/32 FCS processing, and self synchronous scrambling/descrambling ($X^{43}+1$). It also supports a direct flow-thru mode where the system data is passed directly to or from the SPE.

S1201 Block Diagram



Production Information - The information contained in this document is about a product in its fully tested and characterized phase. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

Overview and Applications

SONET Processing

The S1201 performs standard STS-3c/STM-1 or STS-12c/(STM-4/AU-4-4c) processing for both the transmit and receive directions. ATM cells or PPP/LAPS packets are mapped into the SONET/SDH SPE/VC, the POH, TOH/SOH are inserted, and the resulting STS frame is transmitted in byte wide format to the line-side interface. The reverse process occurs when receiving data from the line-side. A TOH interface provides direct add/drop capability for E1, E2, F1, & both Section and Line DCC channels. The S1201 also includes a clear channel mode that enables the direct transmission of system payload from the system interface to the line-side interface.

ATM Processing

When configured for ATM cell processing, the S1201's transmit ATM processor will perform all necessary cell encapsulation including HEC generation, cell level scrambling ($X^{43}+1$), and idle cell insertion to adapt the cell rate to the SPE. When receiving data from the line side, it performs cell delineation, Rx header control, descrambling, and receive cell rate adaptation. The S1201 also provides a full suite of status and control registers accessible via the microprocessor.

Packet/HDLC Processing

When configured for POS mode, the S1201's transmit HDLC processor provides the insertion of HDLC framed PPP/LAPS packets into the STS SPE. It will perform packet framing, inter-frame fill and Tx FIFO error recovery. In addition, it optionally performs payload scrambling ($X^{43}+1$), performs transparency processing as required by RFC 1662/ITU-T COM7-D307 and will optionally generate a 16/32 bit CRC.

The receive HDLC processor provides for the extraction of PPP/LAPS packets from HDLC frames, transparency removal, de-scrambling (if enabled), FCS error checking and optionally deletes the HDLC control and address fields. The S1201 also provides a robust set of counters and status/control registers for performance monitoring via the microprocessor.

Line-side Interface

On the line-side, the S1201 supports an 8-bit parallel interface which operates at 77.76/19.44 MHz when the device is configured for STS-12c/STS-3c. The device is typically connected to a parallel-to-serial converter, which is in turn connected to an electrical-to-optical converter for interfacing to the fiber optic interface. (See figure below.)

System Interface

The S1201 interface to the system link-layer device is via a Utopia Level-2 compliant interface when operating in ATM mode, and a POS-PHY^{TM} Level-2 compatible interface when operating in Packet-Over-SONET mode. The interface operates at 25/50 MHz, as either 8 or 16 bits, in either Utopia or POS-PHY^{TM} mode.

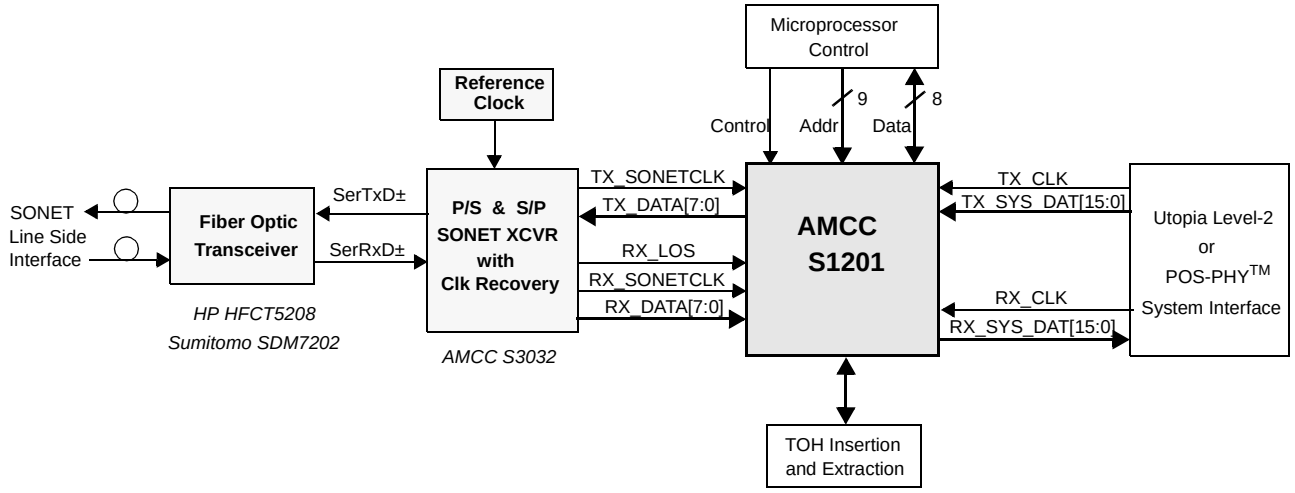
Microprocessor Interface

An 8-bit microprocessor interface is provided for device control and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt driven or polled-mode configurations.

Applications

ATM switches, Routers, IP switches, Virtual Networks.

Typical Application: S1201 in 622 Mb/s ATM or POS System



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