Model® Ware

Standards to Silicon™

Product Brief
SPI-4 Phase 1 Core w/ FIFOs V1.0 For Altera PLDs
June 2001

Features

- OIF-compliant SPI-4 Phase 1 (compatible with AMCC FlexBUS-4) with FIFOs
- ATM, Packet Over SONET (POS), and Direct Data Mapping[1] modes
- Single- and multi-link operation, scalable from 1 to 16 links.
- Programmable per-port bandwidth allocation
- Programmable FIFO size with programmable almost empty/almost full thresholds.
- Programmable burst size
- Automatic link selection in the Source block based on Source FIFO threshold and flow control information.
- 64-bit data bus width.
- Parity generation/checking over data and control words
- Altera's Atlantic Interface on user's side.
- Full synchronous design, exceeds: Clk = 200 MHz
- Fully automatic test bench including driver/monitor.
- Easy to use in Mux/Demux and bridge functions

Standards Compliance

- OIF SPI-4 Phase 1
- AMCC FlexBUS-4

Benefits

- Faster FPGA and ASIC development for improved time-to-market with FlexBUS-4 functions
- Lower development cost through design reuse
- Available source code licensing for easy design integration and migration to gate arrays or ASICs
- Ample design flexibility using control signals and generics/parameters
- Verified functionality and standards compliance

Description

The Optical Interworking Forum's (OIF) SPI-4 Phase 1 interface allows the interconnection of Physical Layer devices to Link Layer devices in 10Gb/s ATM, POS, and Ethernet applications. Modelware's SPI-4 Phase 1 core performs the interface functions on both sides of the interface as shown in Figure 1and Figure 2.

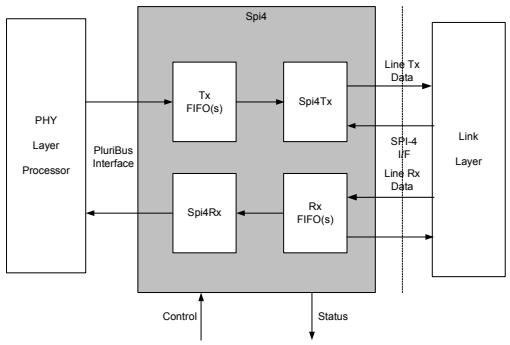

Figure 1: SPI-4 Phase 1 PHY Layer Application

[1] Direct Data Mapping is a raw data mode supported in AMCC's Ganges device.

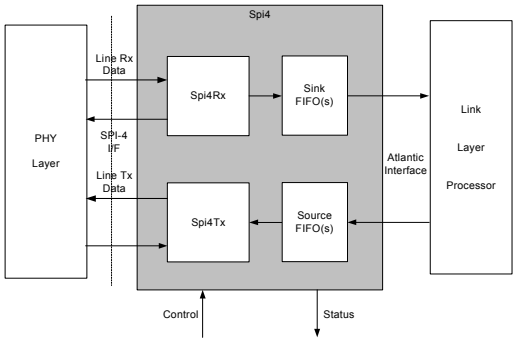

Figure 2: SPI-4 Phase 1 Link Layer Application

On the system side, the SPI-4 Phase 1 core interfaces to a single or to multiple links or ports via Altera's Atlantic interface.

The Spi4Tx block monitors the Source FIFOs fill level and the flow control information received from the opposite side of the SPI-4 interface. If a Source FIFO has data and the flow control information for the corresponding channel indicates that it is ready to accept data, the Spi4Tx block initiates a data transfer from the Source FIFO towards the SPI-4 interface.

The Spi4Rx block transmits the Sink FIFO status information to the opposite side according to the Sink FIFO almost-full flags. The Spi4Rx block stores data received for a particular link in that link's FIFO. Sink FIFO flags indicate to the user the presence of data in the FIFO(s).

Gate Count

The SPI-4 Phase 1 Core configured for 4 channels and targeted to APEX II uses:

Logic Elements (LEs): 2700
Embedded System Blocks (ESBs): 23

The above numbers include the core and a small amount of circuitry to implement a loopback on the Atlantic Interface.

Design Package

The SPI-4 Phase 1 Core source code package contains:

- Source code or Netlist
- Test bench (source code option)
- Scripts and data files for simulation (behavioral, gate-level, and back-annotated), synthesis, and FPGA layout
- Detailed documentation:
  - ⇒ Reference Guide: Core features, architecture, interfaces, and operation
  - ⇒ User's Guide: Core simulation, synthesis, and FPGA layout step-by step procedures.

Supported Tools

- MTI Modelsim for simulation
- Exemplar Leonardo Spectrum for synthesis
- Altera Quartus

Ordering Information

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