FREQUENCY DEVICES™, INC.

SPPDM-01

DSP Solutions with Analog Input/Output

Dual Channel, Differential Input FIR Filter Platform

Description

Design engineers now have an off-the-shelf precision, dual channel hardware solution for development of digital FIR filters that can be used in production subassemblies. Designers can generate FIR filter characteristics in a MatLab™ V5.3 or V6.0 environment and directly load standard or custom coefficient sets into the SPPDM-01 platform via an RS232 interface located on the users field programmable subassembly or from the SPPDB-01 development board.

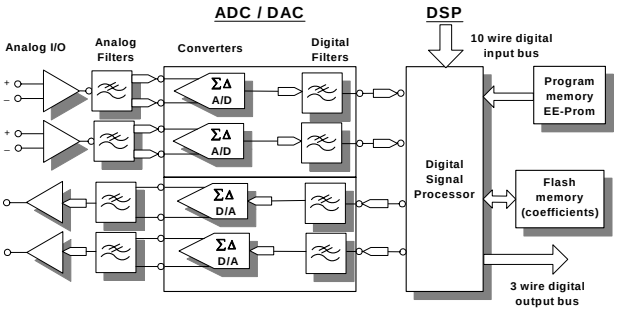
By utilizing the SPPDF-01 hardware with the enclosed MatLab GUI, generated coefficients are loaded directly into the removable SPPDM-01 platform for insertion into finished EOEM products. This unique capability minimizes product development and manufacturing cycle times while providing precise unit-to-unit product matching in a small 2" x 2" footprint that can be reconfigured or upgraded in the field.

SPPDM-01 FIR filter platforms operates over a 100 Hz to 20 kHz audio frequency range. Each channel can be configured to provide up to 9-bits of filter frequency programmability per channel. This dual channel DSP design solution contains anti-alias and reconstruction filters along with ADC's and DAC's offering low noise and distortion signal processing with THD approaching –100 dB. Sampling at 48 kHz the fixed point DSP utilizes 32-bit math to achieve 24-bits of precision.

Features/ Benefits:

- Compact 2" x 2" dual channel design combined with large program memory (256 k EE-Prom) and 4-Mbits of flash memory optimizes DSP processing power in minimal board space.
- SPPDB-01 development hardware offers rapid set-up, programming and performance evaluation, shortening the product development cycle while insuring high precision field programmable installation.
- Field programmability of coefficient sets, analog I/O and storage for 100's of application specific FIR filters provide designers with unmatched design, implementation and field upgrade flexibility.

SPPDM-01 Platform



SPPDM-01 Block diagram

Applications

- Brick-Wall; High-Pass, Low-Pass, Band-Pass, Band-Reject and Multi-Rate filters with Linear Phase and Signal Generators for Data Acquisition Systems.
- Speech analysis, research, pathology
- Sound and vibration testing

OTHER AVAILABLE PLATFORM PRODUCTS

SPP-01: Plug and play hardware/evaluation board, programmable with turnkey or customer generated algorithms.

SPPDB-01: Development Board, for the SPP-01 family of products. May also be used as a mounting assembly.

SPPDS-01: Development Suite for all SPP platform products. Requires TI's Code Composer Studio™.

SPPDF-01: Development Suite for SPPDM-01 FIR filter products. Requires MatLab™ V5.3 or V6.0.

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Typical Program Selection Port Protocol

Data Format

- Logic "0" 0VDC Min – 2VDC Max
- Logic "1" 3.5VDC Min – 5Vdc Max

Bit Weighting (Binary Coded)

D_0 LSB
D_7 or D_8 MSB

Program Selection:
8-Bit: 256 filters with different FIR algorithms on each channel
9-Bit: 512 filters with the same FIR algorithm on each channel.

8 - Bit Programming Table

MSB	---	---	---	---	---	---	LSB	Bit Weight
2^7 D_7	2^6 D_6	2^5 D_5	2^4 D_4	2^3 D_3	2^2 D_2	2^1 D_1	2^0 D_0	Program address
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	1	1	8
0	0	0	0	1	1	1	1	16
0	0	0	1	1	1	1	1	32
0	0	1	1	1	1	1	1	64
0	1	1	1	1	1	1	1	128
1	1	1	1	1	1	1	1	256

1. The program selection data word bus consists of D_0 to D_7 for 8 - bit programming.
2. The channel selection bit is D_8. For D_8, Channel 1 is "0" and Channel 2 is "1".

9 - Bit Programming Table

MSB	---	---	---	---	---	---	---	LSB	Bit Weight
2^8 D_8	2^7 D_7	2^6 D_6	2^5 D_5	2^4 D_4	2^3 D_3	2^2 D_2	2^1 D_1	2^0 D_0	Program address
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	1	4
0	0	0	0	0	0	1	1	1	8
0	0	0	0	0	1	1	1	1	16
0	0	0	0	1	1	1	1	1	32
0	0	0	1	1	1	1	1	1	64
0	0	1	1	1	1	1	1	1	128
0	1	1	1	1	1	1	1	1	256
1	1	1	1	1	1	1	1	1	512

1. The program selection data word bus consists of D_0 to D_8 for 9 - bit programming.
2. The channel selection bit is D_9. For D_9, Channel 1 is "0" and Channel 2 is "1".

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Performance Specifications	
Available bandwidth Bandwidth	DC to 20 kHz 100 Hz to 20 kHz
Frequency Accuracy	< ±0.05 %
Amplitude Accuracy at unity gain.	< ±0.1 dB
Total Broad Band Noise (Ref to input 7 VRMS)	< -96dB Max
Total Harm. Dist.(THD) (10V peak to peak)	<-96 dB Max. to 20 kHz
Maximum FIR tap number for filter design	300 taps
Channel to Channel phase tracking	< ±0.1°
Cross talk dual channel version with different signals on each channel	DC to 20K <-100 dB Typ.
Temperature Operating Storage	 0 to +70°C -25 to +85°C
Size	2.0” x 2.0” x 0.5”

Specifications

(@25°C and Vs = ±15 Vdc)

Analog Input Characteristics

Maximum Input Impedance	1.0 MΩ
Input voltage	±10 V peak

Analog Output Characteristics

Minimum load Impedance	10 kΩ
Maximum capacitive load	50 pF
Output voltage	±10 V peak
Offset Voltage	2 mV Typ., 10mV Max.

Power Supply (±Vs)

Analog Vs range	±12Vdc Min to ±15 Vdc Max.
Analog supply current at Max. Vs	70 mA Typ.
Digital PS Voltage	+5 Vdc
Digital supply current	370 mA Typ.
Power consumption at Max. Vs	4.0 watts Typ.

Care must be taken to stay above the minimum Vs in order to maintain the linearity and distortion performance of the DSP platform.

See SPPDF-01 User’s Manual, Appendix C for the Field Programmability Design Guidelines and Schematic

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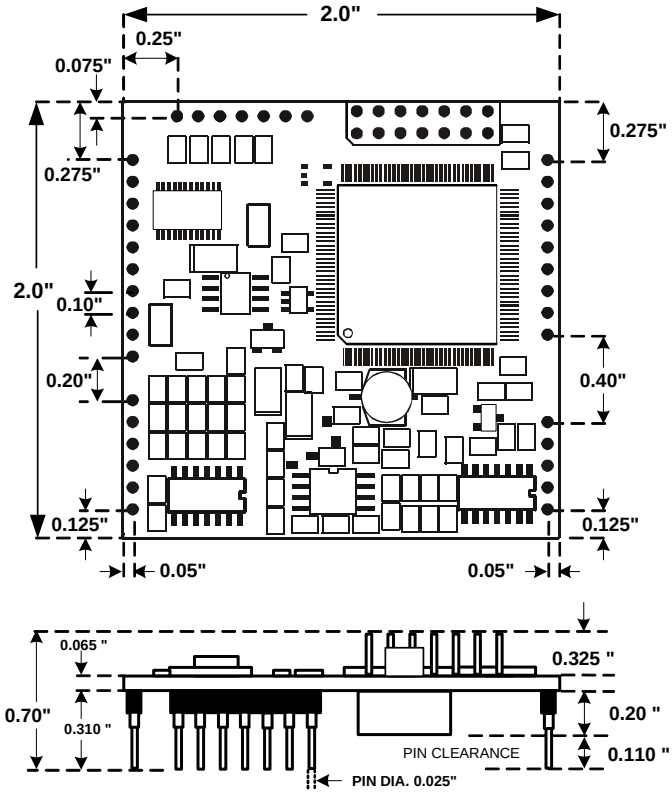
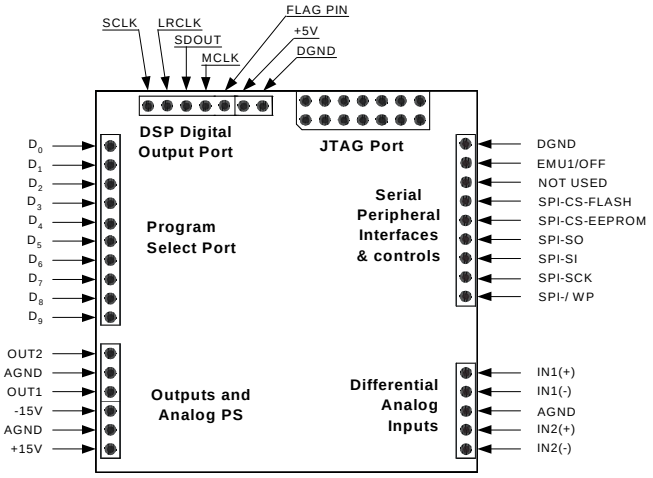


SPP-01 AND SPPDM-01
TOP VIEW
AND DIMENSIONS
All normal pin spacing 0.10"



SPPDM-01 TOP VIEW
PIN IDENTIFICATION

$D_0 – D_8$	9–bit program select pins
D_{8*}	*8-bit Ch select; Ch 1= 0, Ch 2=1
D_9	Channel 1 or 2 select
Out 1 & 2	Analog outputs
±Inputs 1&2	Differential analog inputs
± 15 Vdc	Analog Dc power In
+ 5 Vdc	Digital Power In
A Gnd	Analog Grounds (3)
D Gnd	Digital Grounds (2)
JTAG™	JTAG port, see SPPDS-01

Ordering information

SPPDM-01

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