MIC2176-1/-2/-3

Wide Input Voltage, Synchronous Buck Controllers Featuring Adaptive On-Time Control

Hyper Speed Control™ Family

General Description

The Micrel MIC2176-1/-2/-3 is a family of constant-frequency, synchronous buck controllers featuring a unique digitally modified adaptive ON-time control architecture. The MIC2176 family operates over an input supply range of 4.5V to 75V and can be used to supply up to 15A of output current. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of ±1%, and the device operates at a constant switching frequency of 100kHz, 200kHz, and 300kHz.

Micrel's Hyper Speed Control™ architecture allows for ultra-fast transient response while reducing the output capacitance and also makes (High V_{IN})/(Low V_{OUT}) operation possible. This digitally modified adaptive t_{ON} ripple control architecture combines the advantages of fixed-frequency operation and fast transient response in a single device.

The MIC2176 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, fold-back current limit, "hiccup" mode short-circuit protection and thermal shutdown.

All support documentation can be found on Micrel's web site at: www.micrel.com.

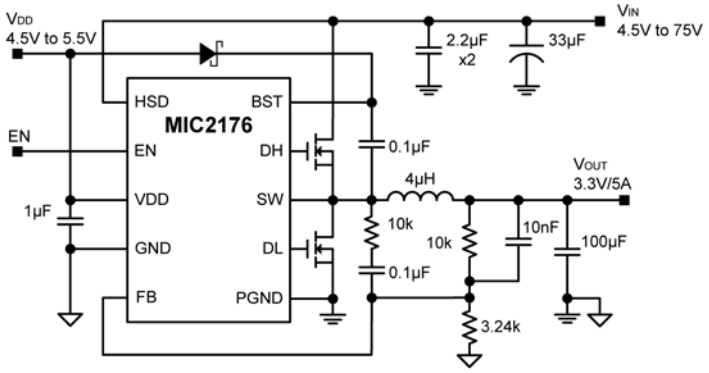
Features

- Hyper Speed Control™ architecture enables
  - High delta V operation (V_{IN} = 75V and V_{OUT} = 1.2V)
  - Small output capacitance
- 4.5V to 75V input voltage
- Output down to 0.8V with ±1% accuracy
- Any Capacitor™ Stable
  - Zero-ESR to high-ESR output capacitance
- 100kHz/200kHz/300kHz switching frequency
- Internal compensation
- 6ms Internal soft-start
- Foldback current limit and "hiccup" mode short-circuit protection
- Thermal shutdown
- Supports safe start-up into a pre-biased output
- –40°C to +125°C junction temperature range
- Available in 10-pin MSOP package

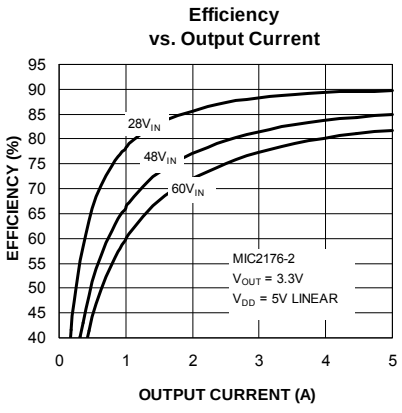
Applications

- Distributed power systems
- Networking/Telecom Infrastructure
- Printers, scanners, graphic cards and video cards

Typical Application



MIC2176-2 Adjustable Output 200KHz Buck Converter



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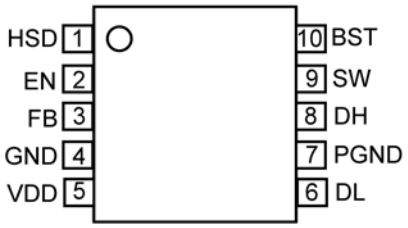
Ordering Information

Part Number	Output Voltage	Switching Frequency	Junction Temperature Range	Package	Lead Finish
MIC2176-1YMM	Adjustable	100kHz	–40°C to +125°C	10-pin MSOP	Pb-Free
MIC2176-2YMM	Adjustable	200kHz	–40°C to +125°C	10-pin MSOP	Pb-Free
MIC2176-3YMM	Adjustable	300kHz	–40°C to +125°C	10-pin MSOP	Pb-Free

Pin Configuration



10-Pin MSOP (MM)

Pin Description

Pin Number	Pin Name	Pin Function
1	HSD	High-Side MOSFET Drain Connection (Input): The HSD pin in the input of the adaptive On-time control circuitry. A 0.1uF ceramic capacitor between the HSD pin and the power ground (PGND) is required and must be place as close as possible to the IC.
2	EN	Enable (Input): A logic level control of the output. The EN pin is CMOS compatible. Logic high or floating = enable, logic low = shutdown. In the off state, the V_{DD} supply current of the device is reduced (typically 0.7mA). Do not connect the EN pin to the HSD pin.
3	FB	Feedback (Input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
4	GND	Signal ground. GND is the ground path for the device bias voltage V_{DD} and the control circuitry. The loop for the signal ground should be separate from the power ground (PGND) loop.
5	VDD	V_{DD} Bias (Input): Power to the internal reference and control sections of the MIC2176. The V_{DD} operating voltage range is from 4.5V to 5.5V. A 1µF ceramic capacitor from the VDD pin to the PGND pin must be placed next to the IC.
6	DL	Low-Side Drive (output): High-current driver output for external low-side MOSFET. The DL driving voltage swings from ground to V_{DD}.
7	PGND	Power Ground. PGND is the ground path for the buck converter power stage. The PGND pin connects to the sources of low-side N-Channel external MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal ground (GND) loop.
8	DH	High-Side Drive (output): High-current driver output for external high-side MOSFET. The DH driving voltage is floating on the switch node voltage (V_{SW}). Adding a small resistor between DH pin and the gate of the high-side N-channel MOSFETs can slow down the turn-on and turn-off time of the MOSFETs.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
9	SW	Switch Node and Current-Sense input (Input): High current output driver return. The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to the SW pin using a Kelvin connection.
10	BST	Boost (Output): Bootstrapped voltage to the high-side N-channel internal MOSFET driver. A Schottky diode is connected between the VDD pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the SW pin. Adding a small resistor in series with the BST pin can slow down the turn-on time of high-side N-Channel MOSFETs.

Absolute Maximum Ratings[1, 2]

V_{HSD} to PGND ..... –0.3V to +76V
V_{DD} to PGND ..... –0.3V to +6V
V_{SW} to PGND ..... –0.3V to (V_{HSD} +0.3V)
V_{BST} to V_{SW} ..... –0.3V to 6V
V_{BST} to PGND ..... –0.3V to 82V
V_{EN} to PGND ..... –0.3V to (V_{DD} + 0.3V)
V_{FB} to PGND ..... –0.3V to (V_{DD} + 0.3V)
PGND to GND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10sec) ..... 260°C

Operating Ratings[3]

Supply Voltage (V_{HSD}) ..... 4.5V to 75V
Bias Voltage (V_{DD}) ..... 4.5V to 5.5V
Enable Input (V_{EN}) ..... 0V to V_{DD}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
MSOP (θ_{JA}) ..... 130.5°C/W
Continuous Power Dissipation
(derate 5.6mW/°C above 70°C)
(T_A = 70°C) 421mW
ESD (Human Body Mode) 1.5kV

Electrical Characteristics[4]

V_{IN} = V_{HSD} = 48V, V_{DD} = 5V; V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input					
HSD Voltage Range (V_{HSD})[5]		**4.5**		**75**	V
V_{DD} Bias Voltage					
Operating Bias Voltage (V_{DD})		**4.5**	5	**5.5**	V
Undervoltage Lockout Trip Level	V_{DD} Rising	**3.2**	3.85	**4.45**	V
UVLO Hysteresis			370		mV
Quiescent Supply Current	V_{FB} = 1.5V		1.4	**3**	mA
Shutdown Supply Current	SW = unconnected, V_{EN} = 0V		0.7	**2**	mA
Reference					
Feedback Reference Voltage	0°C ≤ T_J ≤ 85°C (±1.0%)	**0.792**	0.8	**0.808**	V
	-40°C ≤ T_J ≤ 125°C (±1.5%)	**0.788**	0.8	**0.812**	
FB Bias Current	V_{FB} = 0.8V		5	**500**	nA
Enable Control					
EN Logic Level High	4.5V < V_{DD} < 5.5V	**1.2**	0.85		V
EN Logic Level Low	4.5V < V_{DD} < 5.5V		0.78	**0.4**	V
EN Bias Current	V_{EN} = 0V		50	**100**	µA
Oscillator					
Switching Frequency [6]	MIC2176-1	**75**	100	**125**	kHz
	MIC2176-2	**150**	200	**250**	
	MIC2176-3	**225**	300	**375**	
Maximum Duty Cycle [7]	MIC2176-1, V_{FB} = 0V, HSD=4V, V_O = 3.3V		96		%
	MIC2176-2, V_{FB} = 0V, HSD=4V, V_O = 3.3V		93		
	MIC2176-3, V_{FB} = 0V, HSD=4V, V_O = 3.3V		89		
Minimum Duty Cycle	V_{FB} > 0.8V		0		%
Minimum Off-Time			360		ns
Minimum On-Time			60		ns

Electrical Characteristics[4] (Continued)

$V_{IN} = V_{HSD} = 48V$, $V_{DD} = 5V$; $V_{BST} – V_{SW} = 5V$; $T_A = 25°C$, unless noted. **Bold** values indicate $–40°C \le T_J \le +125°C$.

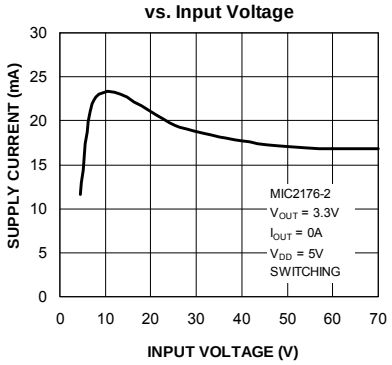
Parameter	Condition	Min.	Typ.	Max.	Units
Soft Start					
Soft-Start time			6		ms
Short Circuit Protection					
Current-Limit Threshold	$V_{FB} = 0.8V$	**103**	130	**162**	mV
Short-Circuit Threshold	$V_{FB} = 0V$	**19**	48	**77**	mV
FET Drivers					
DH, DL Output Low Voltage	$I_{SINK} = 10mA$			**0.1**	V
DH, DL Output High Voltage	$I_{SOURCE} = 10mA$	V_{DD} - 0.1V Or V_{BST} - 0.1V			V
DH On-Resistance, High State			2.1	**3.3**	Ω
DH On-Resistance, Low State			1.8	**3.3**	Ω
DL On-Resistance, High State			1.8	**3.3**	Ω
DL On-Resistance, Low State			1.2	**2.3**	Ω
SW Leakage Current	$V_{SW} = 48V$, $V_{DD} = 5V$, $V_{BST} = 53V$			**55**	µA
HSD Leakage Current	$V_{SW} = 48V$, $V_{DD} = 5V$, $V_{BST} = 53V$			**55**	µA
Thermal Protection					
Over-Temperature Shutdown	T_J Rising		160		°C
Over-Temperature Shutdown Hysteresis			25		°C

Notes:

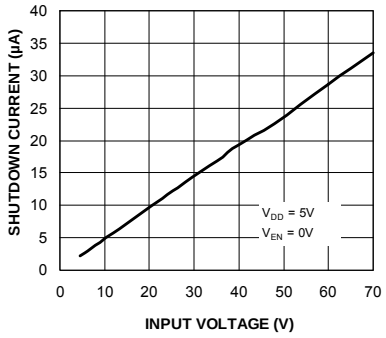
1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside operating range.
4. Specification for packaged product only.
5. The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have enough low voltage V_{TH}.
6. Measured in test mode.
7. The maximum duty-cycle is limited by the fixed mandatory off-time t_{OFF} of typically 360ns.

Typical Characteristics

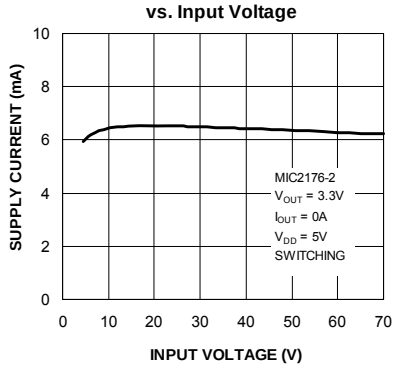
V_{IN} Operating Supply Current vs. Input Voltage



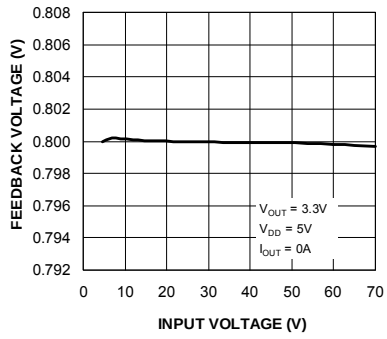
V_{IN} Shutdown Current vs. Input Voltage



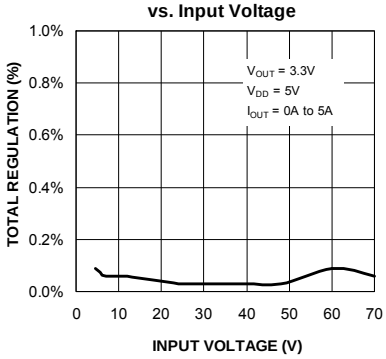
V_{DD} Operating Supply Current vs. Input Voltage



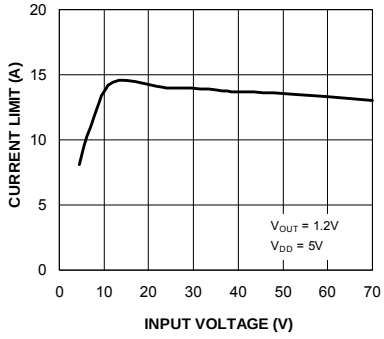
Feedback Voltage vs. Input Voltage



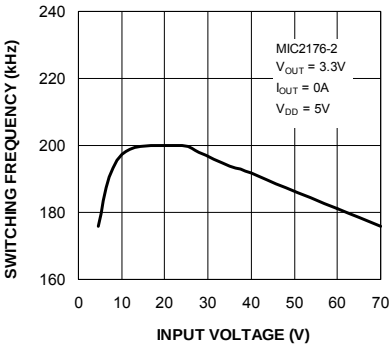
Total Regulation vs. Input Voltage



Current Limit vs. Input Voltage

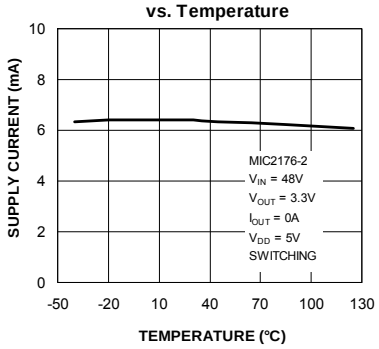


Switching Frequency vs. Input Voltage

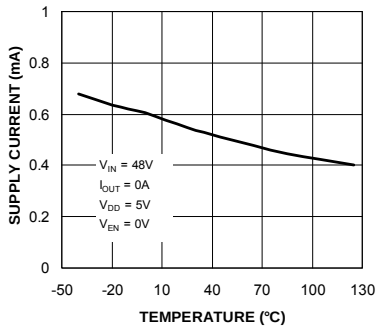


Typical Characteristics (Continued)

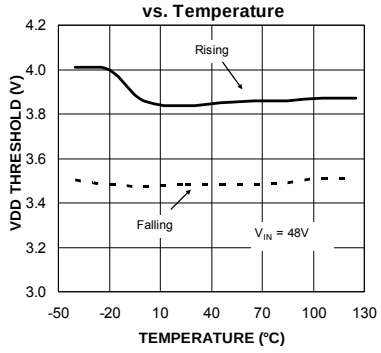
V_{DD} Operating Supply Current vs. Temperature



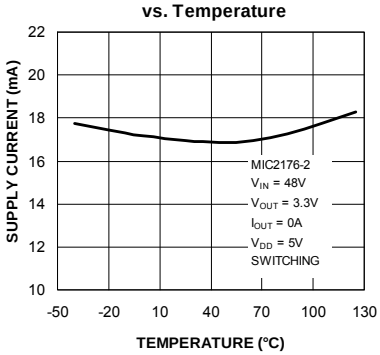
V_{DD} Shutdown Current vs. Temperature



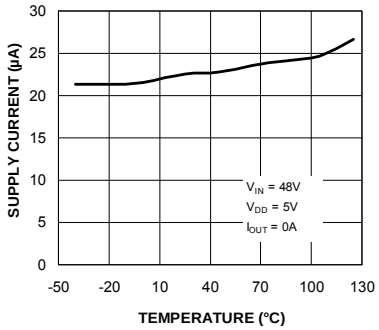
V_{DD} UVLO Threshold vs. Temperature



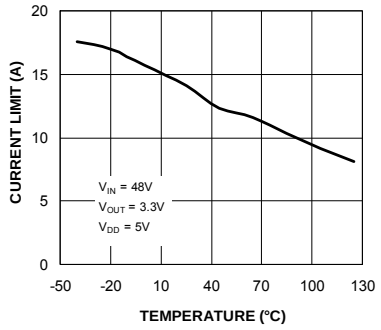
V_{IN} Operating Supply Current vs. Temperature



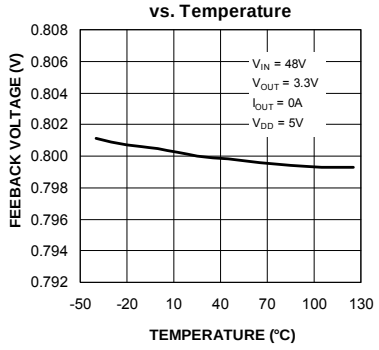
V_{IN} Shutdown Current vs. Temperature



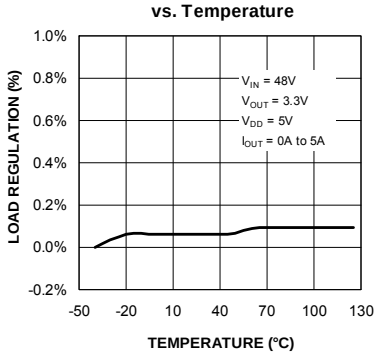
Current Limit vs. Temperature



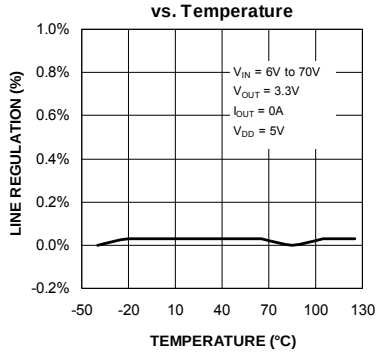
Feedback Voltage vs. Temperature



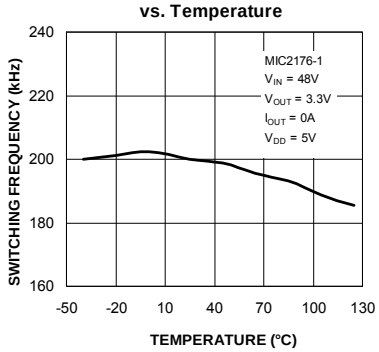
Load Regulation vs. Temperature



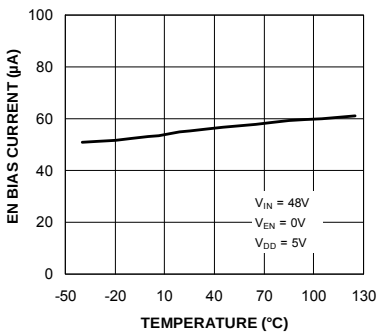
Line Regulation vs. Temperature



Switching Frequency vs. Temperature

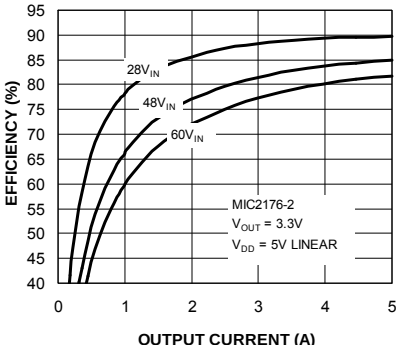


EN Bias Current vs. Temperature

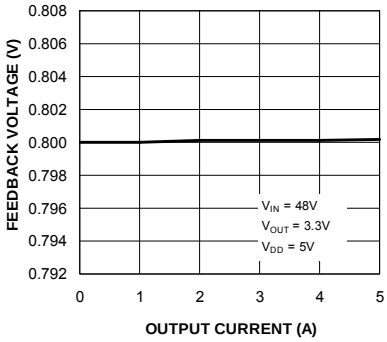


Typical Characteristics (Continued)

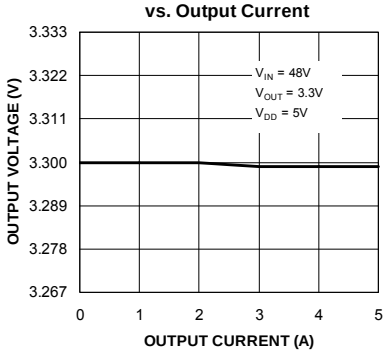
Efficiency vs. Output Current



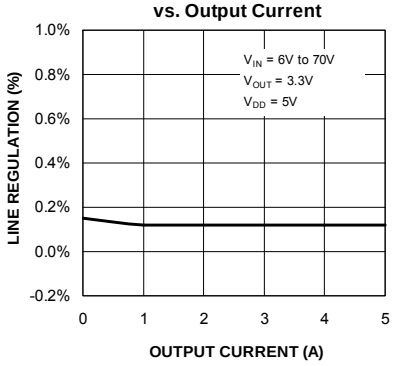
Feedback Voltage vs. Output Current



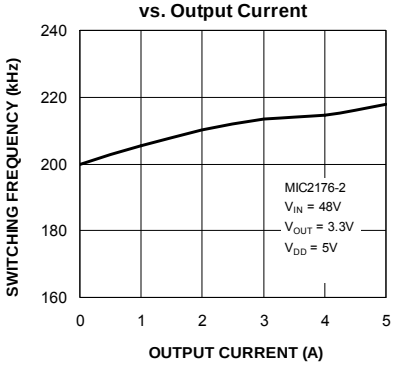
Output Voltage vs. Output Current



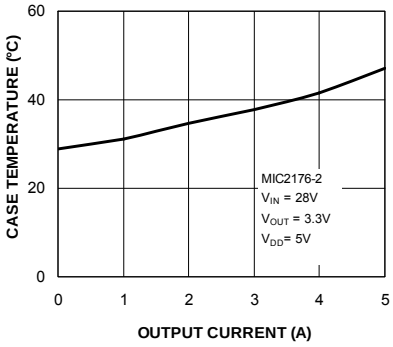
Line Regulation vs. Output Current



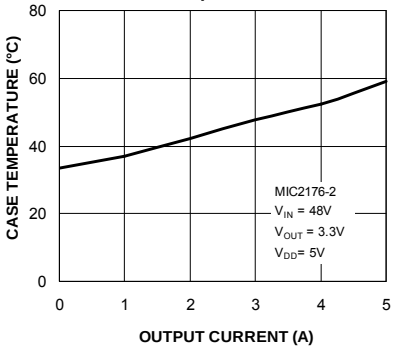
Switching Frequency vs. Output Current



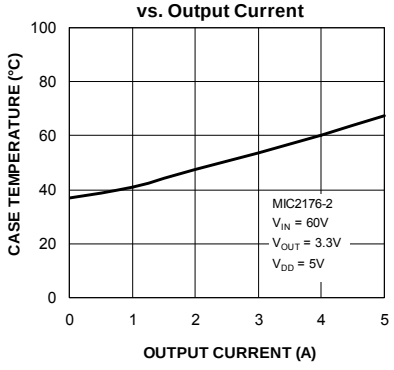
IC Case Temperature* (V_{IN} = 28V) vs. Output Current



IC Case Temperature* (V_{IN} = 48V) vs. Output Current

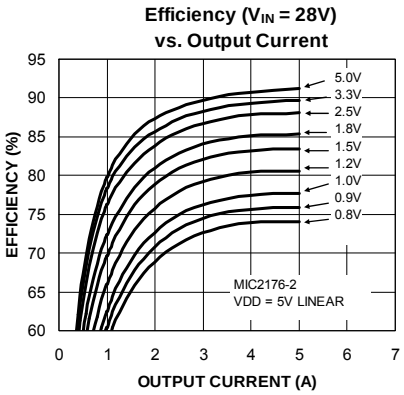


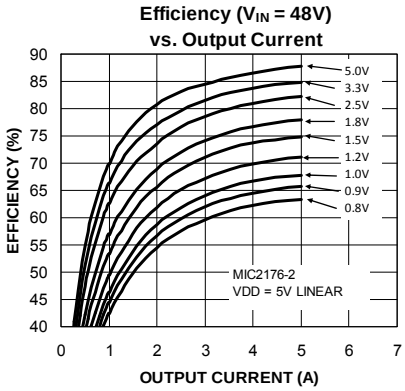
IC Case Temperature* (V_{IN} = 60V) vs. Output Current

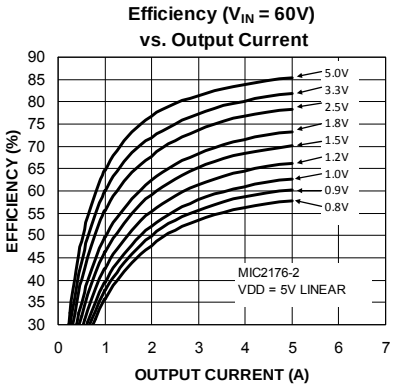


Case Temperature* : The temperature measurement was taken at the hottest point on the MIC2176 case mounted on a 5 square inch PCB, see Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

Typical Characteristics (Continued)

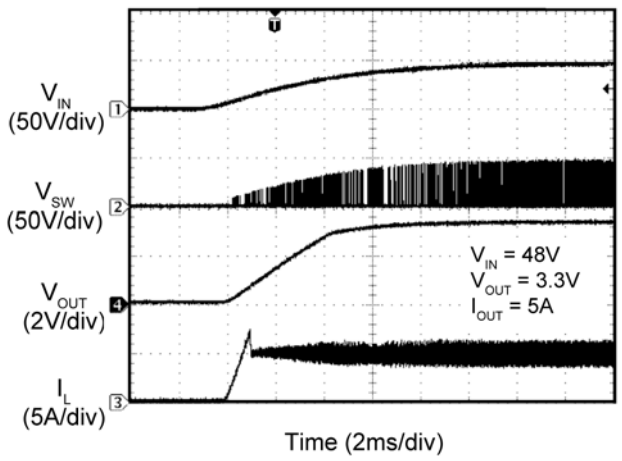




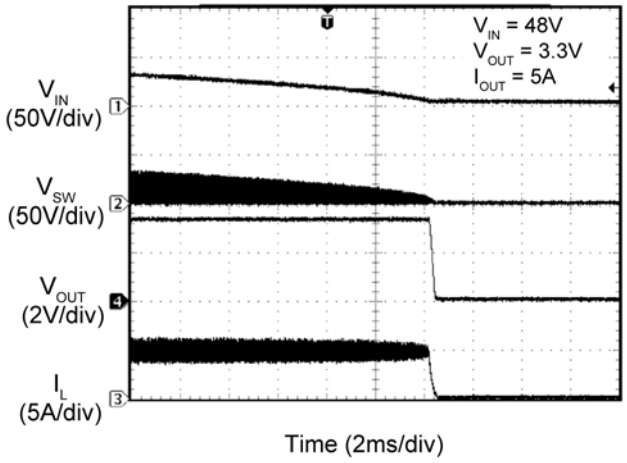


Functional Characteristics

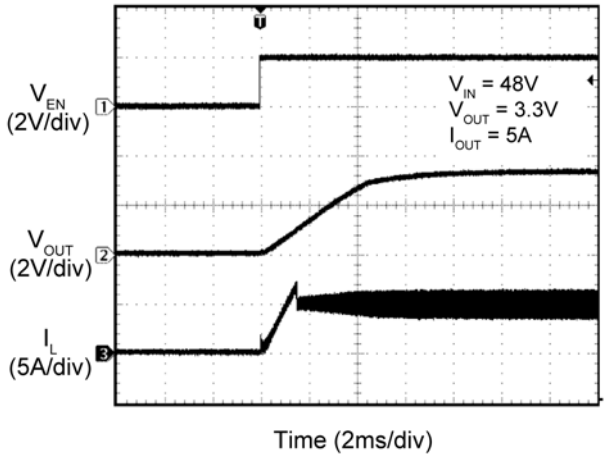
V_{IN} Soft Turn-On



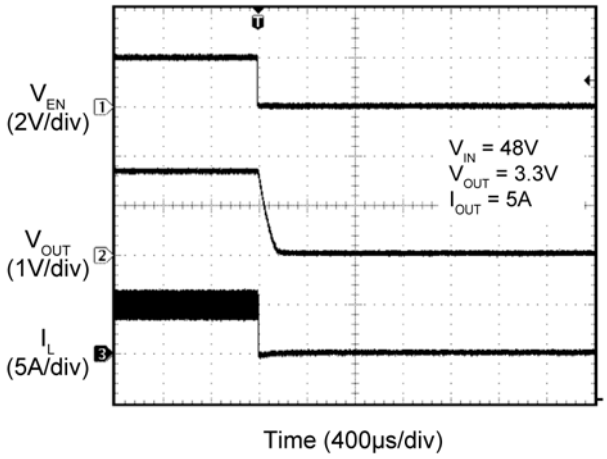
V_{IN} Soft Turn-Off



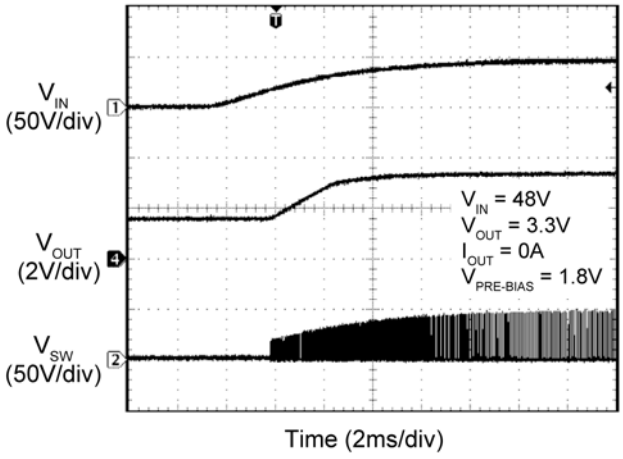
Enable Turn-On Delay and Rise Time



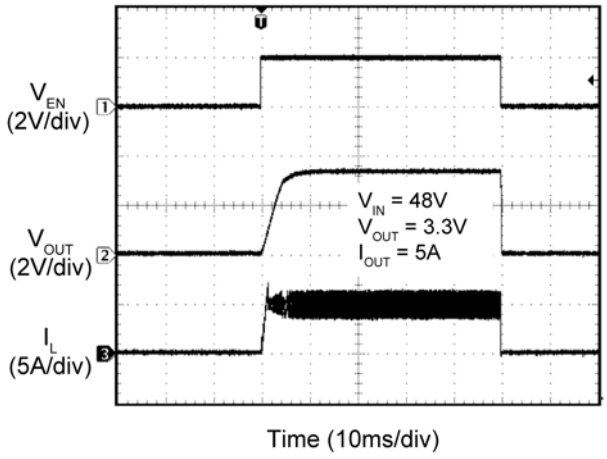
Enable Turn-Off Delay and Fall Time



V_{IN} Start-Up with Pre-Biased Output

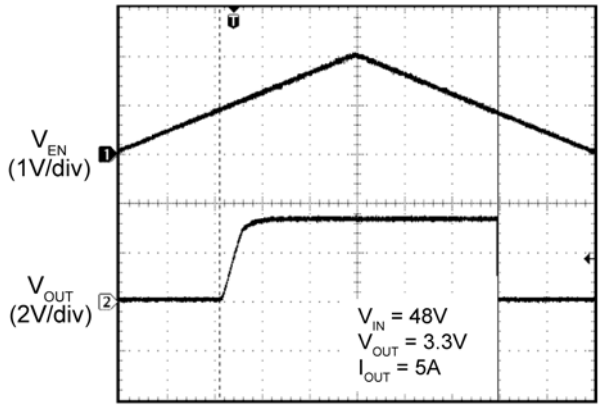


Enable Turn-On/Turn-Off

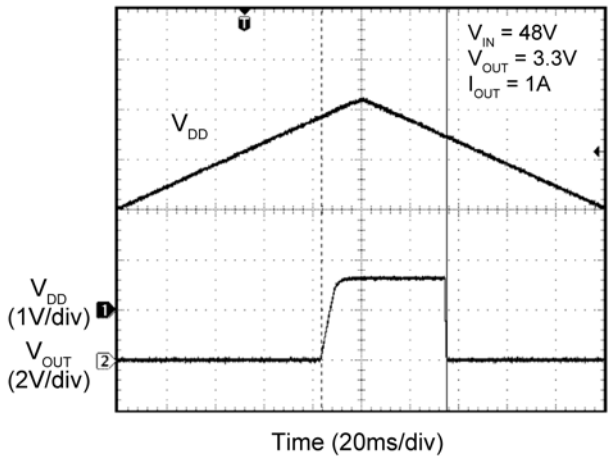


Functional Characteristics (Continued)

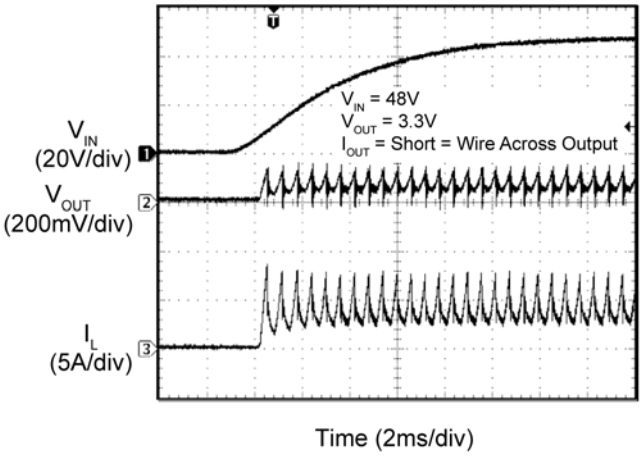
Enable Thresholds



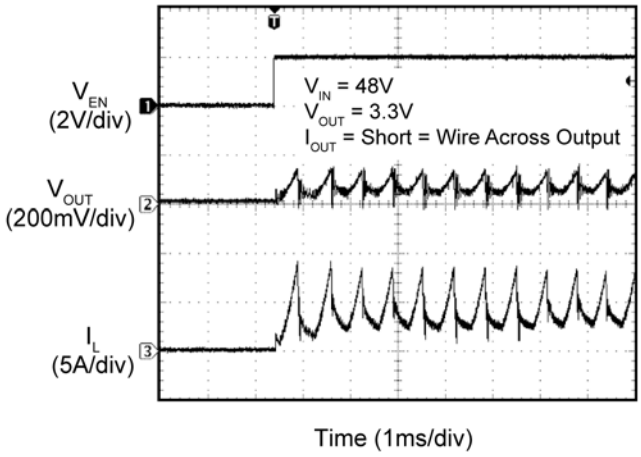
V_{DD} UVLO Thresholds



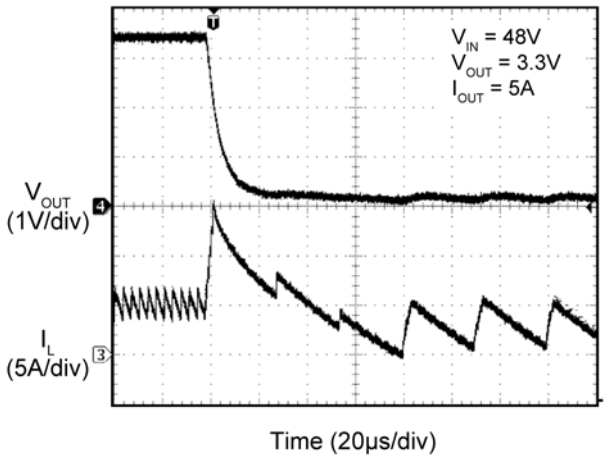
Power-Up Into Short Circuit



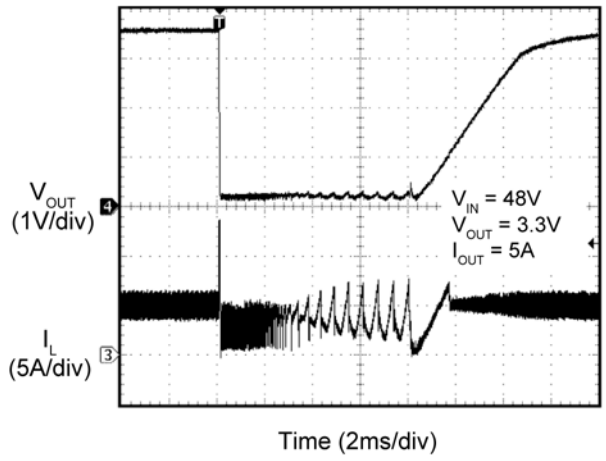
Enabled Into Short Circuit



Short Circuit

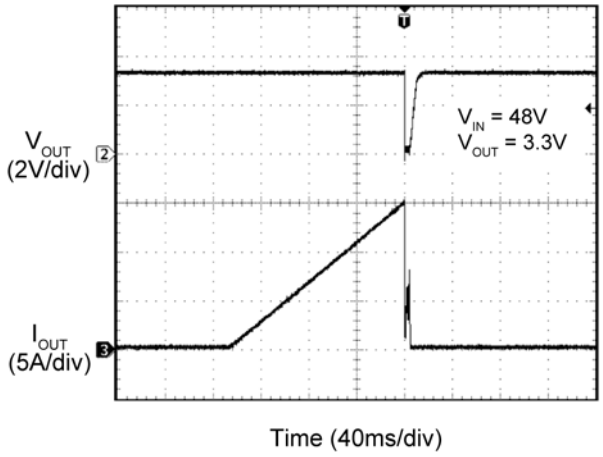


Output Recovery from Short Circuit

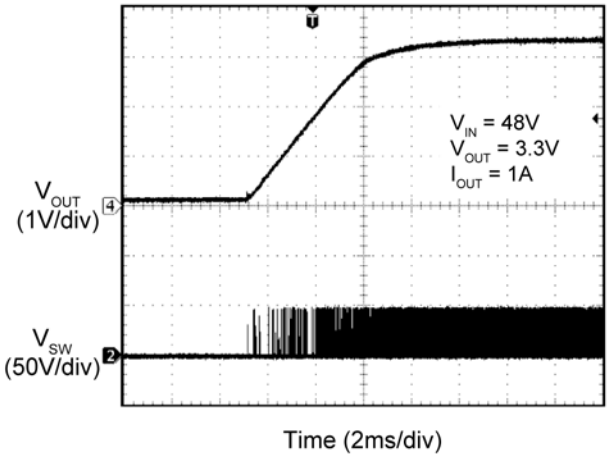


Functional Characteristics (Continued)

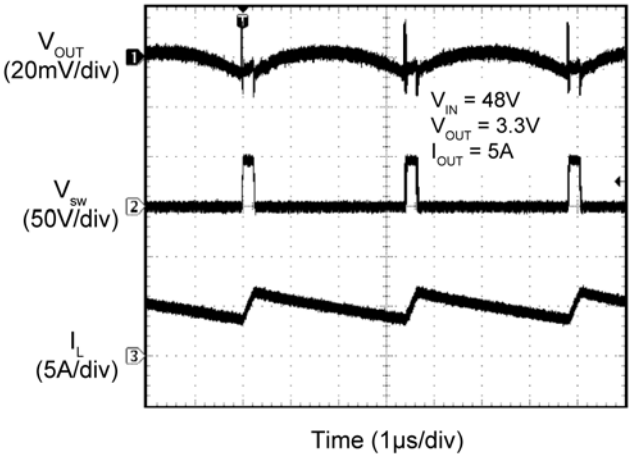
Peak Current-Limit Threshold



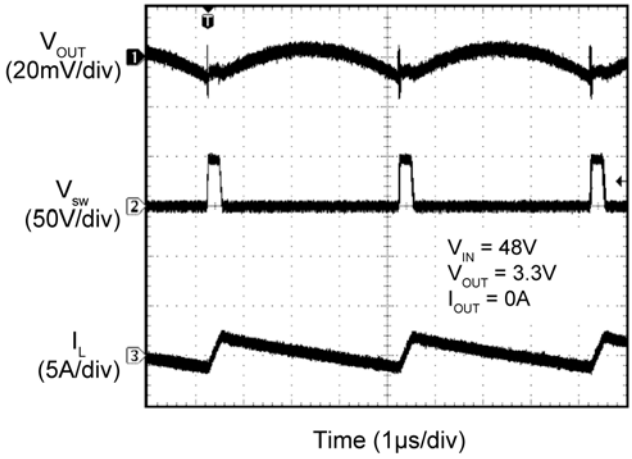
Output Recovery from Thermal Shutdown



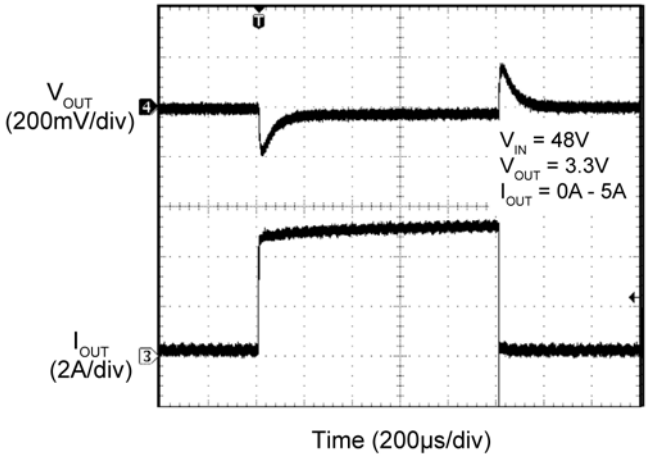
Switching Waveforms: I_{OUT} = 5A



Switching Waveforms: I_{OUT} = 0A



Transient Response



Functional Diagram

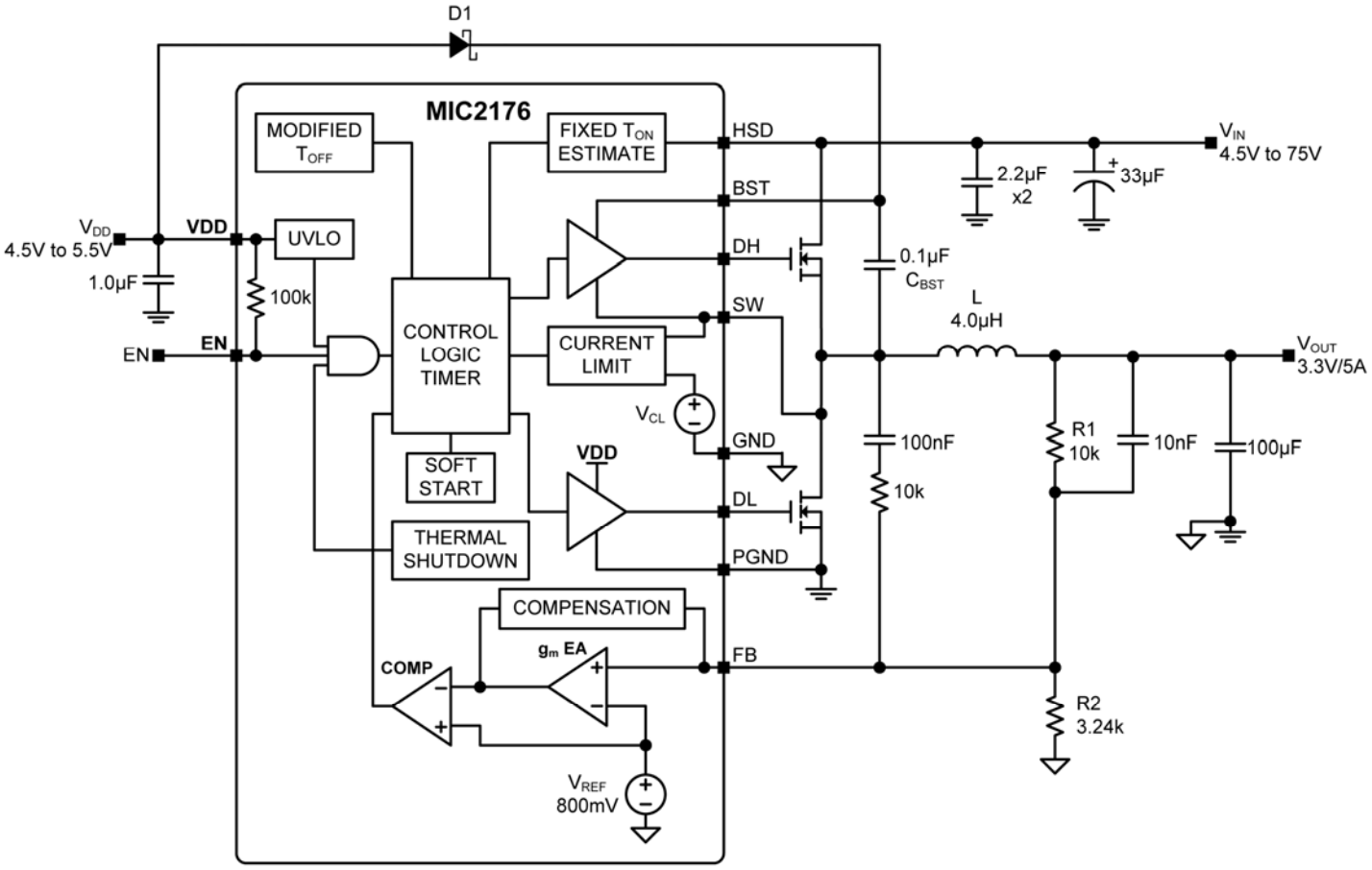


Figure 1. MIC2176 Functional Diagram

Functional Description

The MIC2176 is an adaptive on-time synchronous buck controller family built for high-input voltage and low output voltage applications. It is designed to operate over a wide input voltage range from, 4.5V to 75V and the output is adjustable with an external resistive divider. A digitally modified adaptive on-time control scheme is employed in to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown.

Theory of Operation

Figure 1 illustrates the block diagram of the MIC2176. The output voltage is sensed by the MIC2176 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the amplifier output is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (1)$$

where V_{OUT} is the output voltage, V_{IN} is the power stage input voltage, and f_{SW} is the switching frequency (100kHz for MIC2176-1, 200kHz for MIC2176-2, and 300kHz for MIC2176-3).

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 360ns, the MIC2176 control logic will apply the $t_{OFF(min)}$ instead. $t_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 360ns $t_{OFF(min)}$:

$$D_{max} = \frac{t_S - t_{OFF(min)}}{t_S} = 1 - \frac{360ns}{t_S} \quad (2)$$

where $t_S = 1/f_{SW}$. It is not recommended to use MIC2176 with a OFF-time close to $t_{OFF(min)}$ during steady-state operation.

The adpative ON-time control scheme results in a constant switching frequency in the MIC2176. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the external MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 48V to 1.0V. The minimum t_{ON} measured on the MIC2176 evaluation board is about 60ns. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 2 shows the MIC2176 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

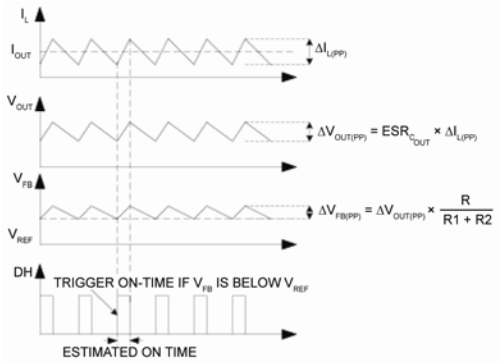


Figure 2. MIC2176 Control Loop Timing

Figure 3 shows the operation of the MIC2176 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC2176 converter.

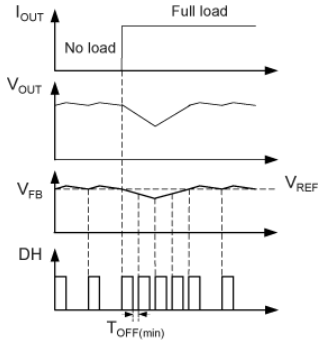


Figure 3. MIC2176 Load Transient Response

Unlike true current-mode control, the MIC2176 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The MIC2176 control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the MIC2176 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV. If a low ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to “Ripple Injection” subsection in *Application Information* for more details about the ripple injection technique.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC2176 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 6ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

Current Limit

The MIC2176 uses the $R_{DS(ON)}$ of the low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space and power losses taken by discrete current sense resistors. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC2176 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage is compared with a current-limit threshold voltage V_{CL} after a blanking time of 150ns. If the sensed voltage is over V_{CL}, which is 133mV typical at 0.8V V_{FB}, then the MIC2176 turns off the high-side and low-side MOSFETs and a soft-start sequence is triggered. This mode of operation is called “hiccup mode” and its purpose is to protect the downstream load in case of a hard short. The current limit threshold V_{CL} has a foldback characteristic related to the FB voltage. Please refer to the “Typical Characteristics” for the curve of current limit threshold vs. FB voltage percentage. The circuit in Figure 4 illustrates the MIC2176 current limiting circuit.

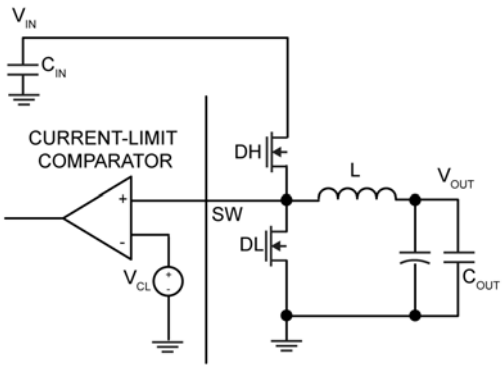


Figure 4. MIC2176 Current Limiting Circuit

Using the typical V_{CL} value of 130mV, the current-limit value is roughly estimated as:

$$I_{CL} \approx \frac{130mV}{R_{DS(ON)}} \quad (3)$$

For designs where the current ripple is significant compared to the load current I_{OUT}, or for low duty cycle operation, calculating the current limit I_{CL} should take into account that one is sensing the peak inductor current and that there is a blanking delay of approximately 150ns.

$$I_{CL} = \frac{130mV}{R_{DS(ON)}} + \frac{V_{OUT} \times T_{DLY}}{L} - \frac{\Delta I_{L(pp)}}{2} \quad (4)$$

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (1-D)}{f_{SW} \times L} \quad (5)$$

where

V_{OUT} = The output voltage

T_{DLY} = Current-limit blanking time, 150ns typical

$\Delta I_{L(pp)}$ = Inductor current ripple peak-to-peak value

D = Duty Cycle

f_{SW} = Switching frequency

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to I_{CL} in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

MOSFET Gate Drive

The MIC2176 high-side drive circuit is designed to switch an N-Channel MOSFET. Figure 1 shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. ΔBST = 10mA x 3.33µs/0.1µF = 333mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G, which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately $V_{DD} – V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

MOSFET Selection

The MIC2176 controller works from power stage input voltages of 4.5V to 73V and has an external 4.5V to 5.5V V_{IN} to provide power to turn the external N-Channel power MOSFETs for the high- and low-side switches. For applications where V_{DD} < 5V, it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for V_{GS} of 2.5V. For applications when V_{DD} > 5V; logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used.

There are different criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles. In such an application, the high-side MOSFET is required to switch as quickly as possible to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty cycle approaches 50%, the current carrying capability of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current limit. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2176 gate-drive circuit. At 300kHz switching frequency, the gate charge can be a significant source of power dissipation in the MIC2176. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[high\text{-}side]}(avg) = Q_G \times f_{SW} \quad (6)$$

where:

$I_{G[high\text{-}side]}(avg)$ = Average high-side MOSFET gate current

Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for $V_{GS} = V_{DD}$.

f_{SW} = Switching Frequency

The low-side MOSFET is turned on and off at V_{DS} = 0 because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0 instead of gate charge.

For the low-side MOSFET:

$$I_{G[low\text{-}side]}(avg) = C_{ISS} \times V_{GS} \times f_{SW} \quad (7)$$

Since the current from the gate drive comes from the V_{DD}, the power dissipated in the MIC2176 due to gate drive is:

$$P_{GATEDRIVE} = V_{DD} \times (I_{G[high\text{-}side]}(avg) + I_{G[low\text{-}side]}(avg)) \quad (8)$$

A convenient figure of merit for switching MOSFETs is the on resistance times the total gate charge $R_{DS(ON)} \times Q_G$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2176. Also, the $R_{DS(ON)}$ of the low-side MOSFET will determine the current-limit value. Please refer to "Current Limit" subsection is *Functional Description* for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{HSD}. A safety factor of 20% should be added to the V_{DS}(max) of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC} \quad (9)$$

$$P_{CONDUCTION} = I_{SW(RMS)}^2 \times R_{DS(ON)} \quad (10)$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)} \quad (11)$$

where:

$R_{DS(ON)}$ = On-resistance of the MOSFET switch

D = Duty Cycle = V_{OUT} / V_{HSD}

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{IN} + C_{OSS} \times V_{HSD}}{I_G} \quad (12)$$

where:

C_{ISS} and C_{OSS} are measured at V_{DS} = 0

I_G = Gate-drive current

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{HSD} + V_D) \times I_{PK} \times t_T \times f_{SW} \quad (13)$$

where:

t_T = Switching transition time

V_D = Body diode drop (0.5V)

f_{SW} = Switching Frequency

The high-side MOSFET switching losses increase with the switching frequency and the input voltage V_{HSD}. The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor.

A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current.

The inductance value is calculated by Equation 14:

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times 20\% \times I_{OUT(max)}} \quad (14)$$

where:

f_{SW} = Switching frequency, 300kHz

20% = Ratio of AC ripple current to DC output current

$V_{IN(max)}$ = Maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times L} \quad (15)$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \quad (16)$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(PP)}^2}{12}} \quad (17)$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2176 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor.

Copper loss in the inductor is calculated by Equation 18:

$$P_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING} \quad (18)$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$P_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \quad (19)$$

where:

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad (20)$$

where:

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 21:

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \quad (21)$$

where:

D = duty cycle

C_{OUT} = output capacitance value

f_{sw} = switching frequency

As described in the "Theory of Operation" subsection in *Functional Description*, the MIC2176 requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 22:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad (22)$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^2 \times ESR_{C_{OUT}} \quad (23)$$

Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(pk)} \times ESR_{CIN} \quad (24)$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{CIN(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1-D)} \quad (25)$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN} \quad (26)$$

Voltage Setting Components

The MIC2176 requires two resistors to set the output voltage as shown in Figure 5:

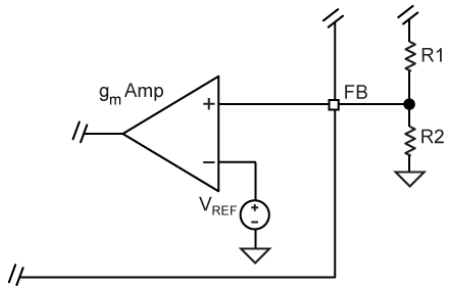


Figure 5. Voltage-Divider Configuration

The output voltage is determined by the equation:

$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2}) \quad (27)$$

where, V_{FB} = 0.8V. A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}} \quad (28)$$

Ripple Injection

The V_{FB} ripple required for proper operation of the MIC2176 g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator can't sense it, then the MIC2176 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

   As shown in Figure 6a, the converter is stable without any ripple injection. The feedback voltage ripple is:

   $$\Delta V_{FB(pp)} = \frac{R2}{R1+R2} \times ESR_{C_{OUT}} \times \Delta I_{L(pp)} \quad (29)$$

   where $\Delta I_{L(pp)}$ is the peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

   The output voltage ripple is fed into the FB pin through a feedforward capacitor C_{ff} in this situation, as shown in Figure 6b. The typical C_{ff} value is between 1nF and 100nF. With the feedforward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

   $$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \quad (30)$$

3. Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors:

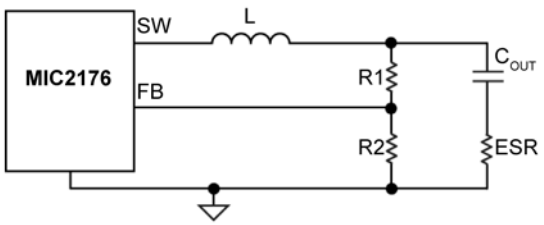


Figure 6a. Enough Ripple at FB

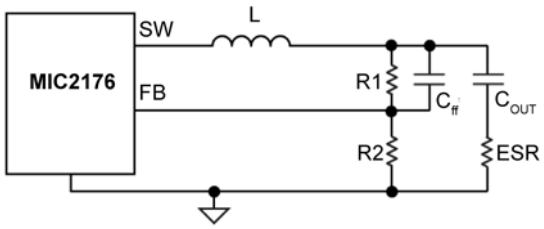


Figure 6b. Inadequate Ripple at FB

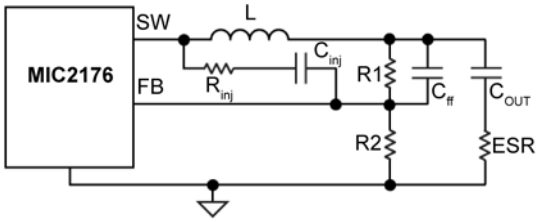


Figure 6c. Invisible Ripple at FB

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{inj} and a capacitor C_{inj}, as shown in Figure 6c. The injected ripple is:

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \quad (31)$$

$$K_{div} = \frac{R1//R2}{R_{inj} + R1//R2} \quad (32)$$

where:

V_{IN} = Power stage input voltage

D = Duty cycle

f_{SW} = Switching frequency

$\tau = (R1//R2//R_{inj}) \times C_{ff}$

In Equations 21 and 22, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1 \quad (33)$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{ff} of 1nF to 100nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor C_{inj} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1nF to 100nF if R1 and R2 are in kΩ range.

Step 2. Select R_{inj} according to the expected feedback voltage ripple using Equation 24:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1-D)} \quad (34)$$

Then the value of R_{inj} is obtained as:

$$R_{inj} = (R1//R2) \times \left(\frac{1}{K_{div}} - 1\right) \quad (35)$$

Step 3. Select C_{inj} as 100nF, which could be considered as short for a wide range of the frequencies.

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2176 converter.

IC

- The 1µF ceramic capacitor, which is connected to the VDD pin, must be located right at the IC. The VDD pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the VDD and PGND pins.
- The signal ground pin (GND) must be connected directly to the ground planes. Do not route the GND pin to the PGND pin on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the MOSFETs as possible.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

RC Snubber

- Place the RC snubber on the same side of the board and as close to the SW pin as possible.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The SW pin should be connected directly to the drain of the low-side MOSFET to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

MOSFETs

- Low-side MOSFET gate drive trace (DL pin to MOSFET gate pin) must be short and routed over a ground plane. The ground plane should be the connection between the MOSFET source and PGND.
- Chose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance to minimize the effect of dv/dt inducted turn-on.
- Do not put a resistor between the Low-side MOSFET gate drive output and the gate.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than 4.5V V_{GS} should not be used.

Evaluation Board Schematic

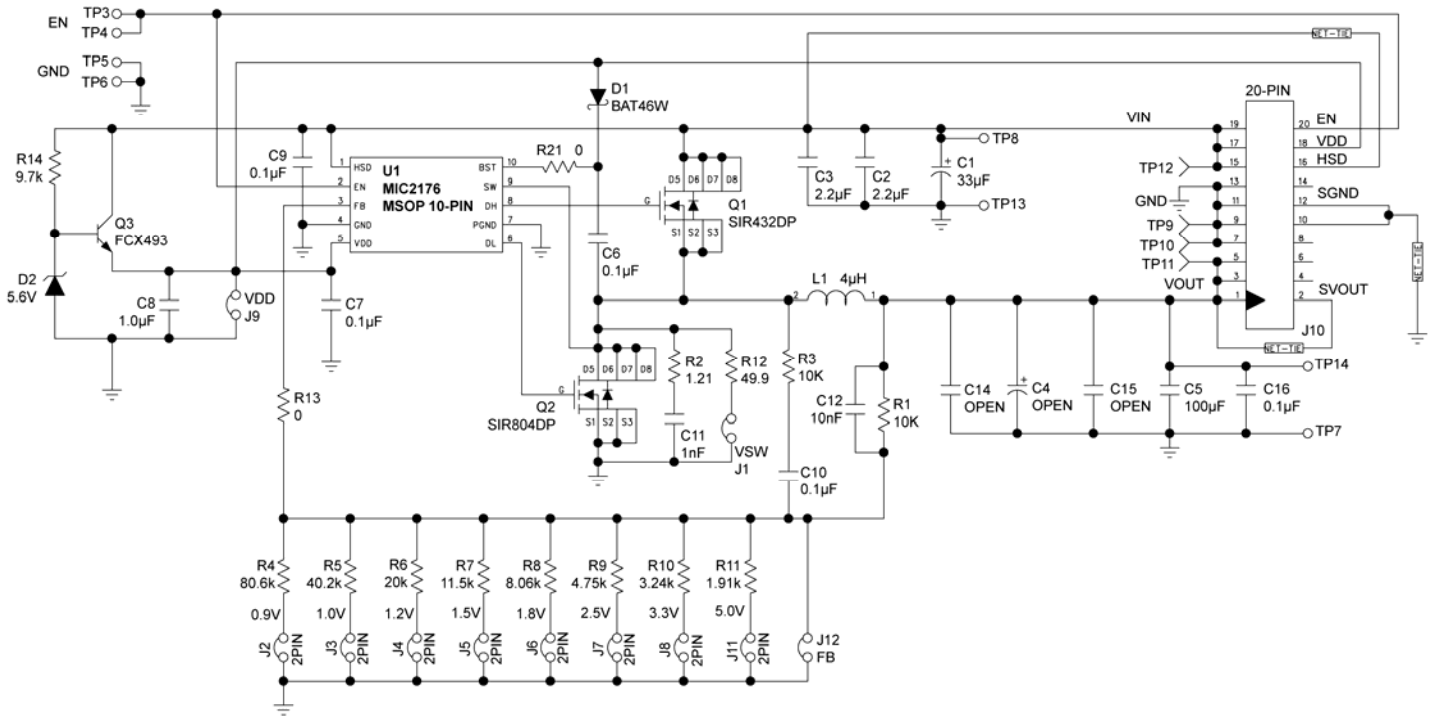


Figure 7. Schematic of MIC2176 Evaluation Board

(J1, J9, J12, R12, and R13 are for testing purposes)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
C1	B41125A9336M	EPCOS[1]	33µF Aluminum Capacitor, SMD, 100V	1
C2, C3	GRM32ER72A225K	Murata[2]	2.2µF/100V Ceramic Capacitor, X7R, Size 1210	2
C4	6SEPC470M	Sanyo[3]	470µF/6.3V OSCON Capacitor	1
C5, C15	GRM32ER60J104KA94D	Murata[2]	100µF/6.3V Ceramic Capacitor, X7R, Size 1210	2
C6, C7, C16	GRM188R71H104KA94L	Murata[2]	0.1µF/6.3V Ceramic Capacitor, X7R, Size 0603	3
C8	GRM188R70J105KA01D	Murata[2]	1µF/6.3V Ceramic Capacitor, X7R, Size 0603	1
C9, C10	GRM188R72A104KA35D	Murata[2]	0.1µF/100V Ceramic Capacitor, X7R, Size 0603	2
C11	GRM188R72A102KA01D	Murata[2]	1nF/100V Cermiac Capacitor, X7R, Size 0603	1
C12	GRM188R71H103K	Murata[2]	10nF/50V Ceramic Capacitor, X7R, Size 0603	1
C14	GRM31CR60J475KA01L	Murata[2]	4.7µF/6.3V Ceramic Capacitor, X5R, Size 1206	1
D1	BAT46W	Diodes, Inc.[4]	100V Small Signal Schottky Diode, SOD123	1
D2	CMDZ5L6	Central Semi[5]	5.6V Zener Diode, SOD323	1
L1	HCL1305-4R0-R	Cooper Bussmann[6]	4.0µH Inductor, 10A RMS Current	1
Q1	SIR432DP	Vishay[7]	MOSFET, N-CH, Power SO-8	1
Q2	SIR804DP	Vishay[7]	MOSFET, N-CH, Power SO-8	1
Q3	FCX493	ZETEX[4]	100V NPN Transistor, SOT89	1
R1, R3	CRCW060310K0FKEA	Vishay Dale[7]	10kΩ Resistor, Size 0603, 1%	2
R2	CRCW08051R21FKEA	Vishay Dale[7]	1.21Ω Resistor, Size 0805, 5%	1
R4	CRCW060380K6FKEA	Vishay Dale[7]	80.6kΩ Resistor, Size 0603, 1%	1
R5	CRCW060340K2FKEA	Vishay Dale[7]	40.2kΩ Resistor, Size 0603, 1%	1
R6	CRCW060320K0FKEA	Vishay Dale[7]	20kΩ Resistor, Size 0603, 1%	1

Notes:

1. EPCOS: www.epcos.com.
2. Murata: www.murata.com.
3. Sanyo: www.sanyo.com.
4. Diodes Inc.: www.diodes.com.
5. Central Semi: www.centralsemi.com.
6. Cooper Bussmann: www.cooperbussmann.com.
7. Vishay: www.vishay.com.

Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty
R7	CRCW060311K5FKEA	Vishay Dale[7]	11.5kΩ Resistor, Size 0603, 1%	1
R8	CRCW06038K06FKEA	Vishay Dale[7]	8.06kΩ Resistor, Size 0603, 1%	1
R9	CRCW06034K75FKEA	Vishay Dale[7]	4.75kΩ Resistor, Size 0603, 1%	1
R10	CRCW06033K24FKEA	Vishay Dale[7]	3.24kΩ Resistor, Size 0603, 1%	1
R11	CRCW06031K91FKEA	Vishay Dale[7]	1.91kΩ Resistor, Size 0603, 1%	1
R12	CRCW060349K24FKEA	Vishay Dale[7]	49.9Ω Resistor, Size 0603, 1%	1
R13, R21	CRCW06030000FKEA	Vishay Dale[7]	0Ω Resistor, Size 0603, 5%	2
R14	CRCW08059K7FKEA	Vishay Dale[7]	9.7kΩ Resistor, Size 0805, 5%	1
U1	**MIC2176-2YMM**	**Micrel. Inc.[8]**	**75V Synchronous Buck DC-DC Regulator**	**1**

Notes:

8. Micrel, Inc.: www.micrel.com.

PCB Layout

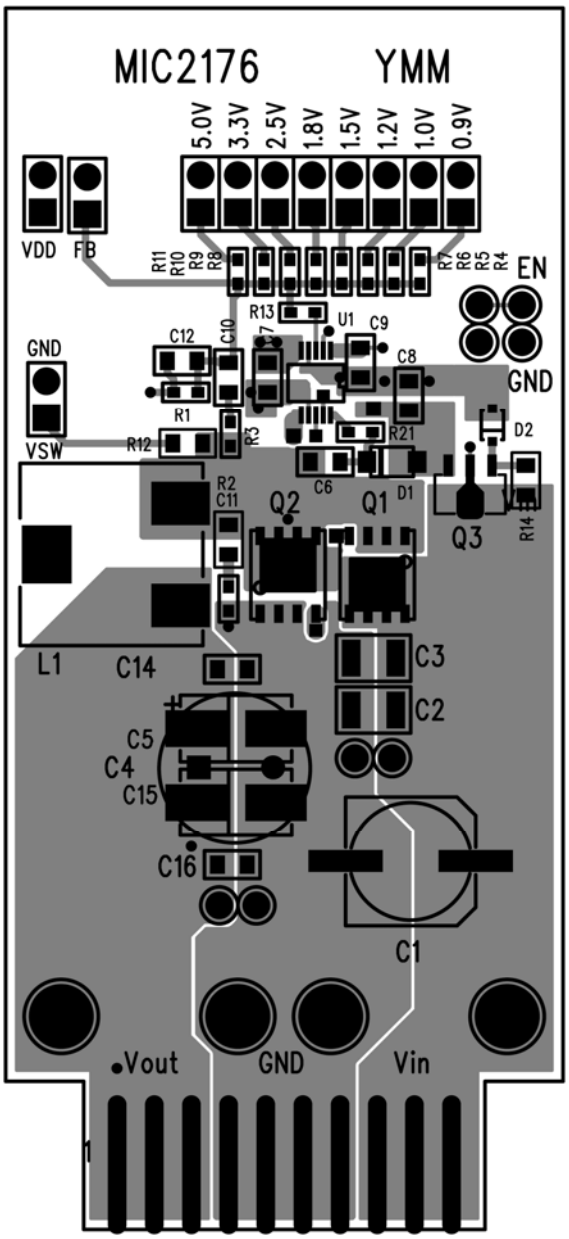


Figure 8. MIC2176 Evaluation Board Top Layer

PCB Layout (Continued)

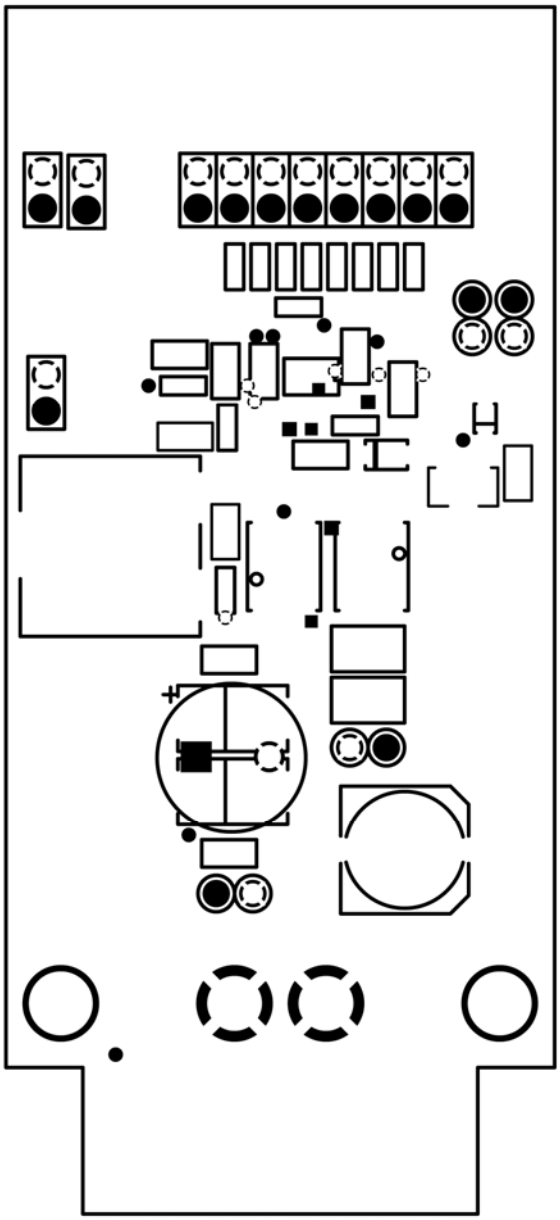


Figure 9. MIC2176 Evaluation Board Mid-Layer 1 (Ground Plane)

PCB Layout (Continued)

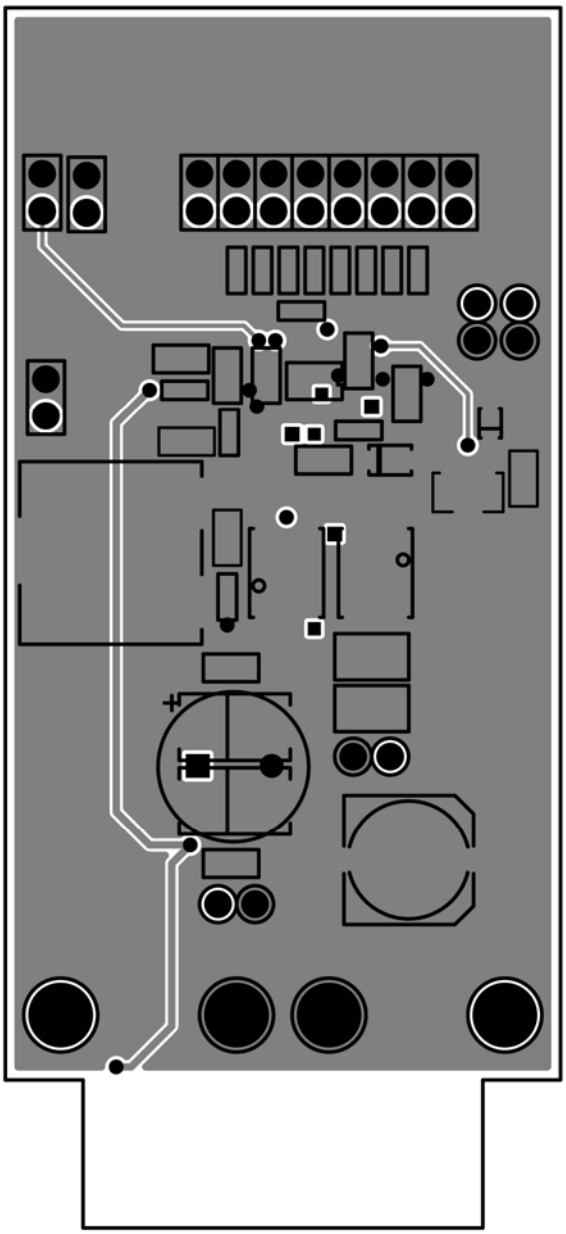


Figure 10. MIC2176 Evaluation Board Mid-Layer 2

PCB Layout (Continued)

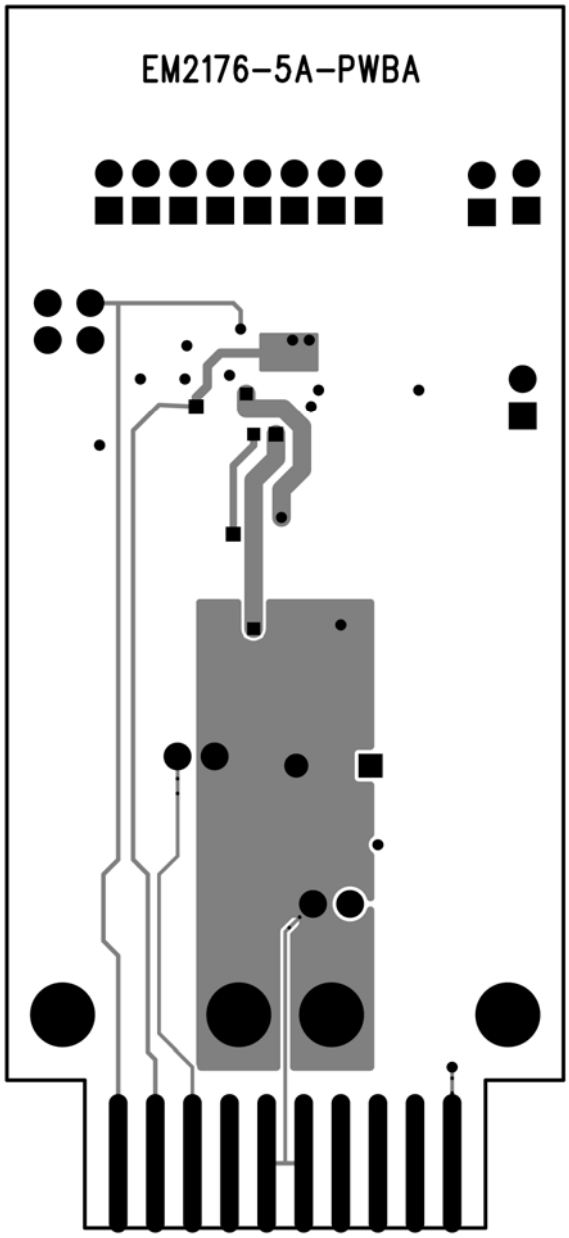
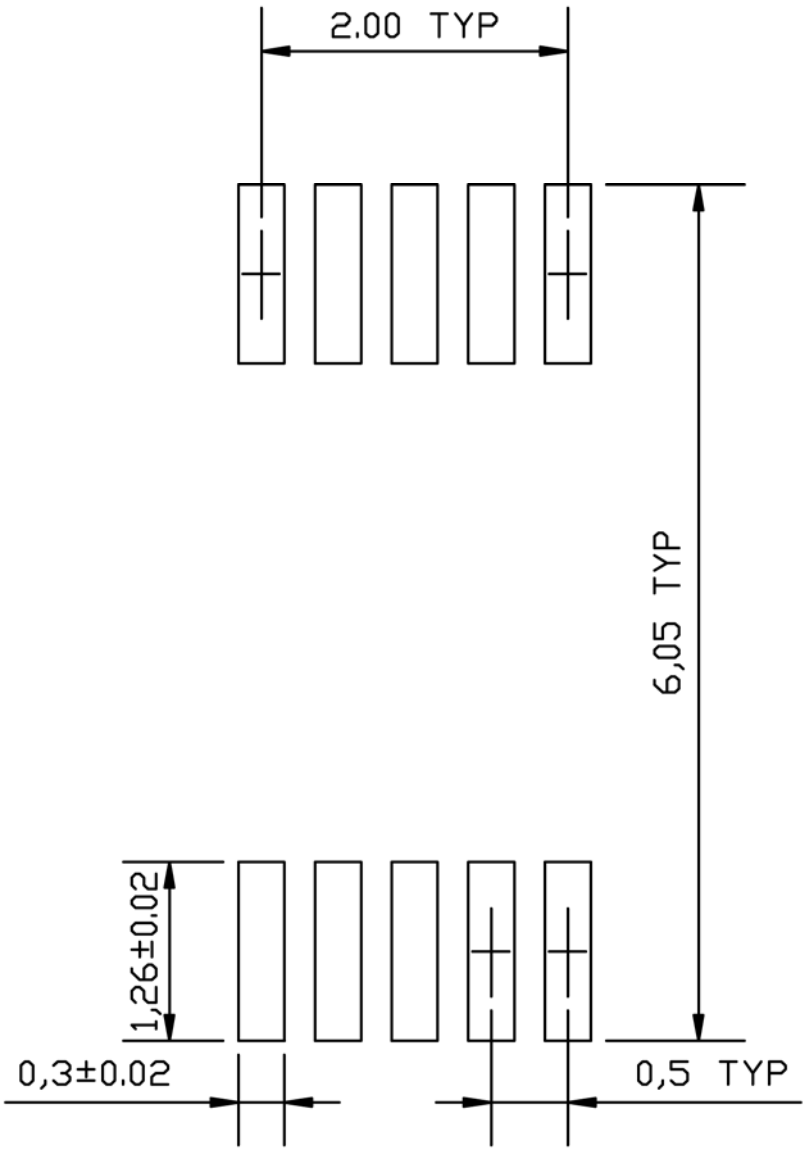


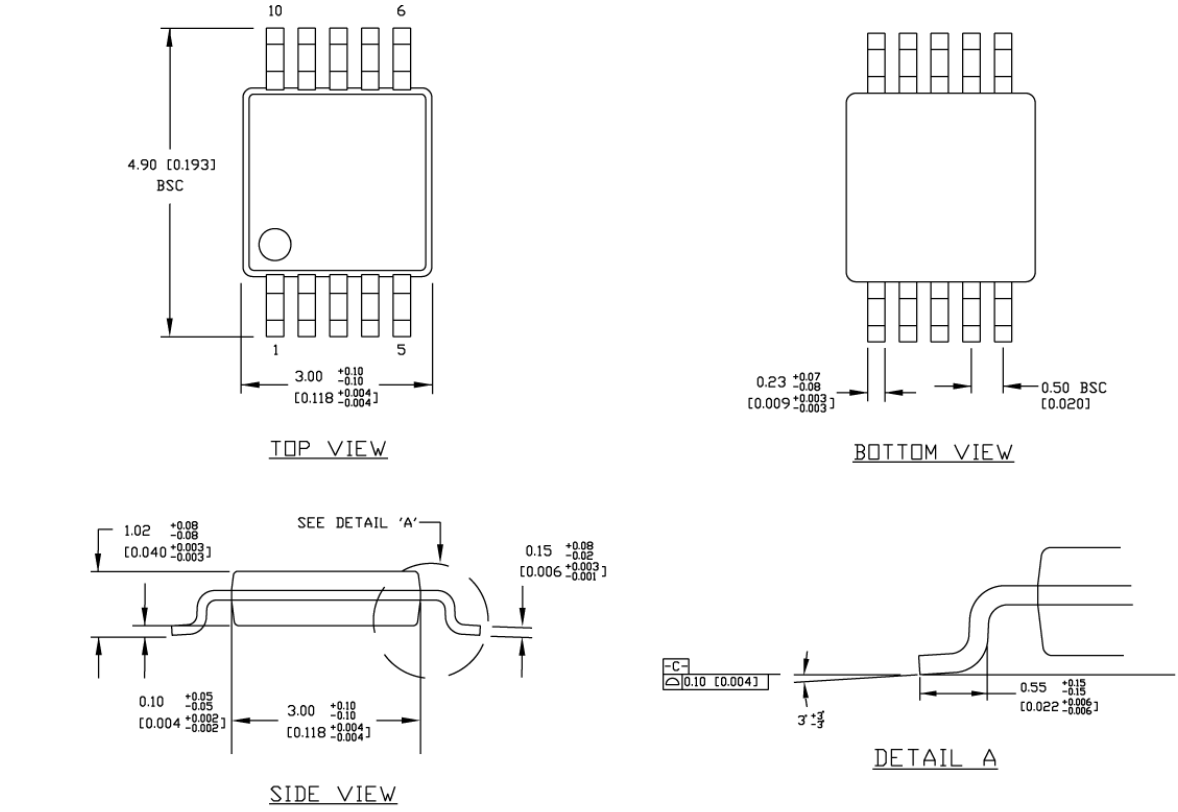
Figure 11. MIC2176 Evaluation Board Bottom Layer

Recommended Land Pattern

LP # MSOP-10LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted



Package Information



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

10-Pin MSOP (MM)

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