

MJD41C (NPN) MJD42C (PNP)

Preferred Device

Complementary Power Transistors

DPAK For Surface Mount Applications

Designed for general purpose amplifier and low speed switching applications.

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built-in Base – Emitter Resistors
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- Pb-Free Packages are Available

MAXIMUM RATINGS

| Rating | Symbol | Max | Unit |
|---|----------------|---------------|--------------------------|
| Collector-Emitter Voltage | V_{CEO} | 100 | Vdc |
| Collector-Base Voltage | V_{CB} | 100 | Vdc |
| Emitter-Base Voltage | V_{EB} | 5 | Vdc |
| Collector Current – Continuous – Peak | I_C | 6 10 | Adc |
| Base Current | I_B | 2 | Adc |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 20 0.16 | W W/ $^\circ\text{C}$ |
| Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 1.75 0.014 | W W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -65 to +150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|------|--------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 6.25 | $^\circ\text{C/W}$ |
| Thermal Resistance, Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 71.4 | $^\circ\text{C/W}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

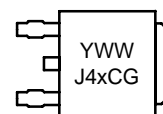
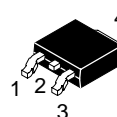


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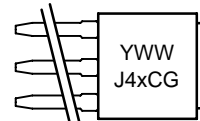
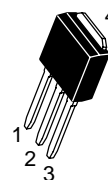
<http://onsemi.com>

SILICON POWER TRANSISTORS 6 AMPERES 100 VOLTS, 20 WATTS

MARKING DIAGRAMS



DPAK
CASE 369C
STYLE 1



DPAK-3
CASE 369D
STYLE 1

Y = Year
WW = Work Week
J4xC = Device Code
x = 1 or 2
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

MJD41C (NPN) MJD42C (PNP)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|----------------|----------|---------|-----------------|
| OFF CHARACTERISTICS | | | | |
| Collector–Emitter Sustaining Voltage (Note 2) ($I_C = 30\text{ mAdc}$, $I_B = 0$) | $V_{CEO(sus)}$ | 100 | – | Vdc |
| Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$) | I_{CEO} | – | 50 | μAdc |
| Collector Cutoff Current ($V_{CE} = 100\text{ Vdc}$, $V_{EB} = 0$) | I_{CES} | – | 10 | μAdc |
| Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}$, $I_C = 0$) | I_{EBO} | – | 0.5 | mAdc |
| ON CHARACTERISTICS (Note 2) | | | | |
| DC Current Gain ($I_C = 0.3\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$) ($I_C = 3\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$) | h_{FE} | 30 15 | – 75 | – |
| Collector–Emitter Saturation Voltage ($I_C = 6\text{ Adc}$, $I_B = 600\text{ mAdc}$) | $V_{CE(sat)}$ | – | 1.5 | Vdc |
| Base–Emitter On Voltage ($I_C = 6\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$) | $V_{BE(on)}$ | – | 2 | Vdc |
| DYNAMIC CHARACTERISTICS | | | | |
| Current Gain – Bandwidth Product (Note 3) ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 1\text{ MHz}$) | f_T | 3 | – | MHz |
| Small–Signal Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ kHz}$) | h_{fe} | 20 | – | – |

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

3. $f_T = |h_{fe}| \cdot f_{test}$.

ORDERING INFORMATION

| Device | Package Type | Package | Shipping† |
|-----------|---------------------|---------|--------------------|
| MJD41CRL | DPAK | 369C | 1800 / Tape & Reel |
| MJD41CRLG | DPAK (Pb–Free) | | |
| MJD41CT4 | DPAK | | 2500 / Tape & Reel |
| MJD41CT4G | DPAK (Pb–Free) | | |
| MJD42C | DPAK | 369D | 75 Units / Rail |
| MJD42CG | DPAK (Pb–Free) | | |
| MJD42C1 | DPAK–3 | | |
| MJD42C1G | DPAK–3 (Pb–Free) | 369C | 1800 / Tape & Reel |
| MJD42CRL | DPAK | | |
| MJD42CRLG | DPAK (Pb–Free) | | |
| MJD42CT4 | DPAK | | 2500 / Tape & Reel |
| MJD42CT4G | DPAK (Pb–Free) | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

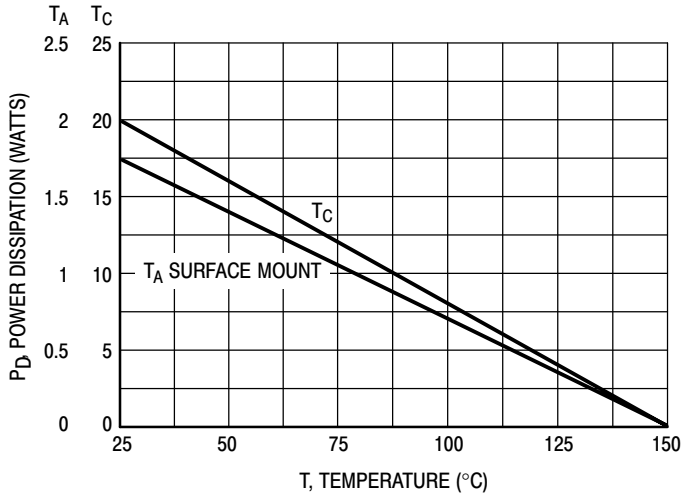
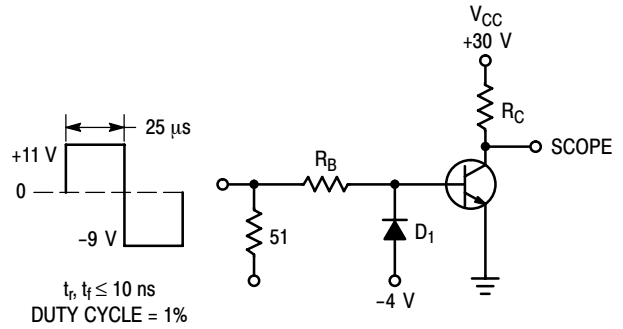


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
 D_1 MUST BE FAST RECOVERY TYPE, e.g.:
 MSB5300 USED ABOVE $I_B \approx 100$ mA
 MSD6100 USED BELOW $I_B \approx 100$ mA
 REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

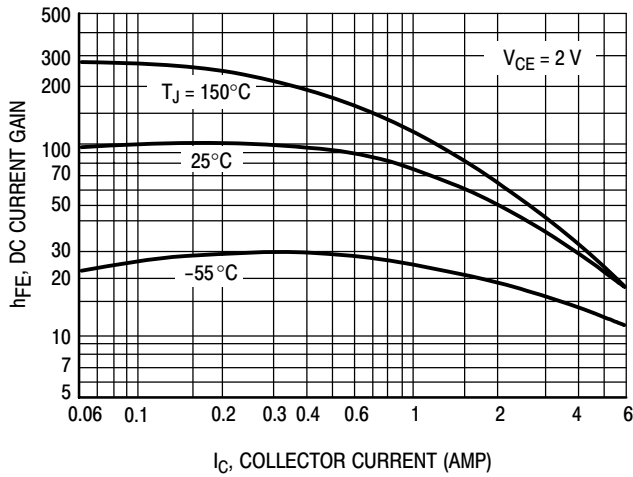


Figure 3. DC Current Gain

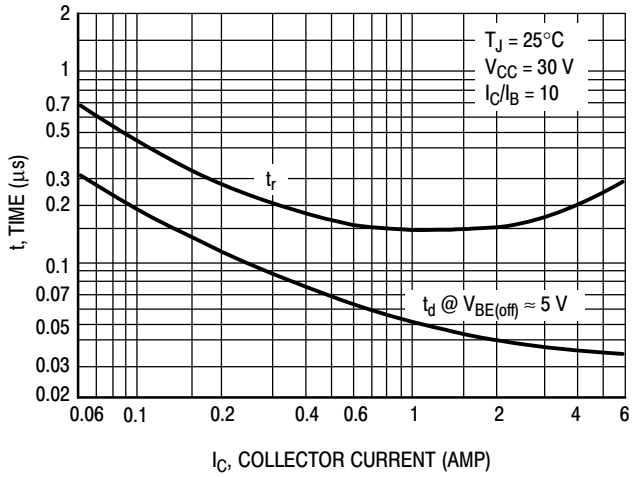


Figure 4. Turn-On Time

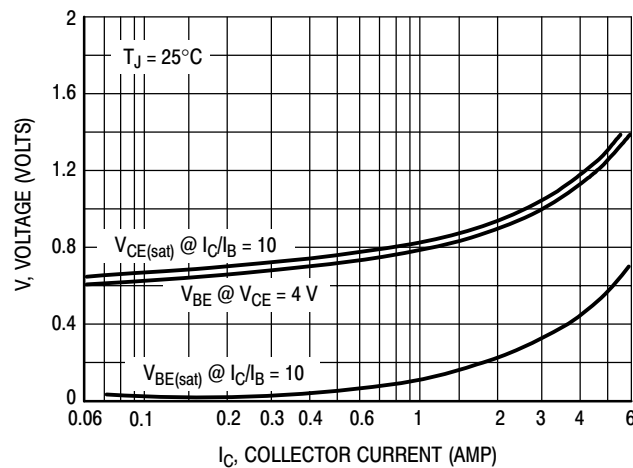


Figure 5. "On" Voltages

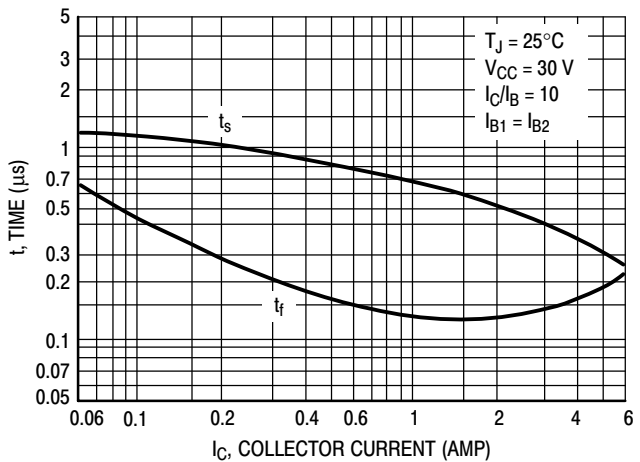


Figure 6. Turn-Off Time

MJD41C (NPN) MJD42C (PNP)

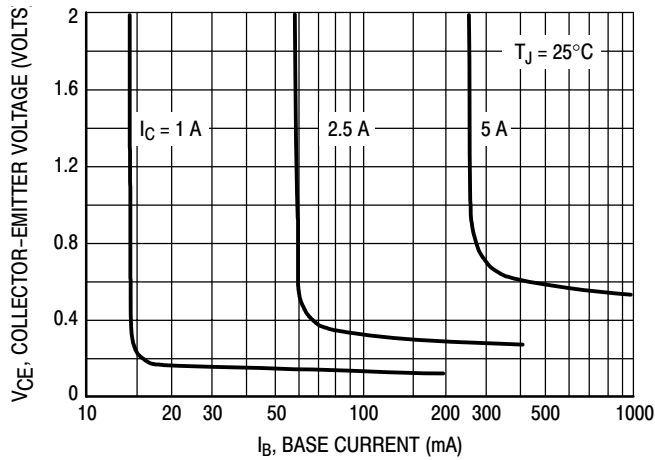


Figure 7. Collector Saturation Region

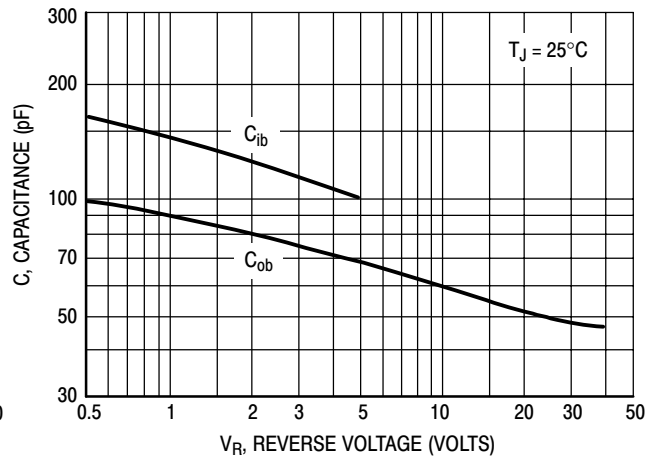


Figure 8. Capacitance

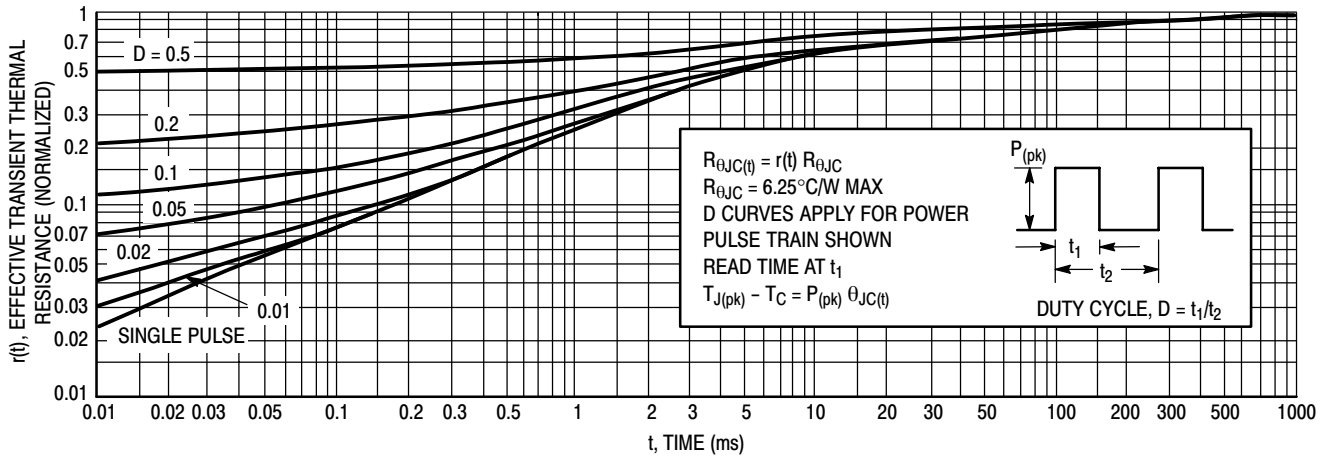


Figure 9. Thermal Response

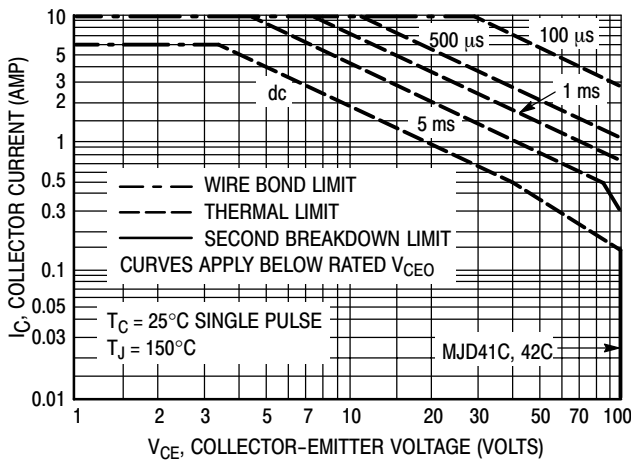


Figure 10. Maximum Forward Bias Safe Operating Area

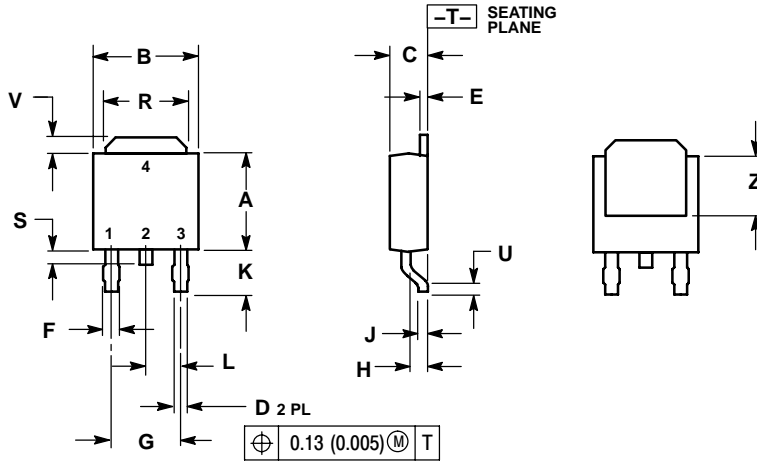
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

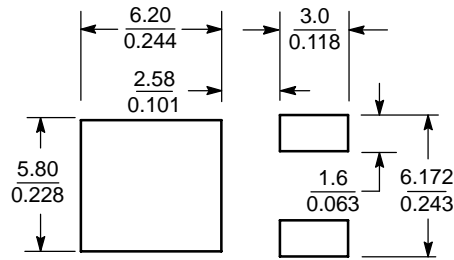


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.180 BSC | | 4.58 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.090 BSC | | 2.29 BSC | |
| R | 0.180 | 0.215 | 4.57 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | --- | 0.51 | --- |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



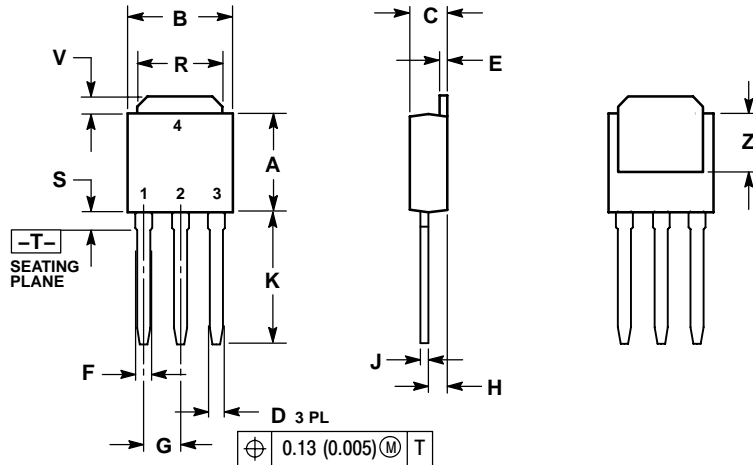
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MJD41C (NPN) MJD42C (PNP)

PACKAGE DIMENSIONS

DKPAK-3
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
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| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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