CS8130

CS8130 Revision G Addendum

Multi-Standard Infrared Transceiver (DS134F1, SEP '05)

The following items represent permanent changes to the specification of the CS8130 IR transceiver.

1) The Silicon Revision Register (Register 28) reads 0010, indicating rev G silicon.
2) The default receive sensitivity setting is changed to 00011 (Register 6 resets to 0011).
3) Oscillator low power mode is now the default condition after reset (Register 21 resets to 0100).
4) The BLKR bit (Register 4, bit D2) blocks the RXD output data during those periods when the transmit LEDs are on. This prevents the UART/system reading the transmitted data. The re-enable signal for the receiver is delayed by 8 µs from when the LEDs are turned off. Set to 1 to block RXD data, set to 0 to allow RXD data through during transmission. This bit goes to 0 upon RESET.
5) An additional control bit was added which causes the CS8130 receiver to ignore the falling edge of the IR pulse. This bit is called ENPOS, and it is bit D2 of Register #7. ENPOS is normally 1, which causes the falling edge to be ignored. This results in greater range in IrDA and high-frequency ASK (Sharp 500 kHz) modes. ENPOS should be set to 0 for low-frequency amplitude modulated modes.
6) For IrDA/HP-SIR pulse width modes, two additional control bits have been added:
   a. The THIN bit (Register 7, bit D1) allows the minimum acceptable pulse width to be reduced from 1 µs to 0.5 µs when set to 1. This bit has effect only when the receiver is programmed to mode 1a (fixed 1.6 µs pulses only) or 1c (receive 1.6 µs to 3/16 of a bit cell pulses). This bit resets to 0.
   b. The WIDE bit (Register 1, Bit D2) expands the maximum allowable pulse width to 9/16 of a bit cell when set to 1. This bit has effect only when the receiver is set to mode 1a (fixed 1.6 µs pulses only).

   For normal IrDA operation, it is recommended that THIN be set to 0 and WIDE be set to 1. Under these conditions, the qualification boundaries for receiver mode 1c (receive 1.6 µs to 3/16 of a bit cell pulses) are identical to the qualification boundaries for receiver mode 1a (fixed 1.6 µs pulses only). This bit resets to 1.
7) A TV remote receive mode hesitate bit has been added (Register 1, Bit D3). When this bit is set to 0, the RXD pin will remain high until the first valid IR signal is detected. At that time, the RXD pin will output serial data at the specified baud rate until the receiver is disabled (Register 0, bit D1). If this bit is set to 1, the RXD pin will immediately and continuously output data. This bit resets to 0.
8) The ASK transmit carrier frequency formula has changed:
   MD=(3.6864E6/FR)-2 , where MD is the Modulator Divider Value and FR is the desired modulation frequency (Registers 10 & 11). The RESET default value for MD is now 5, yielding a default carrier

frequency of 527 kHz.

9) ASK Receive Choices - valid incoming frequency range (with RATS = 0 and MD = 5) is 431 kHz to 609 kHz.

10) RATS register control of receive data frequency window period is now:
T(min) ~= [(2*MD)+3+RATS]*135ns
T(max) ~= [(2*MD)+3+(6*(RATS+1))]*135ns

11) Clarification: the IrDA/HP-SIR baud rate can be as low as 1200 bps.

12) Specifications in the following tables replace those found in the SEP '05 CS8130 data sheet (DS134F1).

POWER SUPPLY SPECIFICATIONS (T_A = 25 °C; V+ = 3.0 V, Digital Input Levels: Logic 0 = 0 V, Logic 1 = V+, Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage		2.7	3.0	5.5	V
Power Supply Current - All functions enabled (Note 2)		-	2.7	3.3	mA
Power Supply Current - All functions disabled (Note 3)		-	0.3	1	µA
Power Supply Current - Receiver only enabled (Note 2)		-	2.0	2.8	mA
Power Supply Current - Transmit only enabled (Note 4)		-	0.7	1.5	mA
Oscillator Power Supply Current low power mode: normal power mode:		- -	0.45 1.3	1.3 2.2	mA mA
Data & State Retention Supply Voltage		2	-	-	V

Notes:
1. Power supply current specifications are with the supply at 3.0 V. For approximate consumption at +5.0 V, multiply the above currents by 1.667.
2. Oscillator in low power mode; does not include LED current. Subtract oscillator current if using an external clock to run the CS8130.
3. Floating digital inputs will not cause the power supply to increase beyond the specification.
4. Does not include LED current, does include oscillator current in low power mode.

RECEIVER CHARACTERISTICS (T_A = 25 °C; V+ = 3.0 V, Digital Input Levels: Logic 0 = 0 V, Logic 1 = V+; unless otherwise specified)

Parameter		Symbol	Min	Typ	Max	Unit
Input capacitance	(Note 5)		-	10	-	pF
Input noise current			-	-	11	pA/rtHz
Maximum signal input current from detector			-	-	2	mA
Maximum DC input current (typically sunlight)			-	-	100	µA
Input current detection thresholds	(Note 6)					
(Programmable with a 5 bit value)	RS4-0 = 00010		-	98	-	nA
	RS4-0 = 00011		-	114	-	nA
	RS4-0 = 00101		-	156	-	nA
	RS4-0 = 00111		-	197	-	nA
	RS4-0 = 11111		-	724	-	nA
Bandpass filter response	High Pass -3dB		-	200	-	kHz
	Low Pass -3dB		-	900	-	kHz
Receiver power-up time	With high (100 µA) dc ambient		-	5	10	ms
	With normal (2 µA) dc ambient		-	0.3	1	ms
Turn-around time, with receiver on continuously	(Note 7)		-	5	10	ms

Notes: 5. Typical PIN diode junction capacitance is 70 pF.

6. The temperature coefficient of the receiver threshold setting is low. Current detection thresholds are above the DC ambient condition. Settings of RS4-0 of less than 00010 are not practical because of noise. RX threshold settings are roughly linear following the formula:
Threshold (nA) = (RX setting + 1) * 20 + 36.

7. Turn-around time is the time taken for the PIN diode receiver to recover from the IR energy from the local transmitter. The remote end of the link must wait for this time after receiving data before transmitting a reply. This time may be reduced to <1 ms by good IR shielding between the transmit LED to the PIN diode.

TRANSMITTER DRIVER CHARACTERISTICS (T_A = 25 °C; V+ = 3.0 V, Digital Input Levels: Logic 0 = 0 V, Logic 1 = V+, unless otherwise specified)

Parameter		Symbol	Min	Typ	Max	Unit
Output Capacitance	(Note 8)		-	70	-	pF
Output rise time (10% to 90%)		tr	-	20	50	ns
Output fall time (90% to 10%)		tf	-	20	50	ns
Overshoot over final current			-	-	25	%
On resistance			-	0.8	1.5	Ω
Off Leakage current			-	-	20	µA

Notes: 8. Typical LED junction capacitance is 20 pF.

RECOMMENDED OPERATING CONDITIONS (All voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Operating Ambient Temperature	T_A	0	25	70	°C
Data and State Retention Temperature (In Power Down)		-40	-	85	°C

DIGITAL PIN CHARACTERISTICS (T_A = 25 °C; Supply= 3.0 V)

Parameter	Symbol	Min	Typ	Max	Unit
High-level Input Voltage	V_{IH}	2.0	-	-	V
Low-level Input Voltage	V_{IL}	-	-	0.8	V
High-level Output Voltage	V_{OH}	VD - 0.3	-	-	V
Low-level Output Voltage	V_{OL}	-	-	0.3	V
Output Leakage Current in Hi-Z state		-	-	0.2	µA
Input Leakage Current (Digital Inputs)		-	-	0.2	µA
Output Capacitance	C_{OUT}	-	5	-	pF
Input Capacitance	C_{IN}	-	5	-	pF

SPEC TABLE TITLE (INSERT 5 COLUMN TABLE) Spec Table Condition

Parameter	Symbol	Min	Max	Unit
Power Supplies		-0.3	6.0	V
Input Current Except Supply Pins & Driver Pins		-	±10	mA
Input Voltage		-0.3	VD + 0.3	V
LED Output Current (each driver) (Note 9)		-	750	mA
Ambient Temperature (Power Applied)		-55	+125	°C
Storage Termperature		-65	+150	°C
ESD using humand body model (100 pF with series 1.5 kΩ)		2000	-	V

Notes: 9. 20% duty cycle, max pulse width 19.5 µs (3/16 of (1/9600 bps)).

ABSOLUTE MAXIMUM RATINGS (All voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
XTALIN/EXTCLK frequencies (Note)					
CLKFR pin low		-	3.6864	-	MHz
CLKFR pin high		-	1.8432	-	MHz
EXTCLK duty cycle (as an input)		45	50	55	%
Crystal Oscillator start up time		-	-	25	ms

Notes: 10. In normal oscillator mode, the crystal is internally loaded with 20 pF, which is the standard loading at which the crystal frequency is tuned. In low power oscillator mode, the internal loading on the crystal is reduced to approximately 5 pF. The crystal frequency will therefore increase by about 0.03% in low power mode.

REVISION HISTORY

Date	Revision	Change
NOV '97	PP2-B	Original Release
SEP '05	F1-B	Update company contact information, legal statement.
MAR '06	F1-B1	Remove invalid contact phone number.