

### General Description

The MIC5400 consists of 2 banks of 8 LED driver outputs, each output capable of sinking up to 30mA. Each bank is intended to drive 8 LED pixels of the same color. Most applications will use the MIC5400 to drive pixel clusters of 4 LEDs (RRGB.) Typically two red LEDs are used for every one green and blue to compensate for red LED brightness.

A single external resistor sets maximum drive current. Use of an external resistor allows different color LED banks to be biased to the same intensity. Brightness control is digitally programmed through the serial interface. Coarse Brightness Control is determined by two 4-bit DACs, one for each driver bank, limiting the full-scale output to a fraction of the maximum value. Additionally, each output has Fine Brightness Control using 10-bit resolution PWM.

Groups of drivers can be cascaded in Daisy Chain fashion. Open circuit output faults are detected and can be read back from the internal Status register.

### Features

- 2 banks of 8 outputs
- Output characteristics:
  - Current sink: 30mA
    - Programmable brightness control
      - Coarse: 4-bit resolution DAC
      - Fine: 10-bit resolution PWM
    - Resistor sets maximum LED current to compensate variation in LEDs
    - Current limit on each output
- Full protection:
  - Over-temperature shutdown
  - Watchdog disables output under fault condition
  - Power-on reset (all LEDs Off)
  - Soft-start on power up and watchdog recovery
  - Output open fault detection with status register readback
- Output transitions are staggered to minimize supply transients

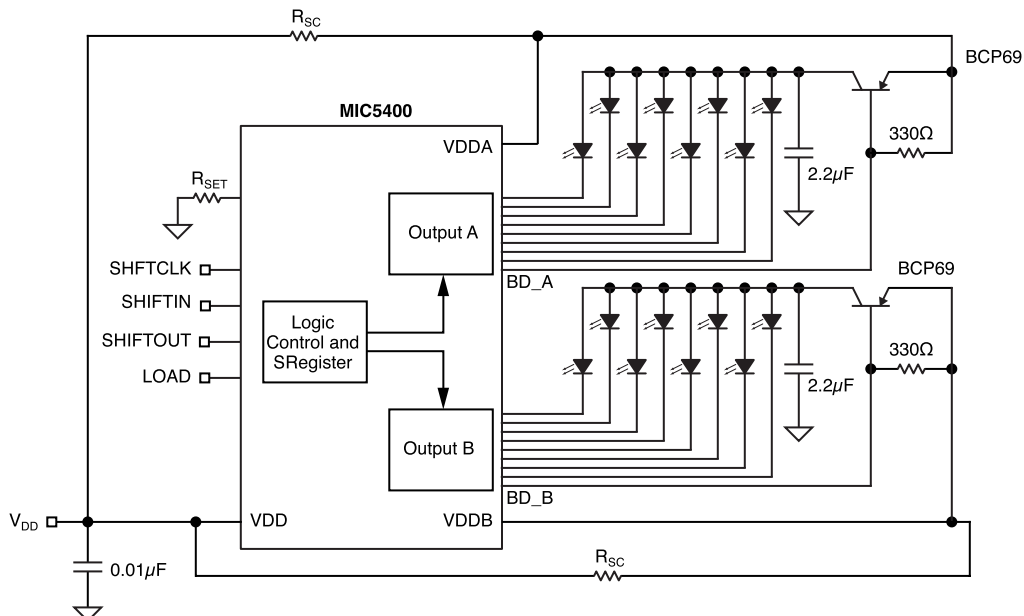
### Applications

- Outdoor video screen
- Large LED display

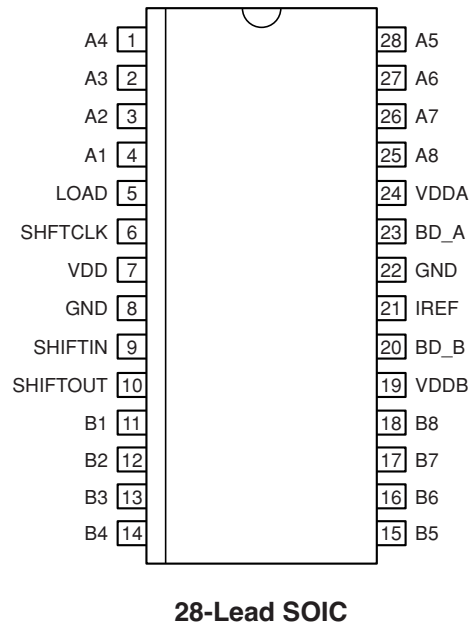
### Ordering Information

| Part Number | Junction Temp. Range | Package          |
|-------------|----------------------|------------------|
| MIC5400BWM  | -40°C to +85°C       | 28-Pin Wide SOIC |
| MIC5400YWM  | -40°C to +85°C       | 28-Pin Wide SOIC |

### Typical Application



## Pin Configuration



## Pin Description

| Pin Number  | Pin Name    | Pin Function   |
|-------------|-------------|--|
| Pin         | Name        | Function   |
| 1,2,3,4     | A4,A3,A2,A1 | Current Sink pins to be connected to LED cathodes  |
| 5           | LOAD        | If this pin is Low, the device acts as a shift register. When this pin is High, only the first falling edge of the clock transfers data from the Shift-Register to the Parallel Register. The next rising edge transfers data from the Status Register to the Shift Register |
| 6           | SHFTCLK     | Shift-register Clock Input   |
| 7           | VDD         | Positive Supply Voltage  |
| 8,22        | GND         | Ground   |
| 9           | SHIF TIN    | Shift-register Data Input  |
| 10          | SHIF TOUT   | Shift-register Data Output   |
| 11,12,13,14 | B1,B2,B3,B4 | Current Sink pins to be connected to LED cathodes  |
| 15,16,17,18 | B5,B6,B7,B8 | Current Sink pins to be connected to LED cathodes  |
| 19          | VDD B       | Analog Power source pins which provide current sense points for Channel A and Channel B PNP emitter currents, independently.   |
| 20          | BD_B        | Base Drive Outputs for external PNP transistors. Feedback Loop compensation requires one external capacitor at each PNP transistor collector.  |
| 21          | REF         | Reference current output. Must be connected to an external resistor to set the maximum current for the current sink outputs.   |
| 23          | BD_A        | Base Drive Outputs for external PNP transistors. Feedback Loop compensation requires one external capacitor at each PNP transistor collector.  |
| 24          | VDD A       | Analog Power source pins which provide current sense points for Channel A and Channel B PNP emitter currents, independently.   |
| 25,26,27,28 | A8,A7,A6,A5 | Current Sink pins to be connected to LED cathodes  |

**Absolute Maximum Ratings (Note 1)**

|   |                          |
|---|--------------------------|
| Supply Voltage .....                      | +7V                      |
| Input Voltage .....                       | -0.3V to $V_{CC} + 0.3V$ |
| Base Drive Voltage .....                  | +7V                      |
| Output Sink Current (per output) .....    | 35mA                     |
| Lead Temperature (soldering, 5 sec) ..... | 260°C                    |
| Junction Temperature ( $T_J$ )(max) ..... | 125°C                    |

**Operating Ratings (Note 2)**

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage ( $V_{CC}$ ) .....    | +4.75V to +5.5V |
| Junction Temperature ( $T_J$ ) ..... | -40°C to +125°C |
| Package Thermal Resistance           |                 |
| SOIC ( $\theta_{JC}$ ) .....         | 28°C/W          |
| SOIC ( $\theta_{JA}$ ) .....         | 100°C/W         |

**DC Electrical Characteristics**

$V_{DD} = 4.75V$  to  $5.5V$ ,  $T_A = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_A \leq +85^\circ C$ .  $R_{BIAS} = 500\Omega$ . Applies to all channels unless noted.

| Symbol           | Parameter                    | Condition        | Min        | Typ | Max        | Units   |
|------------------|------------------------------|------------------|------------|-----|------------|---------|
| $I_{OUT}$        | Output Sink Current          |                  | <b>26</b>  |     | <b>35</b>  | mA      |
| $\Delta I_{OUT}$ | Output Current Matching      |                  |            |     | <b>7</b>   | %       |
| $I_{OUT(OFF)}$   | Output Off Leakage           | $V_{OUT} = 5V$   | <b>-1</b>  |     | <b>1</b>   | $\mu A$ |
| $I_{DD}$         | Supply Current               | $V_{DD} = 5.5V$  | <b>0</b>   |     | <b>2</b>   | mA      |
| $I_B$            | PNP Base Drive Current       | $V_{BD} = 4V$    | <b>7</b>   |     | <b>50</b>  | mA      |
| $V_{REF}$        | Reference Output Voltage     | $I_{REF} = -4mA$ | <b>1.9</b> |     | <b>2.1</b> | V       |
| $V_{IH}$         | Logic 1 Input Threshold      |                  | <b>2.2</b> |     |            | V       |
| $V_{IL}$         | Logic 0 Input Threshold      |                  |            |     | <b>0.8</b> | V       |
| $V_{OH}$         | Logic 1 Output Level         | $I_{LOAD} = 1mA$ | <b>2.4</b> |     |            | V       |
| $V_{OL}$         | Logic 0 Output Level         | $I_{LOAD} = 1mA$ |            |     | <b>0.4</b> | V       |
| $T_{SHUTDOWN}$   | Thermal Shutdown Temperature |                  |            | 165 |            | °C      |

**AC Electrical Characteristics**

$V_{DD} = 4.75V$  to  $5.5V$ ,  $T_A = 25^\circ C$ , **bold** values indicate  $-40^\circ C \leq T_A \leq +85^\circ C$ .  $R_{BIAS} = 500\Omega$ . Applies to all channels unless noted.

| Symbol           | Parameter                       | Conditions   | Min       | Typ | Max        | Units   |
|------------------|---------------------------------|--|-----------|-----|------------|---------|
| $f_{SHIFT}$      | Shift Frequency                 |  |           |     | <b>15</b>  | MHz     |
| $t_{SET-DATA}$   | Set Up Time for Data In         | Note 5   | 7         |     |            | ns      |
| $t_{HOLD-DATA}$  | Hold Time for Data In           | Note 5   | 13        |     |            | ns      |
| $t_{SET-LOAD}$   | Set Up Time for Load            | Note 5   | 20        |     |            | ns      |
| $t_{HOLD-LOAD}$  | Hold Time for Load              | Note 5   | 13        |     |            | ns      |
| $t_{OUT(tr)}$    | Rise Time $I_{OUT}$             | Note 4, 5  |           |     | <b>125</b> | ns      |
| $t_{OUT(ttf)}$   | Fall Time $I_{OUT}$             | Note 4, 5  |           |     | <b>50</b>  | ns      |
| $t_{D-SHIFT}$    | Clock to Shift Out Delay        | Rise and Fall, 50% $C_{LOAD} = 30pF$ , <b>Note 5</b> |           |     | <b>23</b>  | ns      |
| $t_{r,f-OUT}$    | Shift Out Rise and Fall Time    | 10% to 90%; $C_{LOAD} = 30pF$ , <b>Note 5</b>        |           |     | <b>10</b>  | ns      |
| $t_{WD-TIMEOUT}$ | Watch Dog Timeout Delay         | No Shiftclock  | <b>25</b> |     | <b>200</b> | $\mu s$ |
| $t_{r,ff[in]}$   | Logic Input Rise and Fall Times |  |           |     | 10         | ns      |

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating rating.

**Note 3.** Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

**Note 4.** Test circuit shown in Figure 1.

**Note 5.** Guaranteed by design; not production tested.

### Test Circuit

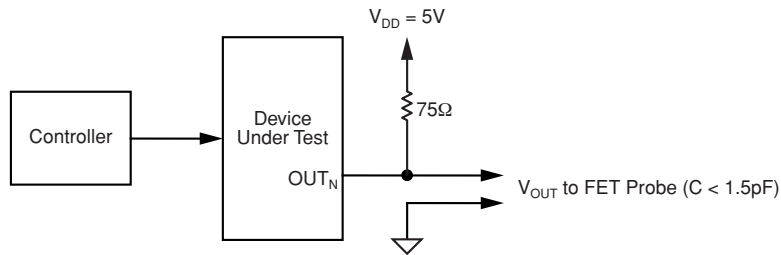


Figure 1. AC Output Test Circuit

### Timing Diagrams

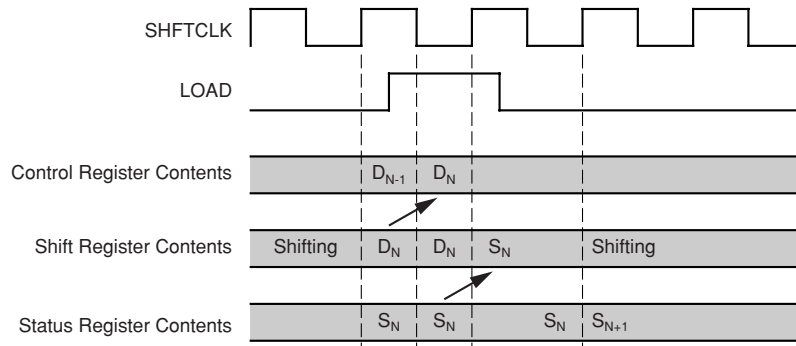


Figure 2. MIC5400 Timing Diagram

### Linearity

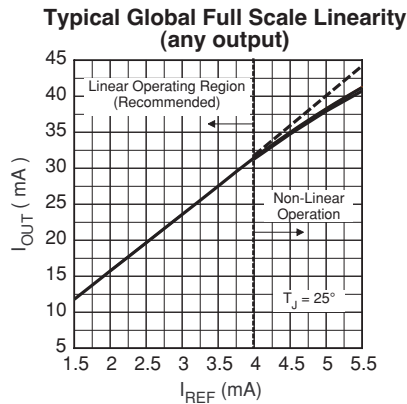
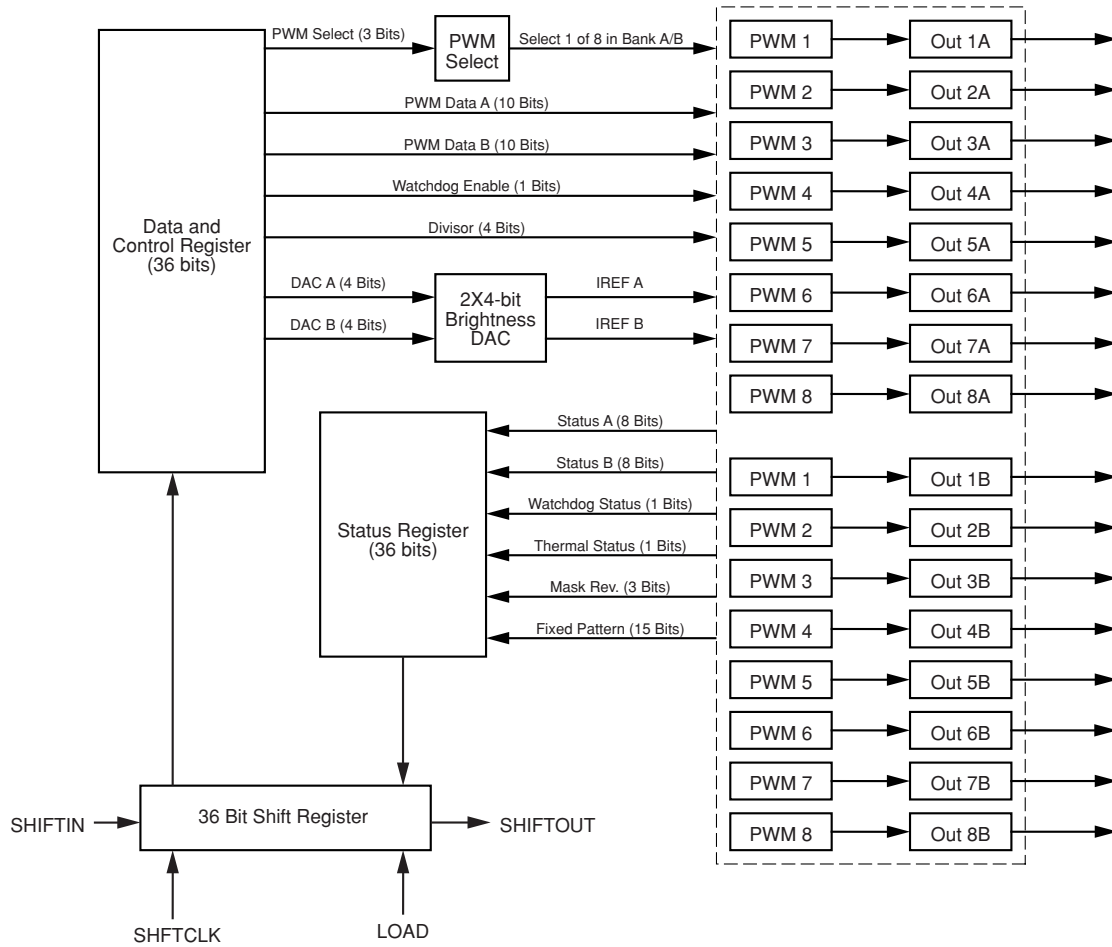


Figure 3. Typical Global Full Scale Linearity

# Functional Diagram



**MIC5400 Functional Diagram**

| Address                | Data A    | Data B     | Watchdog | Divisor    | DAC B      | DAC B      |
|------------------------|-----------|------------|----------|------------|------------|------------|
| 3 Bits                 | 10 bits   | 10 Bits    | 1 Bit    | 4 Bits     | 4 Bits     | 4 Bits     |
| Q1 to Q3<br>[Q1 = LSB] | Q4 to Q13 | Q14 to Q23 | Q24      | Q25 to Q28 | Q29 to Q32 | Q33 to Q36 |

| Bit | Description                |
|-----|----------------------------|
| 1   | Address bit 1              |
| 2   | Address Bit 2              |
| 3   | Address Bit 3              |
| 4   | Data A Bit 1               |
| 5   | Data A Bit 2               |
| 6   | Data A Bit 3               |
| 7   | Data A Bit 4               |
| 8   | Data A Bit 5               |
| 9   | Data A Bit 6               |
| 10  | Data A Bit 7               |
| 11  | Data A Bit 8               |
| 12  | Data A Bit 9               |
| 13  | Data A Bit 10              |
| 14  | Data B Bit 1               |
| 15  | Data B Bit 2               |
| 16  | Data B Bit 3               |
| 17  | Data B Bit 4               |
| 18  | Data B Bit 5               |
| 19  | Data B Bit 6               |
| 20  | Data B Bit 7               |
| 21  | Data B Bit 8               |
| 22  | Data B Bit 9               |
| 23  | Data B Bit 10              |
| 24  | Watchdog Bit [Disable = 1] |
| 25  | Divisor Bit 1              |
| 26  | Divisor Bit 2              |
| 27  | Divisor Bit 3              |
| 28  | Divisor Bit 4              |
| 29  | DAC A Bit 1                |
| 30  | DAC A Bit 2                |
| 31  | DAC A Bit 3                |
| 32  | DAC A Bit 4                |
| 33  | DAC B Bit 1                |
| 34  | DAC B Bit 2                |
| 35  | DAC B Bit 3                |
| 36  | DAC B Bit 4                |

**Table 1. Shift Register Data Format**

| Status A<br>[1 = Open Circuit] | Status B<br>[1 = Open Circuit] | Watchdog<br>[1 = Timeout] | Thermal<br>[1 = Overtemp] | Mask Revision | Alternating Bits |
|--------------------------------|--------------------------------|---------------------------|---------------------------|---------------|------------------|
| 8 Bits                         | 8 Bits                         | 1 Bit                     | 1 Bit                     | 3 Bits        | 15 Fixed Bits    |
| D1-D8                          | D9-D16                         | D17                       | D18                       | D19 to D21    | D22 to D36       |

| Bit | Description                                |
|-----|--|
| 1   | Status A - Bit 1 (Output Open Circuit = 0) |
| 2   | Status A - Bit 2 (Output Open Circuit = 0) |
| 3   | Status A - Bit 3 (Output Open Circuit = 0) |
| 4   | Status A - Bit 4 (Output Open Circuit = 0) |
| 5   | Status A - Bit 5 (Output Open Circuit = 0) |
| 6   | Status A - Bit 6 (Output Open Circuit = 0) |
| 7   | Status A - Bit 7 (Output Open Circuit = 0) |
| 8   | Status A - Bit 8 (Output Open Circuit = 0) |
| 9   | Status B - Bit 1 (Output Open Circuit = 0) |
| 10  | Status B - Bit 2 (Output Open Circuit = 0) |
| 11  | Status B - Bit 3 (Output Open Circuit = 0) |
| 12  | Status B - Bit 4 (Output Open Circuit = 0) |
| 13  | Status B - Bit 5 (Output Open Circuit = 0) |
| 14  | Status B - Bit 6 (Output Open Circuit = 0) |
| 15  | Status B - Bit 7 (Output Open Circuit = 0) |
| 16  | Status B - Bit 8 (Output Open Circuit = 0) |
| 17  | Watchdog Status [0 = Normal, 1 = Time Out] |
| 18  | Thermal Status [0 = Normal, 1 = Overtemp]  |
| 19  | Mask Revision Bit 1                        |
| 20  | Mask Revision Bit 2                        |
| 21  | Mask Revision Bit 3                        |
| 22  | 0 [Fixed Pattern Filler Bits]              |
| 23  | 1  |
| 24  | 0  |
| 25  | 1  |
| 26  | 0  |
| 27  | 1  |
| 28  | 0  |
| 29  | 1  |
| 30  | 0  |
| 31  | 1  |
| 32  | 0  |
| 33  | 1  |
| 34  | 0  |
| 35  | 1  |
| 36  | 0  |

Table 2. Status Word Format

## Applications Information

**Output Current Drive**

The MIC5400 includes several ways to program LED output current. These output current controls are superimposed and have an additive effect on LED output current as follows:

**Global Full Scale Current Limit:**

This function sets the Global Full Scale (GFS) current at each of the outputs. The GFS value current is about 8.1 times I<sub>SET</sub>. I<sub>SET</sub> is the current through the single resistor, R<sub>BIAS</sub>, connected from VREF to Ground. VREF is regulated to 2V (nominal) so:

$$I_{SET} = \frac{V_{REF}}{R_{BIAS}} = \frac{(2V)}{R_{BIAS}} \text{ and } GFS = \frac{[8.1] \times [2V]}{R_{BIAS}}$$

$$\text{For } R_{BIAS} = 500\Omega, GFS = \approx 32.4\text{mA}$$

The recommended value for I<sub>SET</sub> is 4mA or less for linear operation. See Figure 3.

**Brightness Control**

Brightness control is provided by two, 4-bit DACs, one DAC for each of the two output banks of 8 outputs. The output current is varied between 0\*GFS and (15/16)\*GFS in 15 equal steps based on the 4 Bit DAC code from the shift register Data Word; Bits Q29-Q32 control Output Bank A and Bits QA33-36 control Output Bank B. (See Table 1: Data Word Format). Watchdog Status is read back from Status Word Bit Q17. Thermal Status is read from Status Word Bit Q18.

**Output Intensity**

Each LED Output intensity is further controlled by a Pulse Width Modulator providing 10-bit resolution intensity variation. One LED output per bank can be set up for each Data Word. A 3-bit address selects 1 of the 8 PWMs for each of the two output banks. Programming bits Q1-Q3 determine the PWM address, bits Q4-Q13 control the PWMs driving Bank A, bits Q14-Q23 control the PWMs driving Bank B. The PWM is created by comparing the count of a 10-bit counter with the 10-bit programming word. If the count output is greater than the programming word, the output is "OFF".

The PWM frequency is also programmable, in ratio to the frequency of the shift register clock. The ratio value is set by the Divisor, loaded into bits Q25-Q28 of the Data Word. See Table 3.

**Watchdog and Thermal Shutdown**

The MIC5400 incorporates both a watchdog and thermal shutdown.

The watchdog shuts off all outputs and sets watchdog status bit to logic 1 if the shift clock is absent for more than 200 microseconds. Watchdog status remains logic 0 for shift clocks more frequent than 25 microseconds. The watchdog is enabled by data word bit Q24. Watchdog status is read back from status word bit D17.

As a result of the 25 microsecond minimum watchdog timeout delay, the lower limit of clock frequency is 40kHz. The thermal shutdown typically activates if the die temperature exceeds 165°C. Thermal shutdown shuts off all outputs and sets the Thermal status bit to logic 1 if over-temperature is detected. Thermal status is read back from status word bit D18.

**External PNP Transistors**

The external PNPs have a dual role. As part of a voltage regulator loop they aid in limiting package power dissipation. Sensing current in the PNP emitters also allows setting an overall limit to the current available to one bank of 8 LEDs.

Power dissipation: The regulator loop controls the voltage at the LED drive output to limit power dissipation. The outputs are typically controlled to 1.1V. A 2.2 μF capacitor is required at the collector of each PNP for frequency compensation.

**PNP Current Limit**

The current limit of the external PNP can be set by connecting a sense resistor R<sub>CS</sub> from VDD to VDDA and VDDDB respectively. The current limit is:

$$I_{LIM} = \frac{48\text{mV}}{R_{SC}}$$

If current limit is not used, short VDDA and VDDDB to VDD.

**Daisy Chains**

Parts may be cascaded in groups of arbitrary size. The SHIFTOUT pin of one part is connected to the SHIFTIN pin of the following part. Data bit 36 is the first bit data to be shifted in. Status bit 36 is the first status bit to be shifted out. (See Table 1 and Table 2)

When loading the 36-bit data words, the user must keep track of the number of SHIFTCLOCK cycles to determine when data is aligned for transfer to the control and PWM registers. For example, if one daisy chains 10 parts, 360 SHIFTCLOCK cycles are required to clock in all the data words.

**LOAD and the Data/Control and Status Registers:**

When LOAD is low, the MIC5400 acts as a 36-bit shift register. When LOAD goes high, the part no longer shifts data. Data is transferred from the Shift Register to the parallel control registers on the first falling edge of SHIFTCLOCK after LOAD goes high. While LOAD remains high, the next rising edge of SHIFTCLOCK transfers data from the status registers to the shift register. The first status bit to appear on SHIFTOUT is Status Filler Bit 36 (Logic 0). See Table 2 for description and Figure 2 for timing.

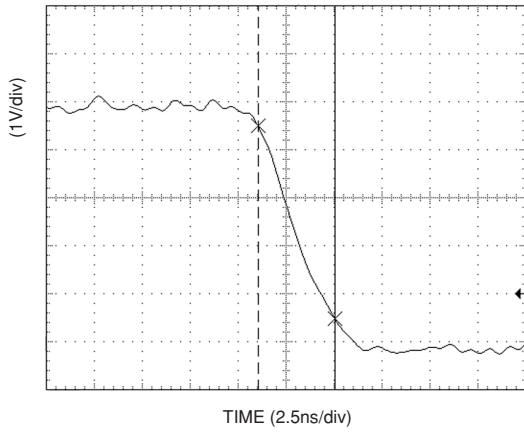
Status A or Status B = 0 if the output is open circuit, i.e., open LED.

After LOAD returns low, normal shift register operation resumes and status data is shifted out as new data words are shifted in on the rising edge of SHIFTCLOCK.

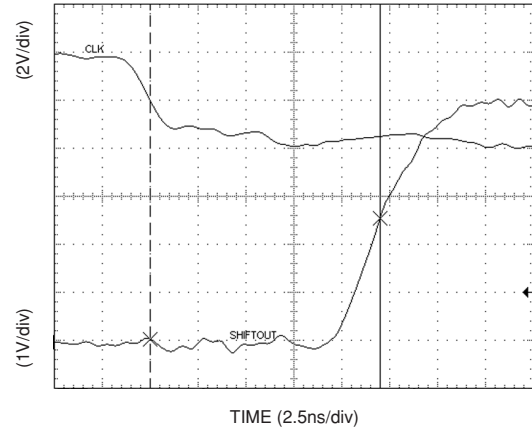
| Divisor Code | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9  | A  | B  | C  | D  | E  | F  |
|--------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|
| Divide by R  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

**Table 3. PWM Clock Ratio to Shift Clock [PWM Clock Freq. = (Shift Clock Freq)/R]**

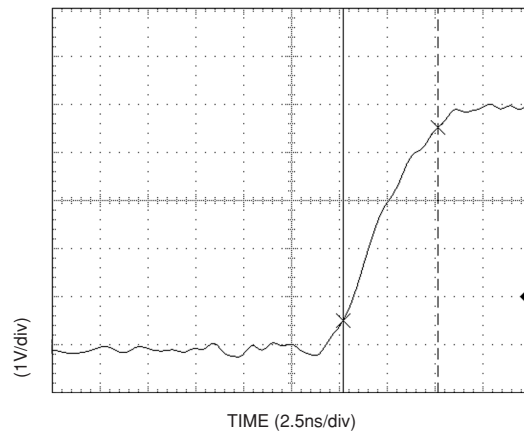




**Output Current Sink Rise Time**

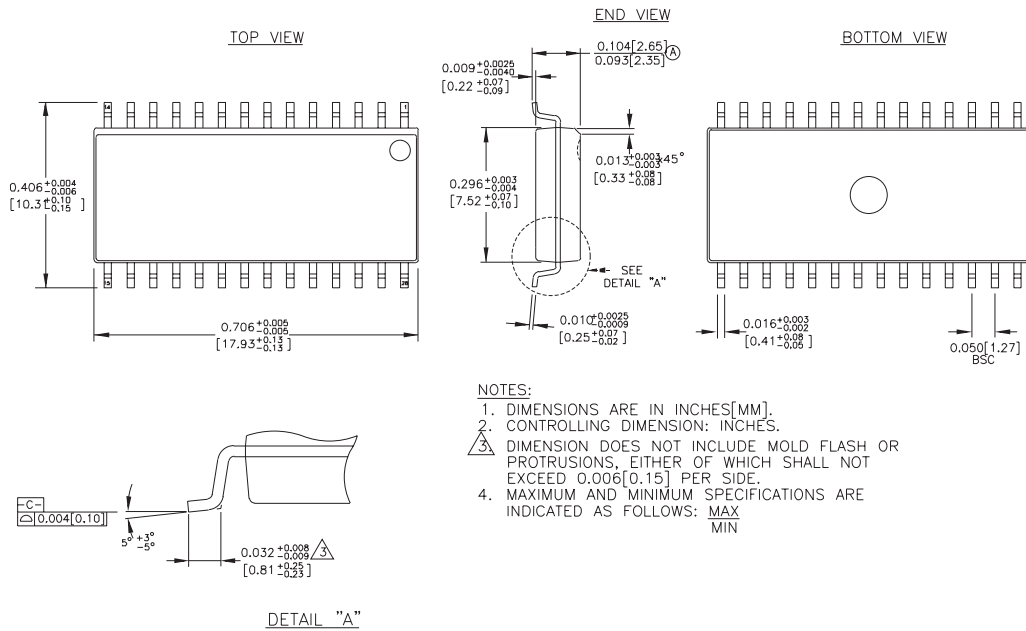


**Clock to Shiftout Delay Time**



**Output Current Sink Fall Time**

## Package Information



Rev. 02

## 28-Pin Wide SOIC

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