



SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

## ATP101 — P-Channel Silicon MOSFET General-Purpose Switching Device Applications

### Features

- Low ON-resistance
- Slim package
- Halogen free compliance
- Large current
- 4.5V drive
- Protection diode in

### Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	VDSS		-30	V
Gate-to-Source Voltage	VGSS		±20	V
Drain Current (DC)	ID		-25	A
Drain Current (PW≤10μs)	IDP	PW≤10μs, duty cycle≤1%	-75	A
Allowable Power Dissipation	PD	Tc=25°C	30	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		-55 to +150	°C
Avalanche Energy (Single Pulse) *1	EAS		25	mJ
Avalanche Current *2	I <sub>AV</sub>		-13	A

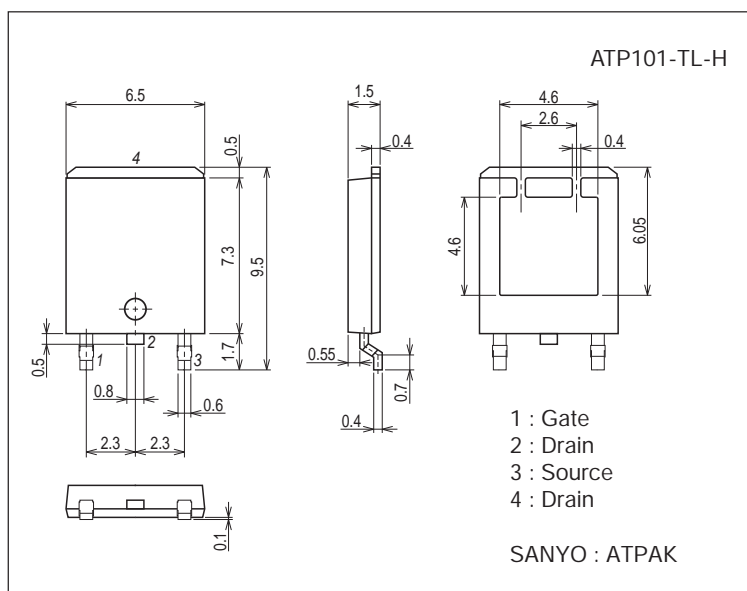
Note : \*1 VDD=-10V, L=200μH, I<sub>AV</sub>=-13A

\*2 L≤200μH, Single pulse

### Package Dimensions

unit : mm (typ)

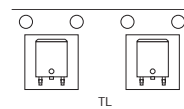
7057-001



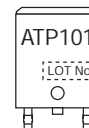
### Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

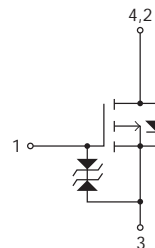
### Packing Type: TL



### Marking



### Electrical Connection

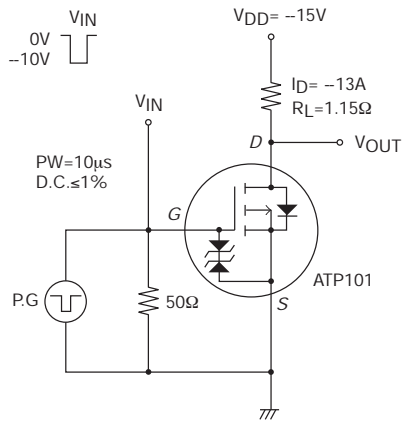


# ATP101

## Electrical Characteristics at Ta=25°C

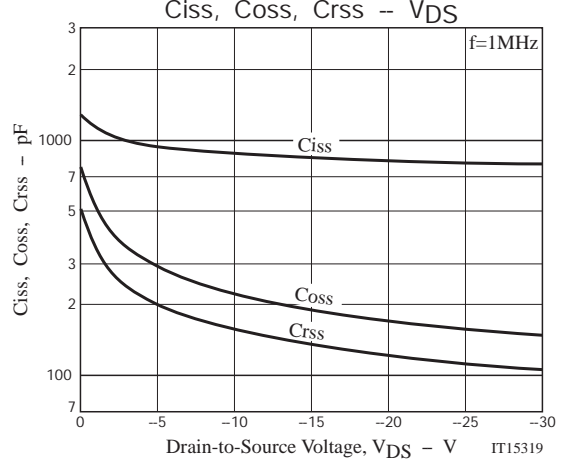
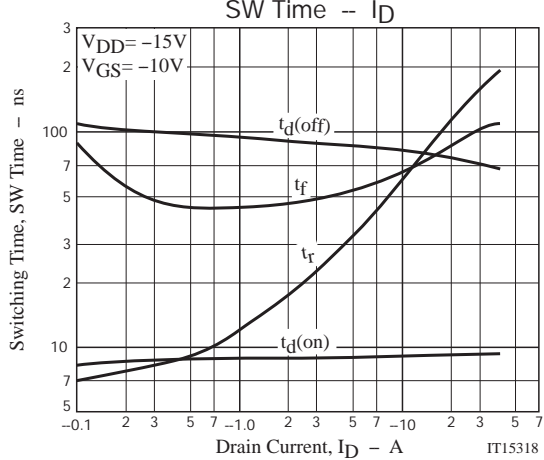
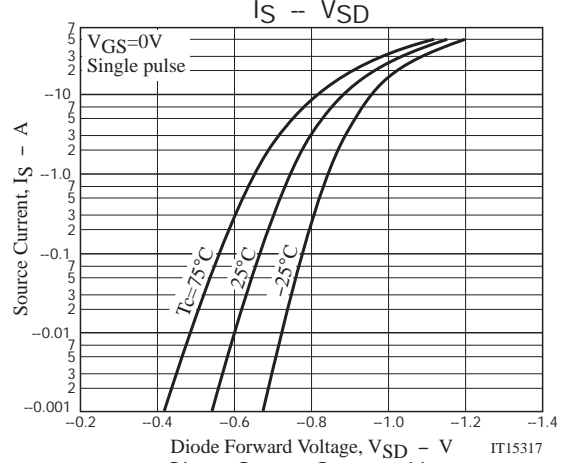
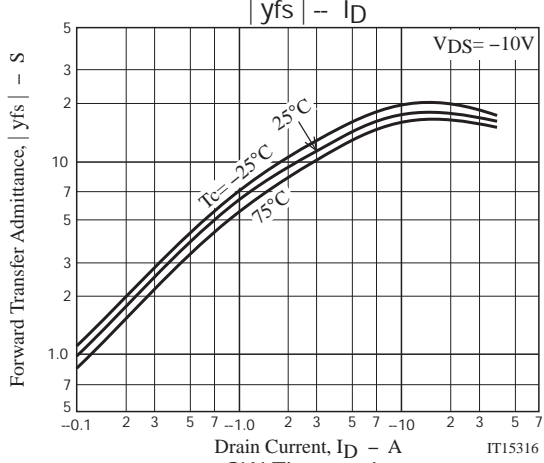
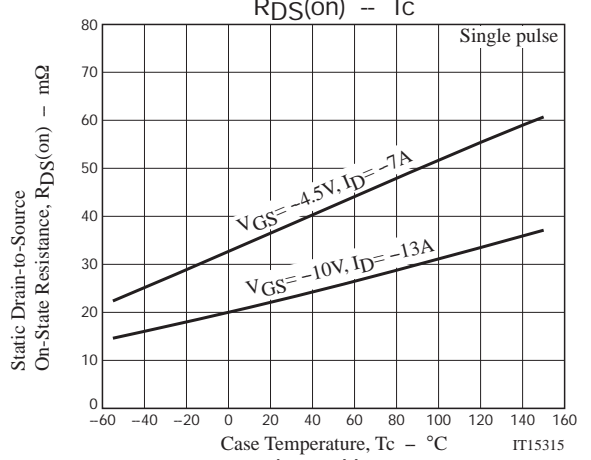
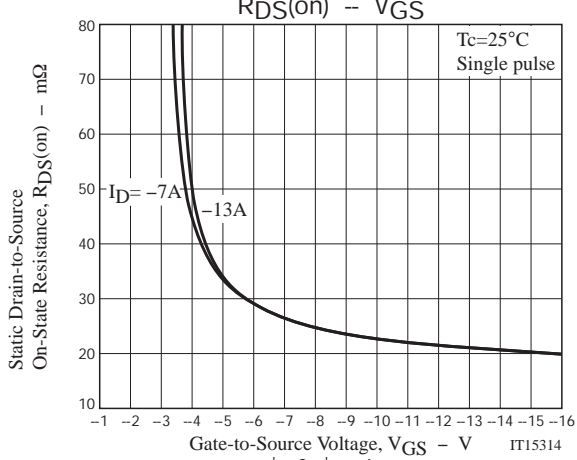
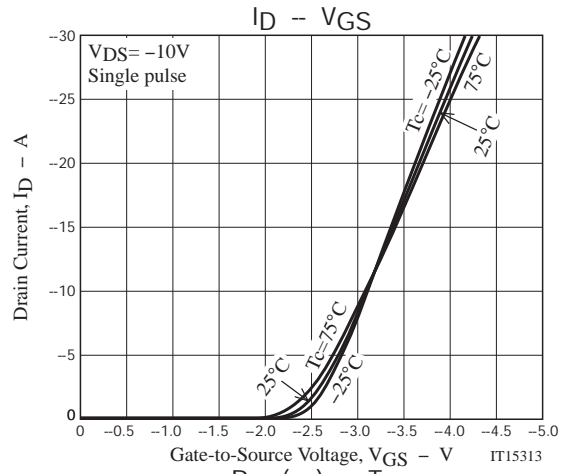
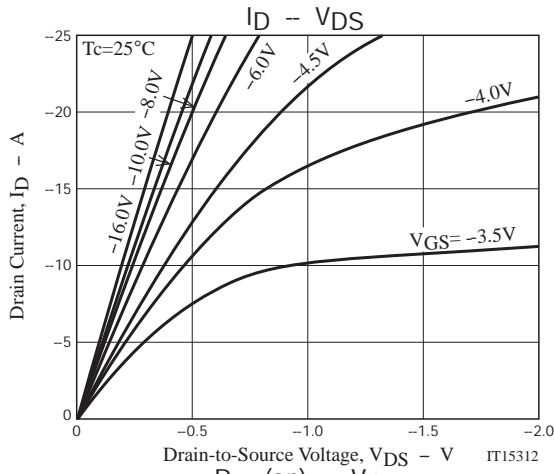
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -1\text{mA}, V_{GS} = 0\text{V}$	-30			V
Zero-Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 16\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{V}, I_D = -1\text{mA}$	-1.2		-2.6	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{V}, I_D = -13\text{A}$		17		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D = -13\text{A}, V_{GS} = -10\text{V}$		23	30	$\text{m}\Omega$
	$R_{DS(on)2}$	$I_D = -7\text{A}, V_{GS} = -4.5\text{V}$		36	51	$\text{m}\Omega$
Input Capacitance	Ciss	$V_{DS} = -10\text{V}, f = 1\text{MHz}$		875		pF
Output Capacitance	Coss			220		pF
Reverse Transfer Capacitance	Crss			155		pF
Turn-ON Delay Time	$t_{d(on)}$		See specified Test Circuit.		9.2	
Rise Time	$t_r$			70		ns
Turn-OFF Delay Time	$t_{d(off)}$			80		ns
Fall Time	$t_f$			70		ns
Total Gate Charge	Qg	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -25\text{A}$			18.5	
Gate-to-Source Charge	Qgs			3.2		nC
Gate-to-Drain "Miller" Charge	Qgd			4.0		nC
Diode Forward Voltage	$V_{SD}$	$I_S = -25\text{A}, V_{GS} = 0\text{V}$		-0.99	-1.5	V

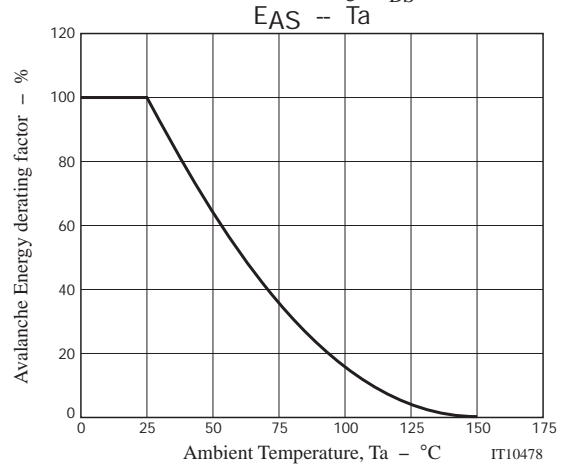
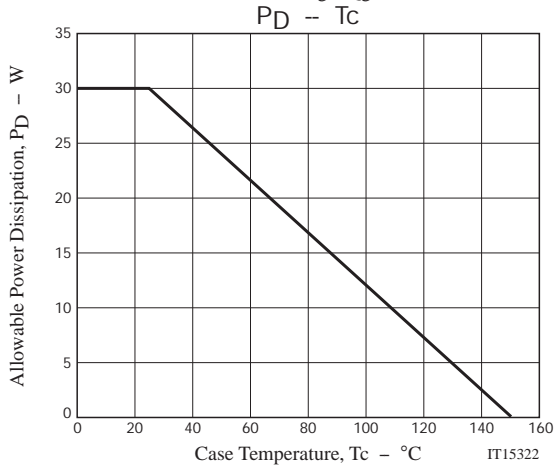
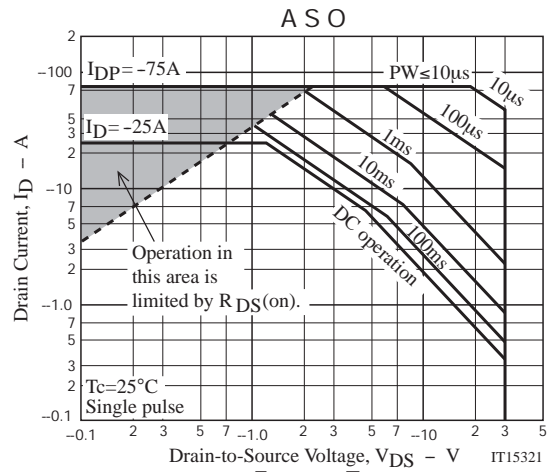
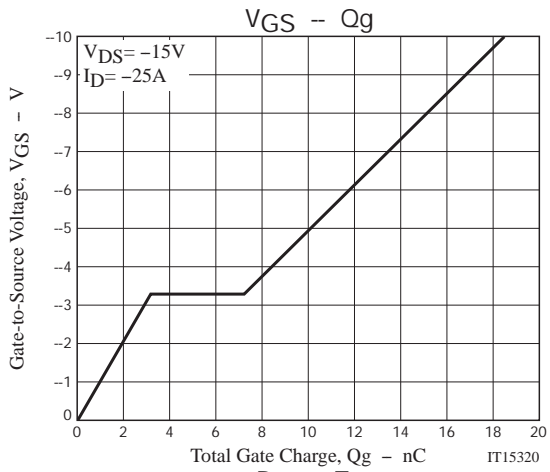
## Switching Time Test Circuit



## Ordering Information

Device	Package	Shipping	memo
ATP101-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free





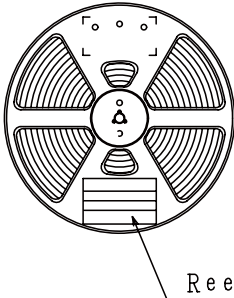
Taping Specification

ATP101-TL-H

1. Packing Format (TL)

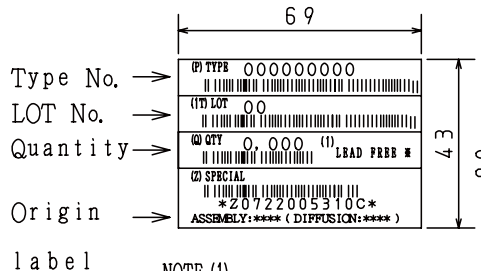
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

Packing method



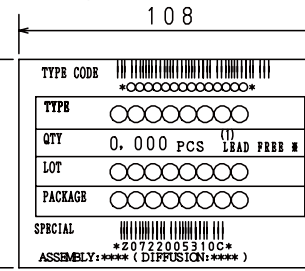
Reel label

Reel label, Inner box label  
(unit:mm)



Outer box label

It is a label at the time of factory shipments.  
The form of a label may change in physical distribution process.



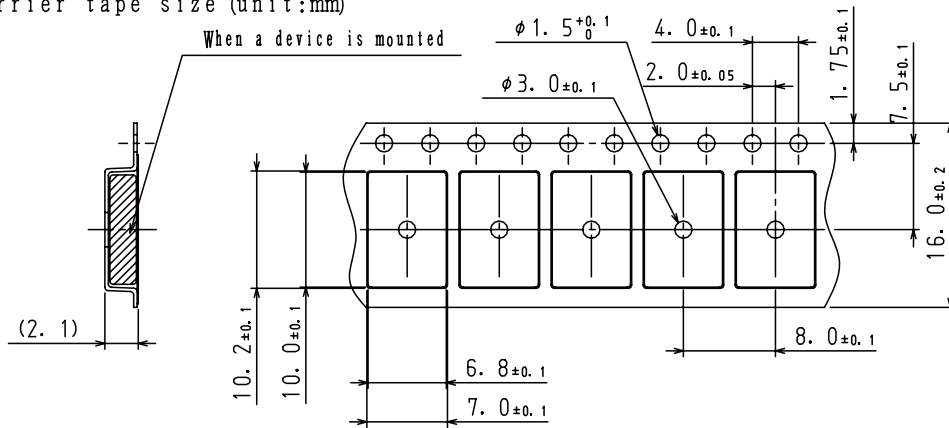
NOTE (1)

The LEAD FREE \* description shows that the surface treatment of the terminal is lead free.

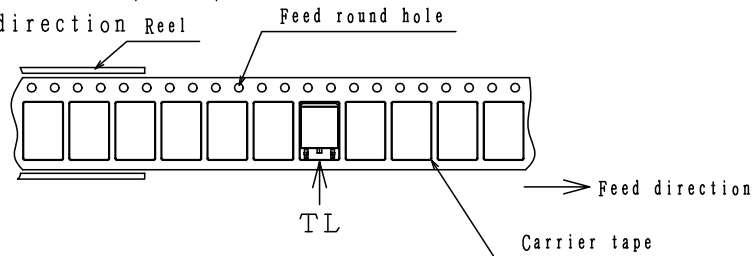
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel

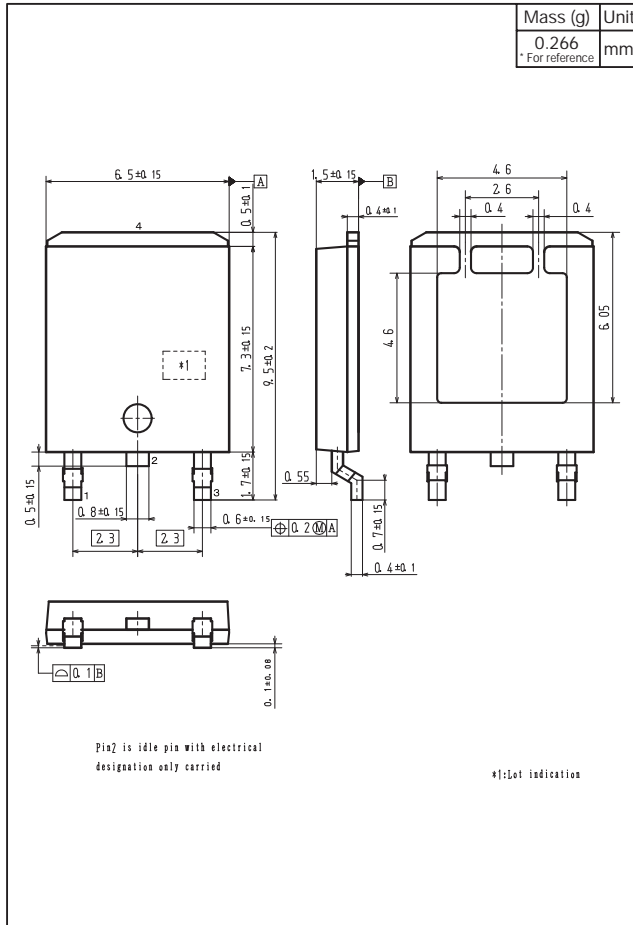


The one electrode terminals on feed hole side...TL

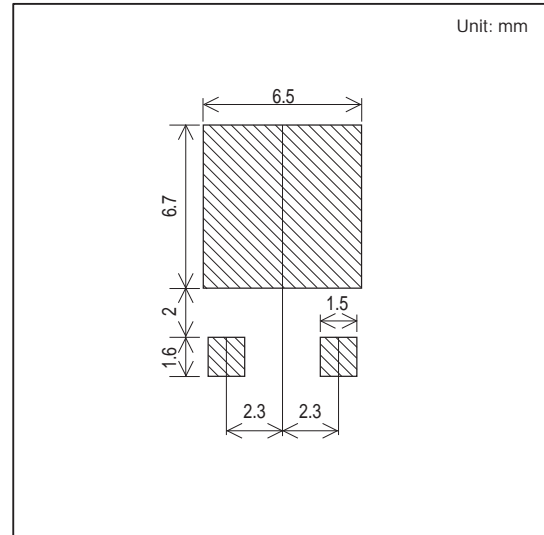
# ATP101

## Outline Drawing

ATP101-TL-H



## Land Pattern Example



Note on usage : Since the ATP101 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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