



SPN2054

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN2054 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as DC/DC converter and Desktop computer power management.

The package is universally preferred for commercial industrial surface mount applications

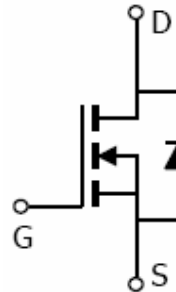
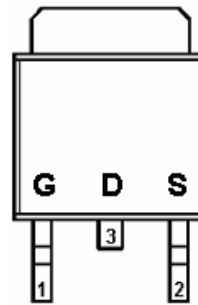
APPLICATIONS

- Power Management in Desktop Computer
- DC/DC Converter
- LCD Display inverter

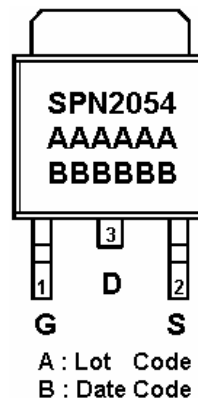
FEATURES

- ◆ 20V/12A, $R_{DS(ON)}=40m\Omega@V_{GS}=10V$
- ◆ 20V/ 7A, $R_{DS(ON)}=45m\Omega@V_{GS}=4.5V$
- ◆ 20V/ 4A, $R_{DS(ON)}=50m\Omega@V_{GS}=2.5V$
- ◆ 20V/ 2A, $R_{DS(ON)}=60m\Omega@V_{GS}=1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L package design

PIN CONFIGURATION(TO-252-2L)



PART MARKING





SPN2054

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2054T252RG	TO-252-2L	SPN2054

- ※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)
- ※ SPN2054T252RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	20	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	12	A
		T _A =70°C	8	
Pulsed Drain Current	I _{DM}	20	A	
Continuous Source Current(Diode Conduction)	I _S	12	A	
Power Dissipation	P _D	T _A =25°C	40	W
		T _A =70°C	20	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	105	°C/W	



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ELECTRICAL CHARACTERISTICS

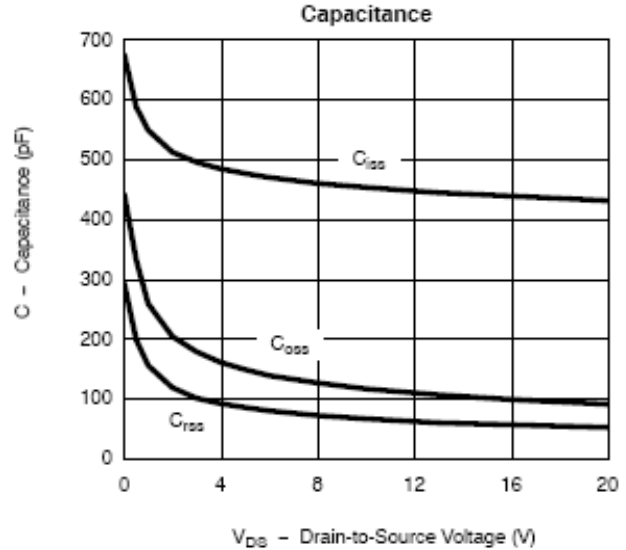
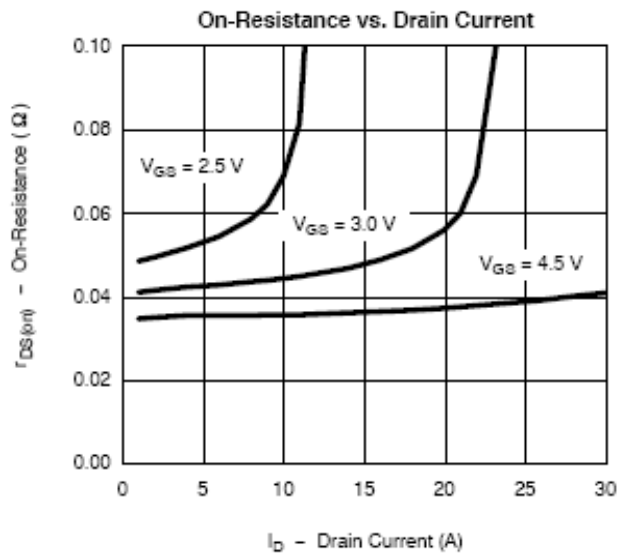
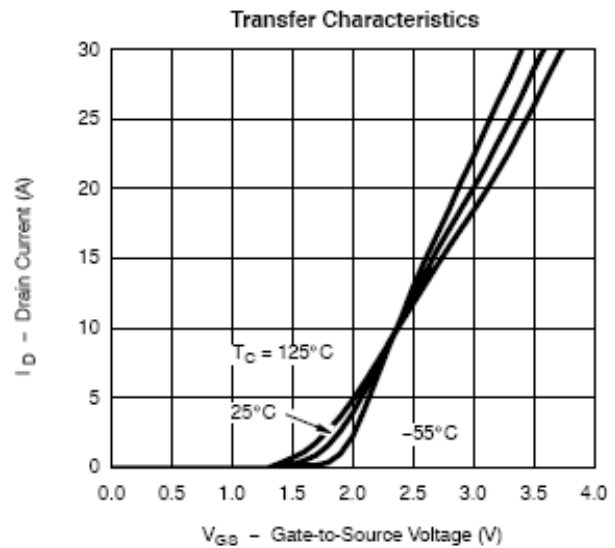
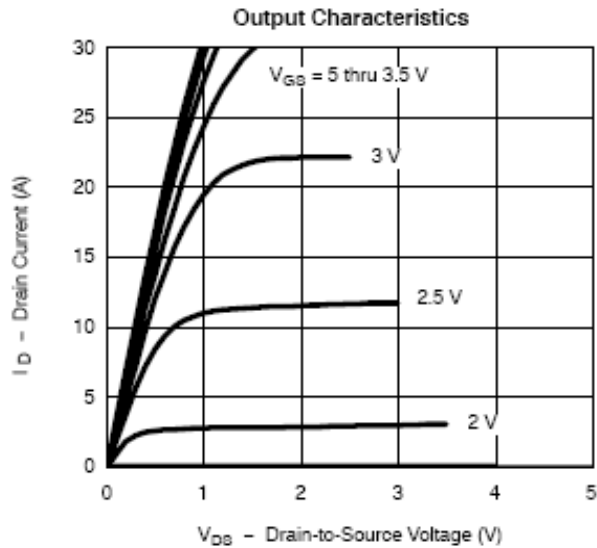
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.36		1.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=55^\circ C$			5	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$		0.031	0.040	Ω
		$V_{GS}=4.5V, I_D=7A$		0.035	0.045	
		$V_{GS}=2.5V, I_D=4A$		0.040	0.050	
		$V_{GS}=1.8V, I_D=2A$		0.048	0.060	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=-3.6A$		10		S
Diode Forward Voltage	V_{SD}	$I_S=7A, V_{GS}=0V$		0.95	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{GS}=4.5V$ $I_D=12A$		4.8	8	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V$ $f=1MHz$		485		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V, R_L=6\Omega$ $I_D=1.0A, V_{GEN}=4.5V$ $R_G=6\Omega$		8	14	ns
	t_r			12	18	
Turn-Off Time	$t_{d(off)}$			30	35	
	t_f			12	16	



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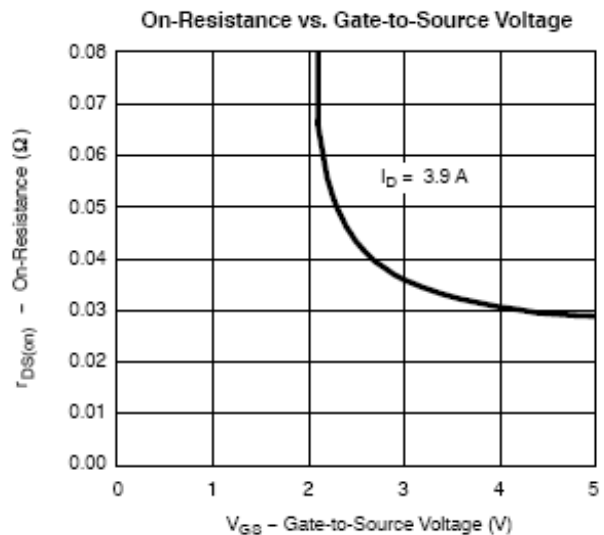
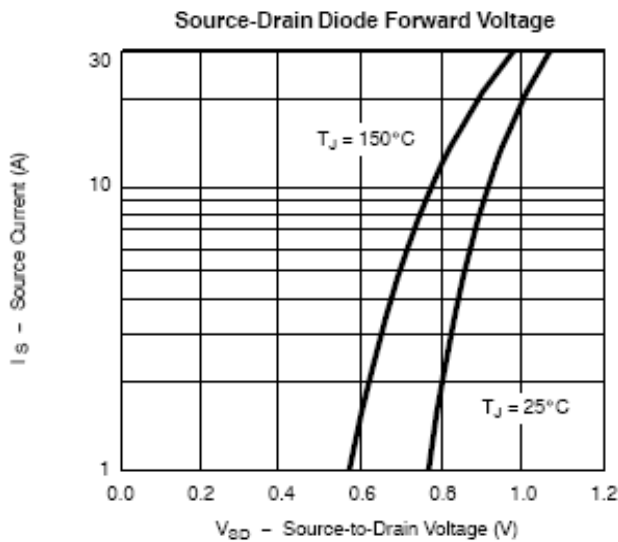
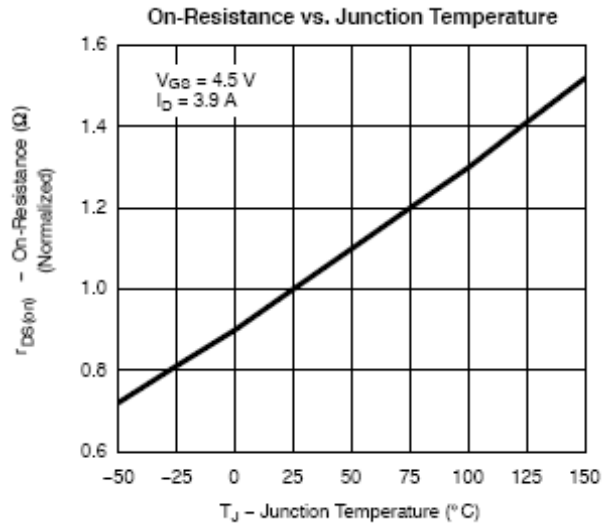
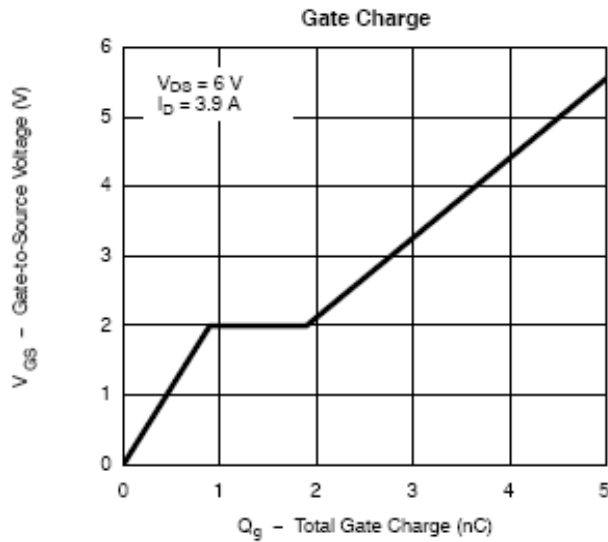
TYPICAL CHARACTERISTICS





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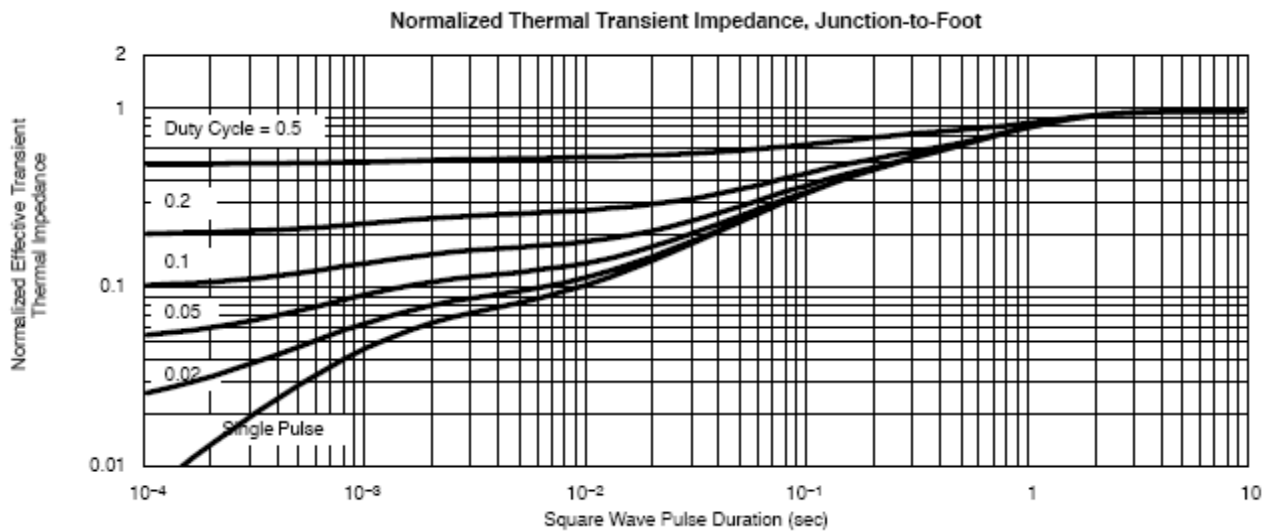
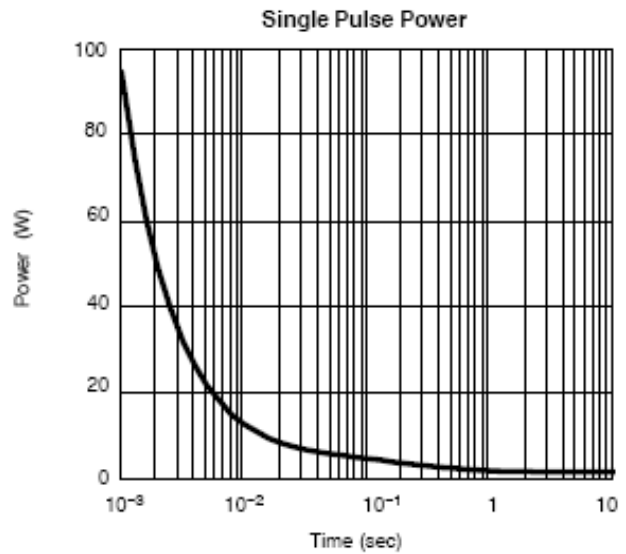
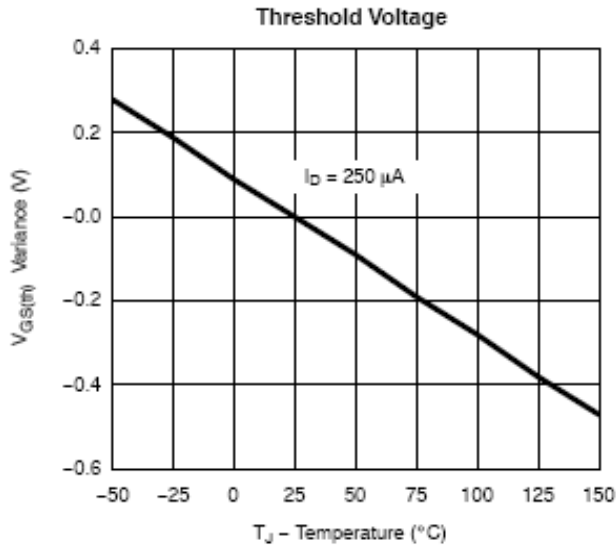
TYPICAL CHARACTERISTICS





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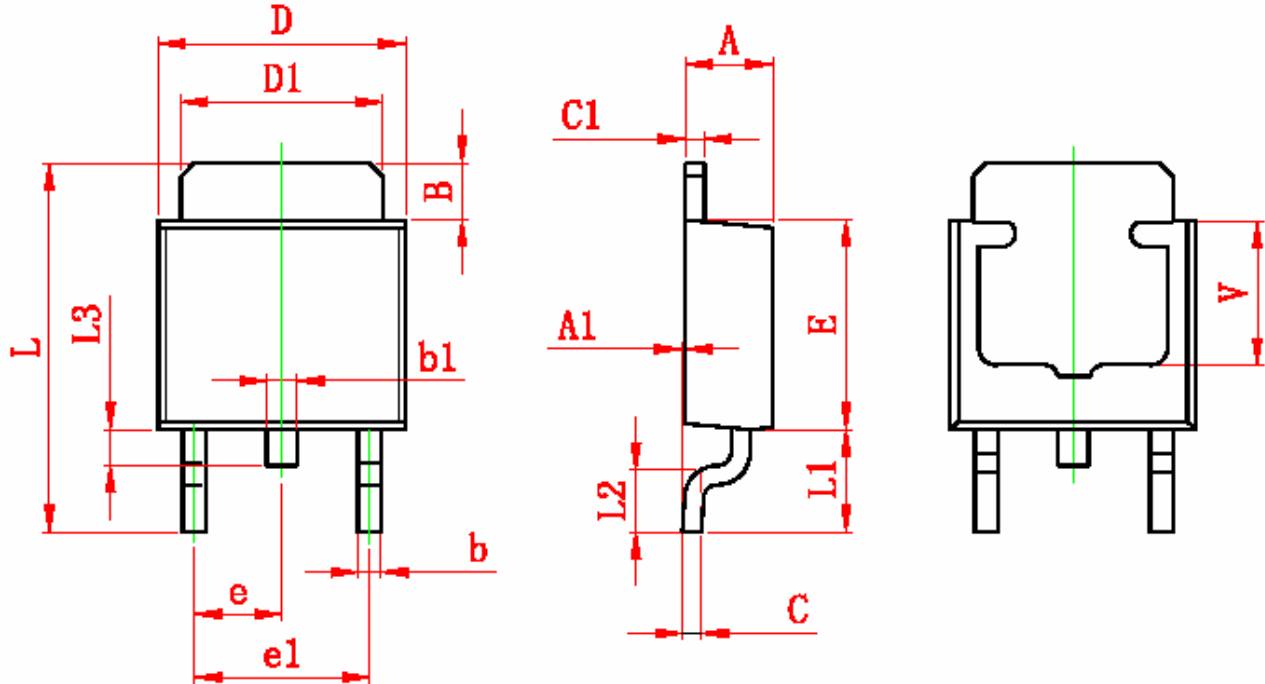
TYPICAL CHARACTERISTICS





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TO-252-2L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	



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