ZVS RESONANT CONTROLLER

FEATURES

- **Optimized for Off-Line and Battery Powered Operation**
- **Internal Zero-Voltage Detector**
- **Soft-Start**
- **Pulse-by-Pulse Current Limit**
- **Overdissipation Protection with Soft-Start**
- **Overvoltage Protection with Soft-Start**
- **Low-Current Standby mode**
- **Programmable On/Off Timing**
- **Enable Control**

APPLICATIONS

- **Cold Cathode Fluorescent Lamps**
- **Resonant Power Supplies**
- **Power Supplies for Notebook Computers**
- **Power Supplies for Personal Electronics**

DESCRIPTION

The TK75020 is a low-cost, high-performance Zero-Voltage Switching (ZVS) controller IC. The primary applications are in inverters for Cold Cathode Fluorescent Lamps (CCFL) and in ZVS quasi-resonant or multi-resonant converters. The combination of a unique (patent-pending) control concept and a ZVS resonant inverter generates low-distortion sine wave for the fluorescent lamp, leading to extended lamp life and high luminous efficiency. The IC features all necessary circuits of a controller for such applications, including externally adjustable timing parameters (frequency, $T_{on(min)}$, $T_{off(max)}$), current limit, Soft-Start, enable, error amplifier, and a trimmed reference. The same reference is used for undervoltage protection and other critical internal biases. Supply current in the "off" mode is kept at a minimum level (2 µA typical). Special care has been taken to avoid undesirable turn-on of the external power MOSFET when sufficient supply voltage is not available, or when the device is held in the off mode. Even with no V_{cc} applied, the drive pin of the IC will sink in excess of 20 mA while maintaining the voltage below 1 V to prevent that leakage currents turn on the power MOSFET. An internal zero-voltage detector monitors the voltage across the MOSFET and ensures that the turn-on will only take place under zero-voltage conditions. A unique overdissipation protection prevents the overheating of the power MOSFET in case the zero-voltage switching is lost.

The TK75020 is available in a 14-lead surface mount package.

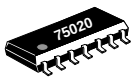
ORDERING INFORMATION

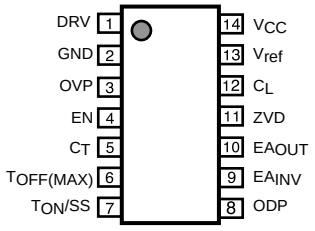
TK75020 □□

Tape/Reel Code

TAPE/REEL CODE
TL: Tape Left

TK75020





ABSOLUTE MAXIMUM RATINGS

All Pins Except T_{ON} / SS, $T_{OFF(MAX)}$, V_{REF}, C_T, ODP and EN (Low Impedance Source) ..... 16 V
T_{ON} / SS, $T_{OFF(MAX)}$, ref, C_T, ODP Pins ..... 6 V
EN Pin ..... 16 V
Power Dissipation (Note 1) ..... 500 mW

Maximum Current (V_{CC} and ZVD Pins) ..... 20 mA
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -20 to +85 °C
Junction Temperature ..... 150 °C
Lead Soldering Temperature (10 s) ..... 235 °C

TK75020 ELECTRICAL CHARACTERISTICS

Test conditions: V_{CC} = 12 V, V_{EN} = 2.4 V, C_T = 360 pF, $I_{TON\ /\ SS}$ = $I_{TOFF(MAX)}$ = 50 µA, DRV is Open, T_A = Full Operating Temperature Range, Typical numbers apply at T_A = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
$I_{CC(OFF)}$	Supply Current OFF	V_{EN} = 0 V			2	100	µA
$I_{CC(OFF,H)}$	Supply Current OFF, HIGH	V_{EN} = 0 V, V_{CC} = 16 V				2	mA
$I_{CC(UVLO)}$	Supply Current, UVLO Mode	V_{CC} = 5 V			700	1000	µA
$I_{CC(ON)}$	Supply Current ON	V_{CC} = 6 V			4.7	6	mA
		6 V < V_{CC} < 16 V				8	mA
$I_{CC(ON,DRV)}$	Supply Current ON, DRV	V_{CC} = 6 V, C_{DRV} = 1 nF			5.6	8	mA
		6 V < V_{CC} < 16 V				10	mA
$V_{CC(ON)}$	UVLO High Threshold			5.2	5.6	6.0	V
$V_{CC(OFF)}$	UVLO Low Threshold			5.0	5.3	5.6	V
$V_{CC(HYST)}$	UVLO Hysteresis			80		500	mV
ON/OFF SECTION (EN PIN)							
V_{EN}	Threshold Voltage	6 V < V_{CC} < 16 V		0.4		2.4	V
I_{EN}	Input Current	V_{EN} = 2.4 V			4		µA
		V_{EN} = 0 V, (Note 2)		-100			nA
REFERENCE SECTION (V_{REF} PIN)							
V_{ref}	Reference Output Voltage	I_{ref} = 0 mA	T_A = 25 ° C	3.8	4.0	4.2	V
			T_A = Full Range	3.7	4.0	4.3	V
$\lvert\Delta V_{ref(LOAD)}\rvert$	Load Regulation	-1 mA < I_{ref} < 0 mA			4.0		mV
$\lvert\Delta V_{ref(LINE)}\rvert$	Line Regulation	6 V < V_{CC} < 16 V			15		mV
$I_{ref(SC)}$	Short Circuit Current	V_{ref} = 0 V			-12		mA

Note 1: Power Dissipation is 500 mW when mounted as recommended. Derate at 4 mW/°C for operation above 25°C.
Note 2: Guaranteed by design.

TK75020 ELECTRICAL CHARACTERISTICS (CONT.)

Test conditions: V_{CC} = 12 V, V_{EN} = 2.4 V, C_T = 360 pF, $I_{TON\ /\ SS}$ = $I_{TOFF(MAX)}$ = 50 µA, DRV is Open, T_A = Full Operating Temperature Range, Typical numbers apply at T_A = 25 °C, unless otherwise specified.

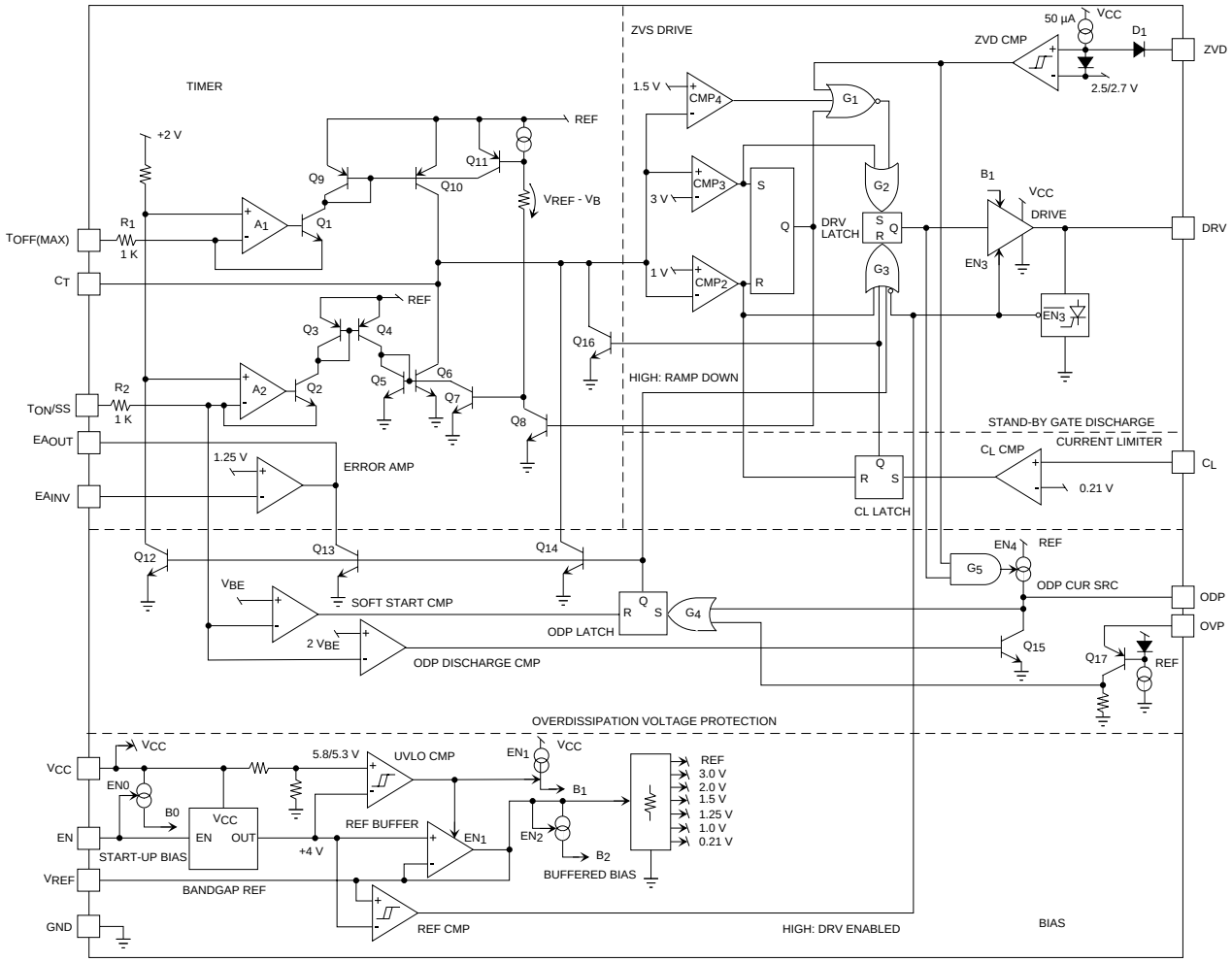
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DRIVE SECTION (DRV PIN)						
$V_{DRV(HIGH)}$	Output High Voltage	I_{DRV} = -20 mA	9.0	10.0		V
		I_{DRV} = -100 mA		9.8		V
$V_{DRV(LOW)}$	Output Low Voltage	I_{DRV} = 20 mA		0.3	0.6	V
		I_{DRV} = 200 mA		1.8	2.5	V
		I_{DRV} = 20 mA, V_{CC} = 0 V or V_{EN} = 0 V		0.9	1.3	V
$I_{DRV(SRC,PK)}$	Peak Source Current	C_{DRV} = 10 nF		500		mA
$I_{DRV(SINK,PK)}$	Peak Sink Current	C_{DRV} = 10 nF		700		mA
t_{RISE}	Rise Time	C_{DRV} = 1 nF		70	120	ns
t_{FALL}	Fall Time	C_{DRV} = 1 nF		25	75	ns
ERROR AMPLIFIER SECTION (EA_{INV} AND EA_{OUT} PINS)						
$V_{EA(ref)}$	Equivalent Internal Reference Voltage		1.19	1.26	1.30	V
$I_{EA(INV)}$	Bias Current			0.10		µA
$V_{EA(OUT,\ LOW)}$	Output Voltage LOW	$I_{EA(OUT)}$ = -1 mA, V_{INV} = 1.5 V		0.25		V
A_{OL}	Open Loop Gain	15 kΩ From EA_{OUT} to T_{ON} / SS		70		dB
GBW	Gain-Bandwidth Product	15 kΩ From EA_{OUT} to T_{ON} / SS, (Note 2)		2		MHz
PSSR	Power Supply Rejection Ratio	6 V ≤ V_{CC} ≤ 16 V		65		dB
CURRENT LIMIT SECTION (C_L PIN)						
I_{CL}	Bias Current	V_{CL} = 0 V		-0.2		µA
$V_{CL(TH)}$	Threshold Voltage		180	210	240	mV
$t_{CL(DRV)}$	Delay to DRV	V_{CL} Steps From 0 to 400 mV		150		ns
ON-TIME SETTING AND SOFT-START SECTION (T_{ON} / SS PIN)						
$I_{TON\ /\ SS\ (SC)}$	Short Circuit Current	$V_{TON\ /\ SS}$ = 0 V		-2.5		mA
$V_{TON\ /\ SS}$	Pin Voltage	$I_{TON\ /\ SS}$ = 0 mA	1.8	2.0	2.2	V
$V_{SS(TH)}$	Soft-Start Threshold		0.40	0.65	0.90	V
$V_{DCH(TH)}$	ODP Discharge Threshold		1.0	1.4	1.9	V

TK75020 ELECTRICAL CHARACTERISTICS (CONT.)

Test conditions: V_{CC} = 12 V, V_{EN} = 2.4 V, C_T = 360 pF, $I_{TON / SS}$ = $I_{TOFF(MAX)}$ = 50 µA, DRV is Open, T_A = Full Operating Temperature Range, Typical numbers apply at T_A = 25 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MAXIMUM OFF-TIME SETTING SECTION ($T_{OFF(MAX)}$ PIN)						
$I_{T(OFF, MAX)}$	Short Circuit Current	$V_{T(OFF, MAX)}$ = 0 V		2.5		mA
$V_{T(OFF, MAX)}$	Pin Voltage	$I_{T(OFF, MAX)}$ = 0 mA	1.8	2.0	2.2	V
TIMING SECTION (C_T PIN)						
$V_{CT(LOW)}$	Low Threshold Voltage		0.9	1.0	1.1	V
$V_{CT(HIGH)}$	High Threshold Voltage		2.7	3.0	3.3	V
f	Oscillator Frequency		115	140	165	kHz
CTR_{TON}	Current Transfer Ratio to C_T Pin, On-time Setting	V_{CT} = 4 V	-6.2	-5.5	-4.8	
$CTR_{TOFF(MAX)}$	Current Transfer Ratio to C_T Pin, Max Off-time Setting	V_{CT} = 0 V	4.75	5.25	5.75	
ZERO VOLTAGE DETECTOR SECTION (ZVD PIN)						
$V_{ZVD(TH)}$	Detector Low Threshold	T_A = 25 ° C	1.8	2.0	2.2	V
I_{ZVD}	Input Current	V_{ZVD} = 2 V	-50		0	µA
$t_{ZVD(DRV)}$	Delay to DRV	V_{ZVD} Steps From 5 to 0 V, C_{DRV} = 1 nF		170	300	ns
OVERDISSIPATION DETECTOR SECTION (ODP PIN)						
$V_{ODP(TH)}$	Detection Threshold Volage		0.45	0.70	0.95	V
$I_{ODP(AVG)}$	Average Current	f = 100 kHz, $T_{OVERLAP}$ = 200 ns		0.6		µA
OVERVOLTAGE DETECTOR SECTION (OVP PIN)						
$V_{OVP(TH)}$	Detection Threshold Volage		3.6	4.0	4.3	V
$t_{OVP(D)}$	Dealy to DRV			350	800	ns

BLOCK DIAGRAM



PIN DESCRIPTION

SUPPLY VOLTAGE PIN (V_{CC})

This pin is connected to the supply voltage. The IC begins normal operation when two conditions are met: 1) the V_{CC} voltage exceeds 5.6 V and 2) the voltage of the enable pin exceeds 2.2 V. Operation ceases and the IC goes into a UVLO mode when the V_{CC} voltage drops below 5.3 V. When the voltage at the enable pin becomes less than 0.4 V, the IC is turned off ("off" mode). In UVLO mode the current consumption is less than 300 μA, in off mode it is further reduced to below 3 μA. The operating voltage range is 6 V to 14 V. The tolerances of the start and stop voltages are 5.6 ± 0.4 V and 5.3 ± 0.3 V, respectively. During normal operation the total IC current consumption is less than 8 mA (no load, 100 kHz operation).

When V_{CC} is applied to the device with the enable pin pulled above 2.2 V ("on" mode), the following events will occur:

First, a trimmed bandgap reference voltage will be generated as soon as V_{CC} reaches about 4.8 V. This reference will be used to determine the UVLO thresholds. When V_{CC} reaches the upper threshold of the undervoltage lockout comparator, that comparator enables the reference buffer. When the voltage at the output of the buffer, i.e. on the V_{REF} pin, becomes higher than about 3.7 V, an enable signal is generated for the drive stage through gate G_3.

Normal operation may be interrupted at any time by pulling the enable pin below 0.4 V. When V_{CC} is reduced below the lower threshold of the undervoltage lockout, the internal 4 V bias is disabled and the drive output is quickly turned off. The bandgap reference remains active as long as V_{CC} is above 4.8 V. Special care has been taken to keep the drive output low even at a lower level of V_{CC} in order to prevent unwanted turn-on of the external MOSFET.

ENABLE (ON/OFF) PIN (EN)

The enable pin is used to enable or disable the IC. The IC is guaranteed to turn on (i.e., to enter the "on" mode) when the pin voltage is above 2.2 V and is guaranteed to turn off when the pin voltage is below 0.4 V. If the On/Off feature is not needed, the pin can be connected directly to the supply voltage. The enable pin is internally equivalent to a 200 kΩ resistor in series with two diodes.

GROUND PIN (GND)

This pin provides ground return connection for the IC.

DRIVE PIN (DRV)

This pin drives the external MOSFET. During standby, the DRV pin provides at least 20 mA current sinking capability with less than 1 V difference between the ground and the DRV pin. The internal circuitry connected to the DRV pin is designed to deliver a peak output voltage of 4 V above ground when the device operates at a minimum supply voltage of 6 V. An internal clamp circuit, however, ensures that the peak output voltage will never exceed 13 V. The DRV pin goes high only if the following five conditions are met simultaneously: 1) the drive (DRV) latch is set, 2) the overdissipation protection latch (ODP) is reset, 3) the current limit latch (C_L) is reset, 4) the enable pin is pulled high, and 5) the output of the reference comparator is high, i.e., it detects that the voltage at the V_{ref} pin is sufficiently high.

CURRENT LIMIT PIN (C_L)

The C_L pin is used for high-speed, cycle-by-cycle overload protection. When the voltage of the C_L pin exceeds 0.2 V above ground, the current limit latch is set by the C_L comparator and the output stage is forced low. At the same time, the timing capacitor is quickly discharged with transistor Q_{16}. Note that a quick discharge is necessary in order to reduce the "on" time (and the duty ratio) without a significant increase in the effective "off" time. The current limit latch is reset when the output of the drive latch goes low, i.e., when the off time is over and the output of the C_L comparator goes high.

REFERENCE PIN (V_{ref})

The bandgap reference, an internal 4 V source, is buffered by a reference buffer, whose output is connected to the V_{ref} pin. The V_{ref} pin voltage is enabled to develop when the upper threshold of the UVLO comparator is passed by V_{CC}.

TIMING CAPACITOR PIN (C_T)

The external timing capacitor is connected to the C_T pin. The voltage across the timing capacitor oscillates between an upper level of 3 V and a lower level of 1 V. During the time the voltage of the timing capacitor is rising (due to the charging current set by the resistor between ground and the $T_{OFF(MAX)}$ pin), the drive latch is in the reset state and

PIN DESCRIPTION (CONT.)

the DRV pin is held low. The drive latch may be set either by the output of comparator CMP_3 through the two-input OR gate G_2 or by the ZVD comparator through G_1 and G_2. CMP_3 detects if the timing voltage reached 3 V, the ZVD comparator detects if the voltage at the ZVD pin dropped below 2 V. Note that gate G_1 allows setting the drive latch through the ZVD pin only when the voltage at the C_T pin is higher than 1.5 V and the current limit latch is in the reset state. The reason for disabling the ZVD path at C_T pin voltages lower than 1.5 V is to prevent an immediate turn-on of the MOSFET after it was turned off. CMP_4 is used to detect if the C_T pin voltage is higher than 1.5 V.

When the voltage of the timing capacitor is falling (due to the discharging current set by the external resistors between the output of the error amplifier and the T_{ON}/SS pin, as well as between the T_{ON}/SS pin and ground), the DRV pin is allowed to go high. The charge and discharge currents are enabled exclusively.

ZERO VOLTAGE DETECTION PIN (ZVD)

This pin is connected to the drain of the power MOSFET switch of the converter or inverter through a high value resistor or a diode. When the MOSFET is turned off, the drain voltage increases at first and then decreases, due to the resonant action in the loading network of the switch. When the drain voltage is above the supply voltage of the IC, the ZVD pin voltage is clamped to the supply voltage through the internal diode D_1. As the drain voltage drops below the supply voltage, the voltage of the ZVD pin begins to follow it. When the ZVD pin voltage drops below 2 V, the output of the ZVD comparator goes high and sets the drive latch through gates G_1 and G_2. Unless there is a fault condition, the DRV pin goes high and turns on the MOSFET switch. By having the ZVD feature, the circuit automatically sets the optimum off time, essentially independently from the value of the resistor between the $T_{OFF(MAX)}$ pin and ground.

ERROR AMPLIFIER PIN (EA_{OUT})

The EA_{OUT} pin is the output of the internal error amplifier. The output stage of the amplifier is an open-collector transistor. It is normally connected to the T_{ON}/SS pin via an external resistor. The non-inverting input of the error amplifier is internally tied to a trimmed 1.25 V reference. The error amplifier is short-circuit protected.

ERROR AMPLIFIER INPUT PIN (EA_{INV})

The EA_{INV} pin (the inverting input of the error amplifier) serves for receiving either an external voltage-feedback or an external current-feedback signal. The compensating network of the feedback loop is usually connected between the EA_{INV} and the EA_{OUT} pins.

TURN-ON TIMING / SOFT-START PIN (T_{ON} / SS)

The on-time is inversely proportional to the current flowing in the resistor connected between this pin and the EA_{OUT} pin. The T_{ON}/SS pin is also useful for providing Soft-Start at turn-on. Soft-Start can be achieved by connecting the series combination of a resistor and capacitor between the T_{ON}/SS pin and ground. When the normal operation of the IC is enabled (either because the V_{CC} voltage exceeds the upper UVLO threshold or because the IC is turned on by the Enable pin), the Soft-Start capacitor, which was initially discharged, begins to charge up through the series resistor. The charging current adds to the current flowing in the on-time-setting resistor and sets a shorter on time. As the voltage builds up across the soft-start capacitor the charging current gradually decreases and the on time gradually increases.

At normal operation a voltage-to-current converter formed by A_2 and Q_2 keeps the voltage of the T_{ON}/SS pin at 2 V. The current flowing through R_2 and the external resistor connected to the T_{ON}/SS pin and ground is mirrored with Q_3 and Q_4 into a second mirror formed by Q_5 and Q_6. The diode-connected section of the second mirror is shorted with the transistor Q_7 via Q_8 when the current switch latch is reset.

MAXIMUM TURNOFF TIMING PIN ($T_{OFF(MAX)}$)

An external resistor connected between this pin and ground sets the current that charges the timing capacitor. The maximum possible off time is inversely proportional to the value of that current. As discussed previously, when the off period is terminated by the zero-voltage detector, the actual off time becomes shorter than the value set by this resistor.

At normal operation the voltage of the $T_{OFF\,(MAX)}$ pin is kept at 2 V with the help of a voltage-to-current converter formed by the amplifier A_1 and transistor Q_1. The current flowing through the off time setting resistor and R_1 is

PIN DESCRIPTION (CONT.)

mirrored by the transistors Q_9 and Q_{10} and it charges the timing capacitor. The incoming mirror current is diverted from the mirror with transistor Q_{11} when the drive latch is set.

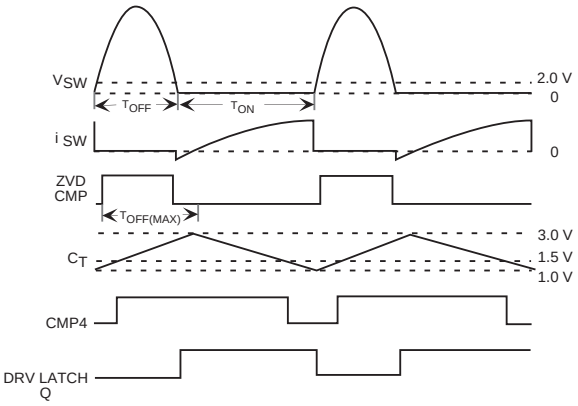
OVERDISSIPATION PROTECTION PIN (ODP)

The ODP pin is used to realize a protection against overdissipation of the power MOSFET due to the loss or absence of zero-voltage switching (ZVS). (ZVS can be lost if the load or the input voltage changes too much. ZVS is absent if the component values of the load network are far from optimal, or if the ZVD function is not implemented and the set off time is either too short or too long.) If ZVS is not present in a converter or inverter that was originally meant to operate with it, the MOSFET is turned on with a substantial voltage across it and the capacitor in parallel with it. Due to the periodic discharge of the parallel capacitor, a significant dissipation appears in the MOSFET. That dissipation is proportional to the switching frequency, the capacitance value, and the square of the voltage across the MOSFET at the instant of turn-on. The overdissipation protection works as follows: a current source is enabled when the MOSFET drain voltage is above the ZVD comparator threshold when the DRV pin voltage goes high. A short current pulse flows into the parallel combination of a resistor and capacitor connected between the ODP pin and ground and gradually begins to raise the pin voltage. When the pin voltage reaches about 0.7 V, the ODP latch is set via gate G_4. The output signal of the ODP latch inhibits gate G_3 and forces the drive output low. The output of the ODP latch also turns on transistors Q_{12}-Q_{14}. Q_{12} removes the 2 V reference signal from the non-inverting input of amplifiers A_1 and A_2 . Q_{13} pulls down the EA_{OUT} pin. The Soft-Start capacitor connected to the T_{ON}/SS pin begins to discharge through the soft-start resistor (see application circuit) and the on-time setting resistor. When the voltage at the T_{ON}/SS pin drops below 2 V_{BE}, the ODP discharge comparator turns on Q_{15}, which pulls down the ODP pin voltage and discharges the capacitor connected to that pin. When the voltage at the T_{ON}/SS pin drops below a V_{BE}, voltage the Soft-Start comparator resets the ODP latch. At that time the 2 V reference is enabled and a new Soft-Start cycle begins. The turnoff/soft restart cycle repeats until zero-voltage switching is reestablished.

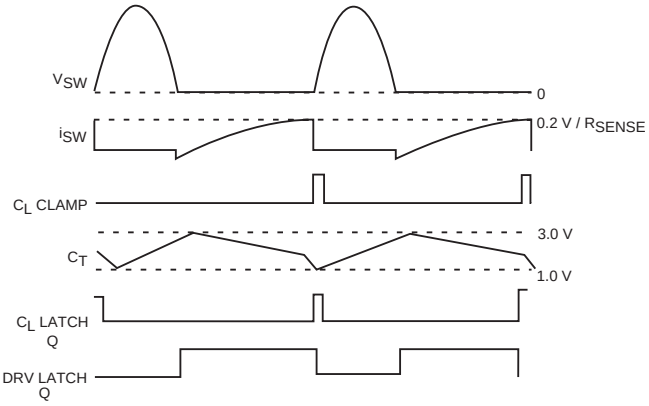
OVERVOLTAGE PROTECTION PIN (OVP)

The OVP pin is used to monitor the voltage across a winding of the transformer in the CCFL inverter. When the OVP comparator detects an overvoltage, it initiates a shutdown via G_4 and a Soft-Start cycle begins.

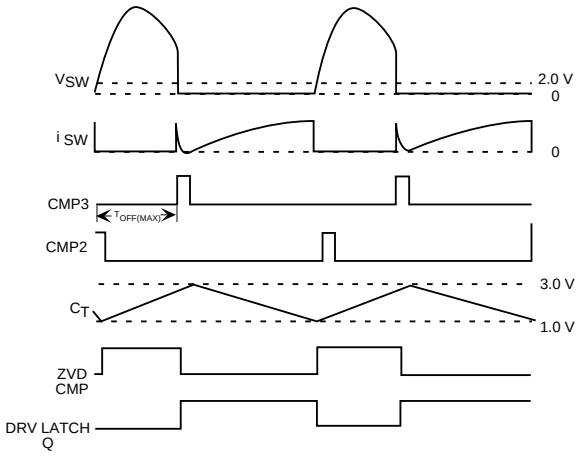
APPLICATION INFORMATION



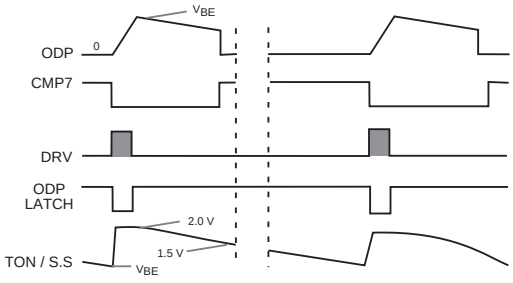
NORMAL OPERATION



CYCLE-BY-CYCLE CURRENT LIMIT

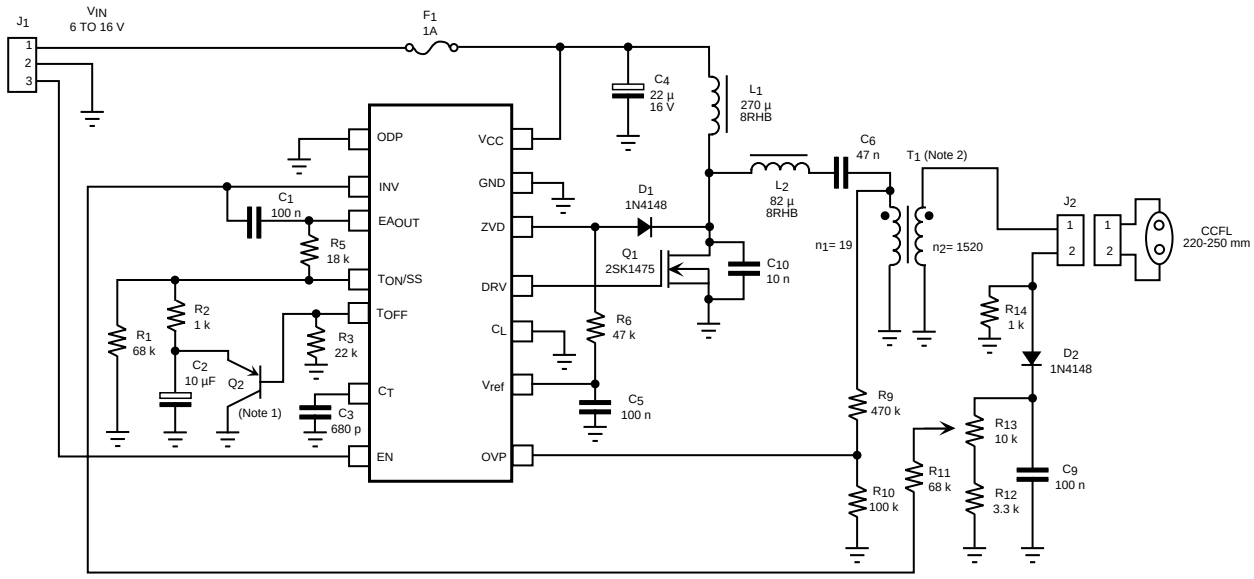


OPERATION WITHOUT ZVD



OVERDISSIPATION PROTECTION

APPLICATION INFORMATION (CONT.)

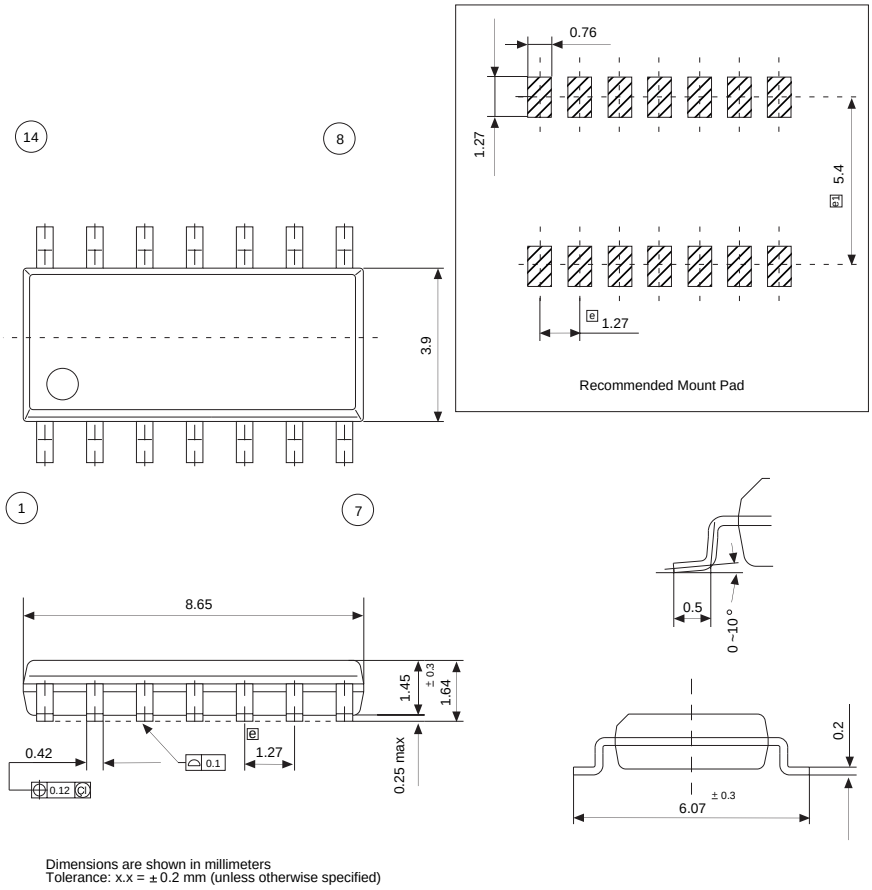


Gen. Note: Q_2 is not required if Q_1 is an avalanche rated FET
Gen. Note: Part #CTX01-13154 (Call Toko Technical Support (719) 528-2200).

LAPTOP DISPLAY BACKLIGHTING EXAMPLE

PACKAGE OUTLINE

SOP-14



Dimensions are shown in millimeters
Tolerance: x.x = ± 0.2 mm (unless otherwise specified)

Marking Information

	Marking
TK75020	75020

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