Real Time Clock with I2C or SPI, Crystal Temperature Compensation, Battery Switchover and Trickle Charger

Description

The EM3027 is an Ultra Low Power CMOS real-time clock IC with two serial interface modes: I2C or SPI. The interface mode is selected by the chip version.

The basic clock is obtained from the 32.768 kHz crystal oscillator. A thermal compensation of the frequency is based on the temperature measurement and calculation of the correction value. The temperature can be measured internally or be input by an external application to the register.

The chip provides clock and calendar information in BCD format with alarm possibility. The actual contents are latched at the beginning of a read transmission and afterwards data are read without clock counter data corruption.

An integrated 16-bit timer can run in Zero-Stop or Auto-Reload mode.

An interrupt request signal can be provided through INT/IRQ pin generated from Alarm, Timer, Voltage detector and Digital Self-Recovery system.

An integrated Trickle Charger allows recharging Backup Supply V_{Back} from the Main Supply Voltage V_{CC} through internal resistor(s). The internal device supply will switchover to V_{CC} when V_{CC} is higher than V_{Back} and vice versa.

The device operates over a wide 1.3 to 5.5V supply range and requires only 900 nA at 5V. It's possible to detect internally two supply voltage levels.

Applications

- Utility meters
- Battery operated and portable equipment
- Consumer electronics
- White/brown goods
- Pay phones
- Cash registers
- Personal computers
- Programmable controller systems
- Automotive systems
- Data loggers

Features

- Fully operational from 1.8 to 5.5V
- Supply current typically 600 nA at 1.3V
- Thermal compensated crystal frequency
- Oscillator stability 0.3 ppm / Volt
- Counter for seconds, minutes, hours, day of week, date months, years in BCD format and alarm
- Leap year compensation
- 16-bits Timer included
- Two Low Voltage Detection Levels V_{Low1}, V_{Low2}
- Automatic Supply switchover
- Serial communication via I2C or SPI
- Thermometer readable by the host
- Trickle Charger to preserve Battery Discharge and Data Integrity
- Integrated oscillator capacitors
- One EEPROM and 8 RAM data bytes for Application
- Digital Self-Recovery system
- No busy states and no risk of corrupted data while accessing
- One hour periodical registers refresh
- Support for standard UL1642 for Lithium Batteries
- Standard Temperature Range: -40°C to +85°C
- Extended Temperature Range: -40°C to +125°C
- Packages: TSSOP8, TSSOP14, SO8.

Block Diagram

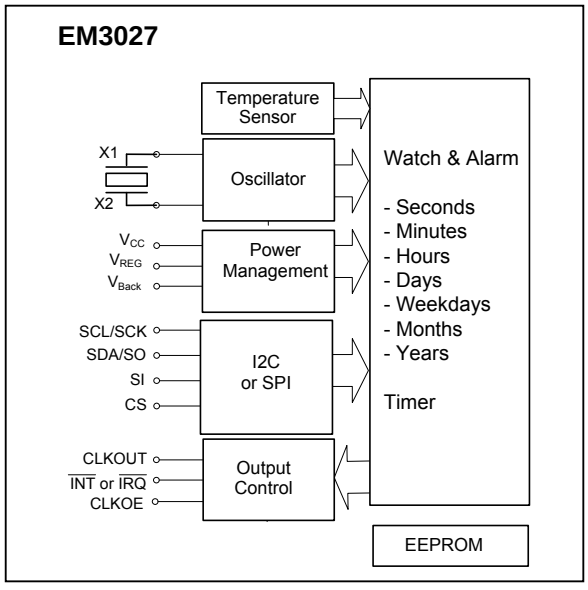
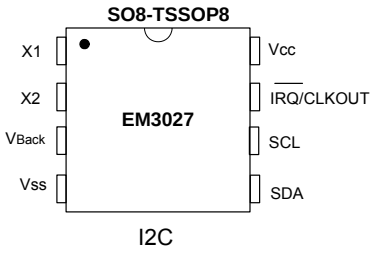


Table of contents

Table of contents 2
1 Packages / Pin Out Configuration 3
2 Absolute Maximum Ratings 4
2.1 Handling Procedures 4
2.2 Operating Conditions 4
2.3 Crystal characteristics 4
2.4 EEPROM Characteristics 4
3 Electrical Characteristics 4
4 EM 3027 Block Diagram and Application Schematic 6
4.1 Block Diagram 6
4.2 Application Schematic 6
4.3 Crystal Thermal Behaviour 7
4.4 Crystal Calibration 8
5 Memory Mapping 9
6 Definitions of terms in the memory mapping 10
7 Serial communication 12
7.1 How to perform READ/WRITE through I2C 12
7.2 How to perform READ/WRITE through SPI 13
8 Functional Description 15
8.1 Start after power-up 15
8.2 Normal Mode functionality 15
8.3 Watch and Alarm functionality 15
8.4 Timer function 15
8.5 Temperature sensor 16
8.6 Temperature compensation 16
8.7 EEPROM memory 16
8.8 RAM User Memory 17
8.9 Status Register 18
8.10 Interrupts 18
8.11 Self-Recovery System 18
8.12 Register Map 18
8.13 Xtal Oscillator and Prescaler 18
9 Power Management 19
9.1 Power Supplies, Switchover and Trickle Charge 19
9.2 Low Supply Detection 20
10 AC Characteristics 21
10.1 AC characteristics – I2C 21
10.2 AC characteristics – SPI 23
11 Using EM3027 with disturbed Supply Voltage on V_{CC} 25
12 Package Information 26
12.1 TSSOP-08/14 26
12.2 SO-8 26
13 Ordering Information 27

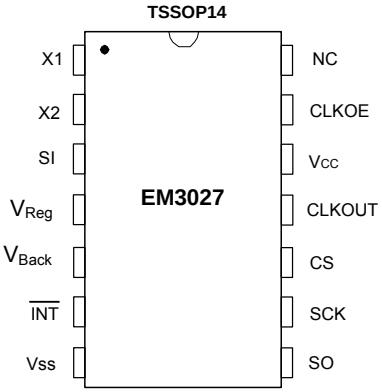
1 Packages / Pin Out Configuration



I2C

Pin	Name	Function
1	X1	32.768 kHz crystal input
2	X2	32.768 kHz crystal output
3	V_{Back}	Backup Supply Voltage
4	V_{SS}	Ground Supply
5	SDA	Serial Data
6	SCL	Serial Clock
7	$\overline{IRQ}$/CLKOUT	Interrupt Request /Clock Output
8	V_{CC}	Positive Supply

Table 1



SPI

Pin	Name	Function
1	X1	32.768 kHz crystal input
2	X2	32.768 kHz crystal output
3	SI	Serial Data Input for SPI transfer
4	V_{Reg}	Regulated Voltage – Reserved for test purpose only (This output is left unconnected)
5	V_{Back}	Backup Supply Voltage
6	$\overline{INT}$	Interrupt Request (Open Drain active low)
7	V_{SS}	Ground Supply
8	SO	Serial Data Output for SPI transfer
9	SCK	Serial Clock for SPI transfer
10	CS	Chip select input for SPI
11	CLKOUT	Clock Output
12	V_{CC}	Main Supply Voltage
13	CLKOE	Clock Output Enable CLKOE = '0' CLKOUT is disabled, CLKOUT is low CLKOE = '1' CLKOUT is enabled, CLKOUT is output
14	NC	Not Connected

Table 2

2 Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{CC}	V_{CCmax}	V_{SS} + 6.0V
Minimun voltage at V_{CC}	V_{CCmin}	V_{SS} – 0.3V
Maximum voltage at any signal pin	V_{max}	V_{CC} + 0.3V
Minimum voltage at any signal pin	V_{min}	V_{SS} – 0.3V
Maximum storage temperature	T_{STOmax}	+150°C
Minimum storage temperature	T_{STOmin}	-65°C
Electrostatic discharge maximum to MIL-STD-883C method 3015.7 with ref. to V_{SS}	V_{Smax}	2000V

Table 3

Stresses above these listed maximum ratings may cause permanent damages to the device.

Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

2.1 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

2.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temp.	T_A	-40		+125	°C
Supply voltage (Note 1)	V_{CC}, V_{Back}	1.3	5.0	5.5	V
Capacitor at V_{CC}, V_{Back}	C_D		100		nF

Table 4

Note 1: Refer to paragraphs 9.1 and 9.2

2.3 Crystal characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Frequency	f		32.768		kHz
Load capacitance	C_L	7	8.2	12.5	pF
Series resistance	R_S		70	110	kΩ

Table 5

Crystal Reference : Micro Crystal CC5V-T1A
web: www.microcrystal.com

2.4 EEPROM Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Read voltage	V_{Read}	1.4			V
Programming Voltage	V_{Prog}	2.2			V
EEPROM Programming Time	T_{Prog}			30	ms
Write/Erase Cycling			5000		cycles

Table 6

3 Electrical Characteristics

Parameter	Symbol	Test Conditions	V_{CC}	Temp. °C	Min	Typ	Max	Unit
Total supply current with Crystal	I_{CC}	All outputs open, Rs < 70 kΩ, V_{Back} = 0V I2C: SDA, SCL at V_{CC}, Clk/Int='0' SPI: All inputs at V_{SS}	1.3	-40 to 85		0.6	1.5	µA
				-40 to 125			4.6	
			3.3	-40 to 85		0.8	2.0	
				-40 to 125			5.2	
			5.0	-40 to 85		0.9	2.2	
				-40 to 125			5.5	
Total supply current with Crystal	I_{Back}	All outputs open, Rs < 70 kΩ, V_{CC} = 0V I2C: SDA, SCL at V_{Back}, Clk/Int='0' SPI: All inputs at V_{SS}						
		V_{Back} 1.3	0	-40 to 85		0.6	1.5	µA
				-40 to 125			4.6	
		3.3		-40 to 85		0.8	2.0	
				-40 to 125			5.2	
		5.0		-40 to 85		0.9	2.2	
				-40 to 125			5.5	
Dynamic current I2C	I_{DD}	SCL = 100kHz (See Note 1)	1.3	-40 to 85			12	µA
				-40 to 125			15	
		SCL = 400kHz (See Note 1)	3.3	-40 to 85			35	
				-40 to 125			40	
		SCL = 400kHz (See note 1)	5.0	-40 to 85			50	
				-40 to 125			60	

Dynamic current SPI Interface	I_{DD}	SCK = 200 kHz (See Note 2)	1.3	-40 to 85			14	µA
				-40 to 125			18	
		SCK = 1 MHz (See Note 2)	3.3	-40 to 85			50	
				-40 to 125			55	
		SCK = 1 MHz (See Note 2)	5.0	-40 to 85			65	
				-40 to 125			75	
Low supply detection level1	V_{low1}	Supply voltage V_{CC} variation		-40 to 125	1.70		1.87	V
Low supply detection level2	V_{low2}	Supply voltage V_{CC} variation		-40 to 125	1.25		1.40	V
Switchover hysteresis	V_{hyst}	V_{CC} with respect to V_{Back}= 3.0V	1.3 to 5.0	-40 to 125		20		mV
Input Parameters:								
Low level input voltage	V_{IL}	at CS, CLKOE, SI	1.3 to 5.0				$0.2V_{CC}$	V
High level input voltage	V_{IH}	at CS, CLKOE, SI			$0.8V_{CC}$			V
Input Leakage	I_{IN}	$0.0 < V_{IN} < V_{CC}$	1.3 to 5.0	-40 to 85	-1		1	µA
				-40 to 125	-1.5		1.5	µA
Output Parameters:								
Low level output voltage	V_{OL}	I_{OL} = 0.4 mA	1.3	-40 to 125			0.2	V
High level output voltage	V_{OH}	I_{OH} = 0.1 mA			1.0			V
Low level output voltage	V_{OL}	I_{OL} = 1.5 mA	3.3	-40 to 125			0.25	V
High level output voltage	V_{OH}	I_{OH} = 1.5 mA			2.7			V
Low level output voltage	V_{OL}	I_{OL} = 5.0 mA	5.0	-40 to 125			0.8	V
High level output voltage	V_{OH}	I_{OH} = 2.0 mA			4.5			V
Output HiZ leakage on INT	I_{LEAK_OUT}	$\overline{INT}$ not active	1.3 to 5.0	-40 to 85	-1		1	µA
				-40 to 125	-1.5		1.5	µA
Oscillator:								
Start-up voltage	V_{STA}	T_{STA} < 10s		-40 to 125	1.2			V
Start-up time	T_{STA}		5.0	-40 to 85		0.5	3	s
				-40 to 125		1	3	s
Frequency stability over voltage	$\Delta f/(f*\Delta V)$	$1.8V \le V_{CC} \le 5.5V$, T_A = +25°C		25		0.5	2	ppm/V
Input capacitance on X1	C_{IN}	T_A = +25°C, f = 32.768kHz, V_{meas} = 0.3V (Note 3)		25		16		pF
Output capacitance on X2	C_{OUT}	T_A = +25°C, f = 32.768kHz, V_{meas} = 0.3V (Note 3)		25		16		pF
Trickle Charger								
Current limiting Resistors	R80k	V_{CC} =5.0V, V_{Back}=3.0V		25		80		kΩ
	R20k	V_{CC} =5.0V, V_{Back}=3.0V		25		20		kΩ
	R5k	V_{CC} =5.0V, V_{Back}=3.0V		25		5.0		kΩ
	R1.5k	V_{CC} =5.0V, V_{Back}=3.0V		25		1.5		kΩ

Table 7

Notes: *The following parameters are tested during production test:*

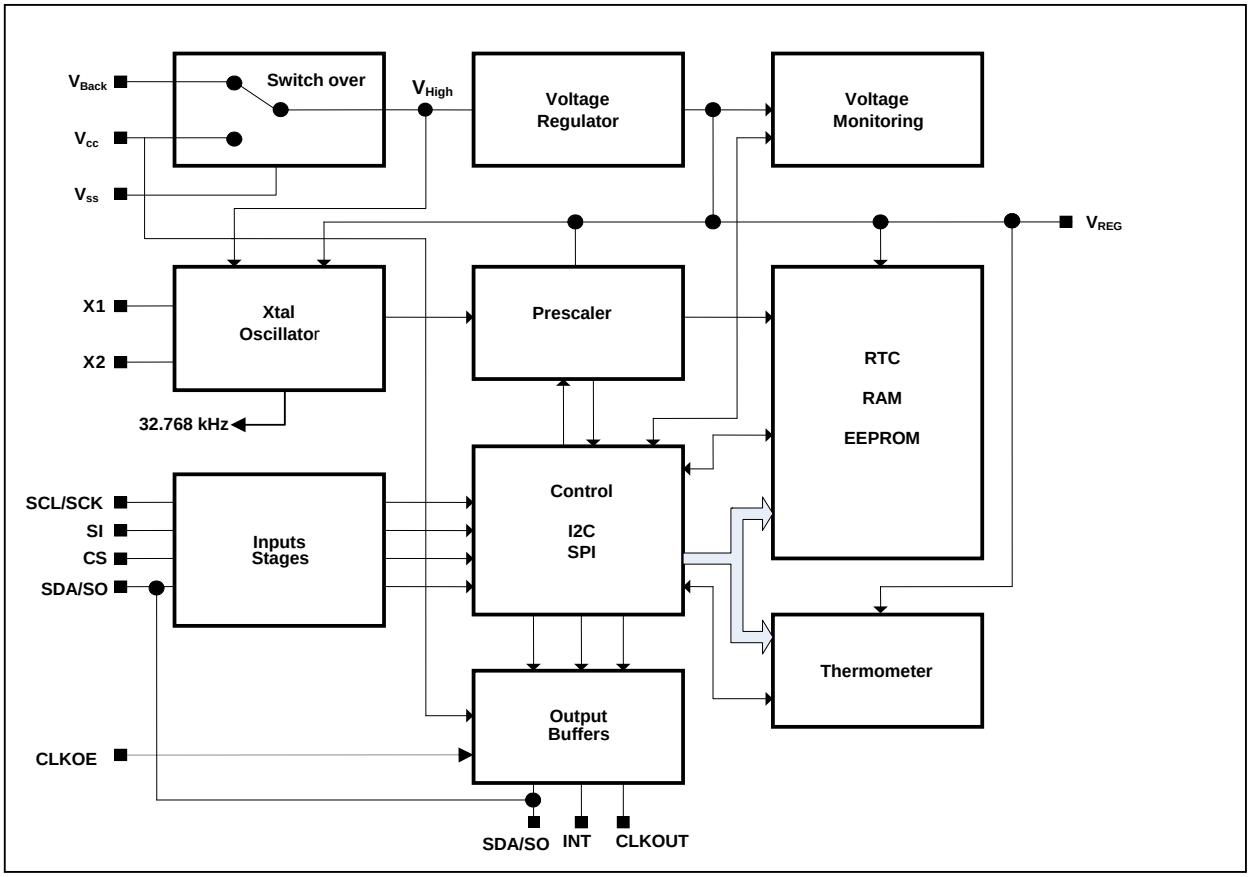
I_{DD}, V_{low1}, V_{low2}, V_{IL}, V_{IH}, V_{OL}, V_{OH}, I_{IN}, I_{LEAK_OUT}

The parameters I_{CC}, V_{hyst}, V_{STA}, T_{STA}, C_{IN}, C_{OUT}, $\Delta f/(f*\Delta V)$ are characterised during the qualification of the IC.

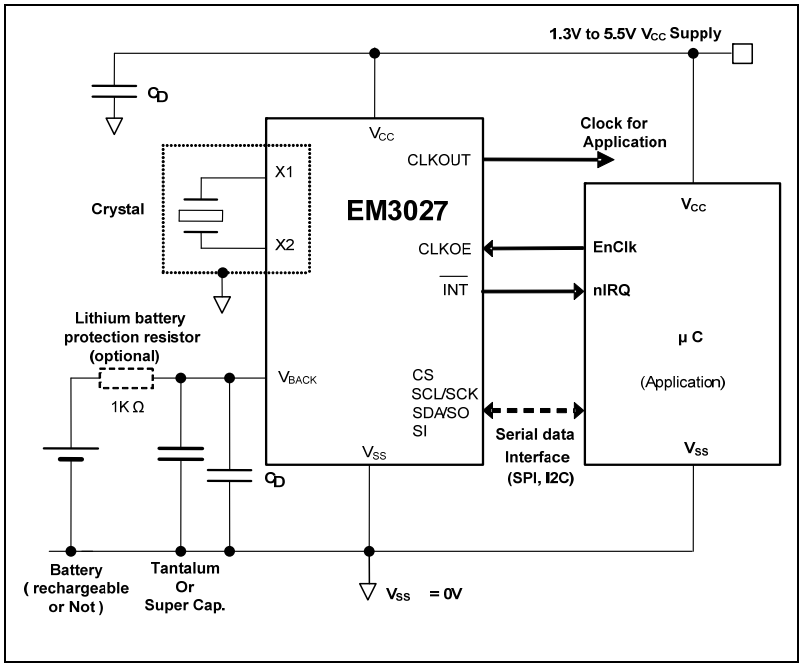
1. SDA ='0', continuous clock applied at SCL
2. CS, SI ='1', continuous clock applied at SCK, SO is not connected
3. V_{meas} : Peak to peak amplitude during capacitance measurement

4 EM 3027 Block Diagram and Application Schematic

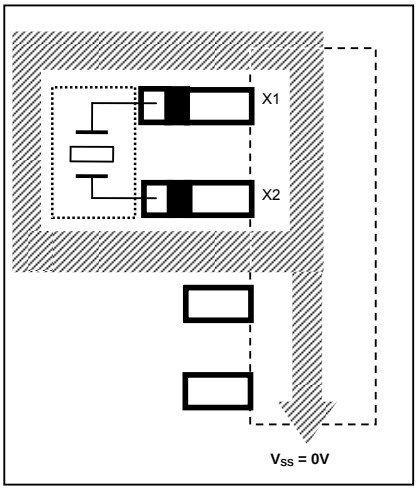
4.1 Block Diagram



4.2 Application Schematic



Crystal Layout Example



4.3 Crystal Thermal Behaviour

A frequency of the real crystal is dependent on the temperature concurring with the following diagram:

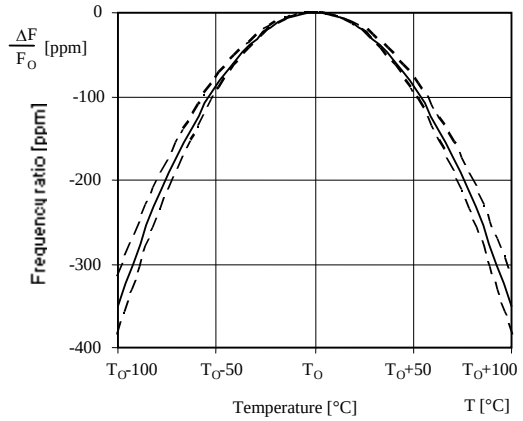


Figure 1 – Crystal thermal behaviour

T_O – Turnover temperature in [°C]
F_O – Crystal frequency when T_O

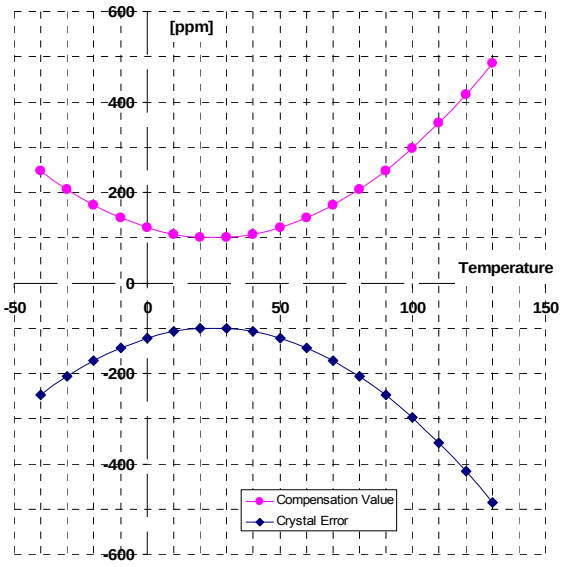
The following formula expresses a compensation value to be used during frequency correction.

$$COMP\_val = Qcoef \times (T - To)^2 - XtalOffset$$

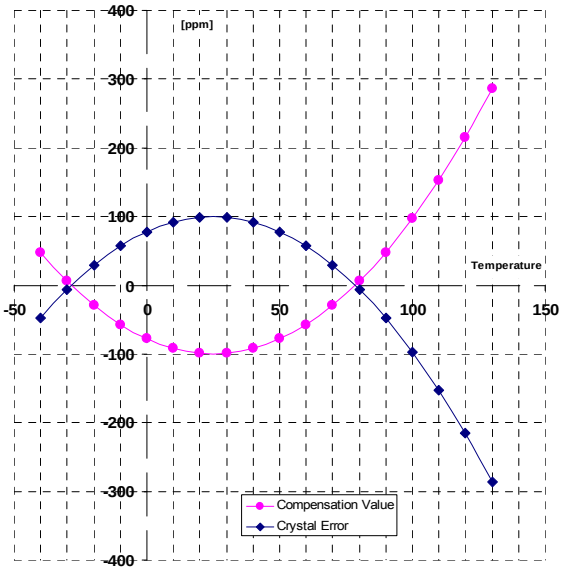
Qcoef	– Thermal quadratic coefficient [ppm/°C^2]
T	– Actual temperature in [°C]
T_O	– Turnover temperature in [°C]
XtalOffset	– Crystal offset at T_O [ppm]
COMP_val	– Compensation value result in [ppm]

The Oscillator Frequency is adjusted, according to the equation above by using coefficients located in the EEPROM control page and a temperature.
The actual temperature can be obtained from the internal thermometer or from Temp register updated externally by an application.
A principle of the frequency compensation is based on the adding/removing of pulses.

Example 1: Qcoef=0.035; T_O=25; XtalOffset=–100



Example 2: Qcoef=0.035; T_O=25; XtalOffset=+100



4.4 Crystal Calibration

In order to compensate temperature dependency of the used crystal properly, correct values of XtalOffset, Qcoef and T_O parameters shall be stored in EEPROM Control Page. User is advised to follow these steps in order to compute the parameters in a correct way:

1) Supply the chip from V_{CC} pin.

2) Set FD0 = FD1 = '0'. Force CLKOE pin to '1'. This provides the uncompensated frequency directly from the crystal oscillator on pin CLKOUT.

3) Measure output frequency f_O at different temperatures (at least five measurements in equidistant points in the whole considered temperature range are recommended).

4) Find a quadratic regression of the measured dependency in form: $f_O = -c_1(T - c_2)^2 + c_3$ or $f_O = aT^2 + bT + c$.

5) Then real values of the searched parameters can by obtained from the following relations:

   $Qcoef_{real} = c_1 = -a$,
   $T_{0\_real} = c_2 = -b/(2a)$,
   $XtalOffset_{real} = c_3 = c - b^2/(4a)$.

6) Values to be stored in EEPROM Control Page have to be corrected in the following way:

   $Qcoef = 4096*(1.05*Qcoef_{real})$,
   $T_0 = T_{0\_real} - 4$,
   $XtalOffset = 1.05*XtalOffset_{real}$.

5 Memory Mapping

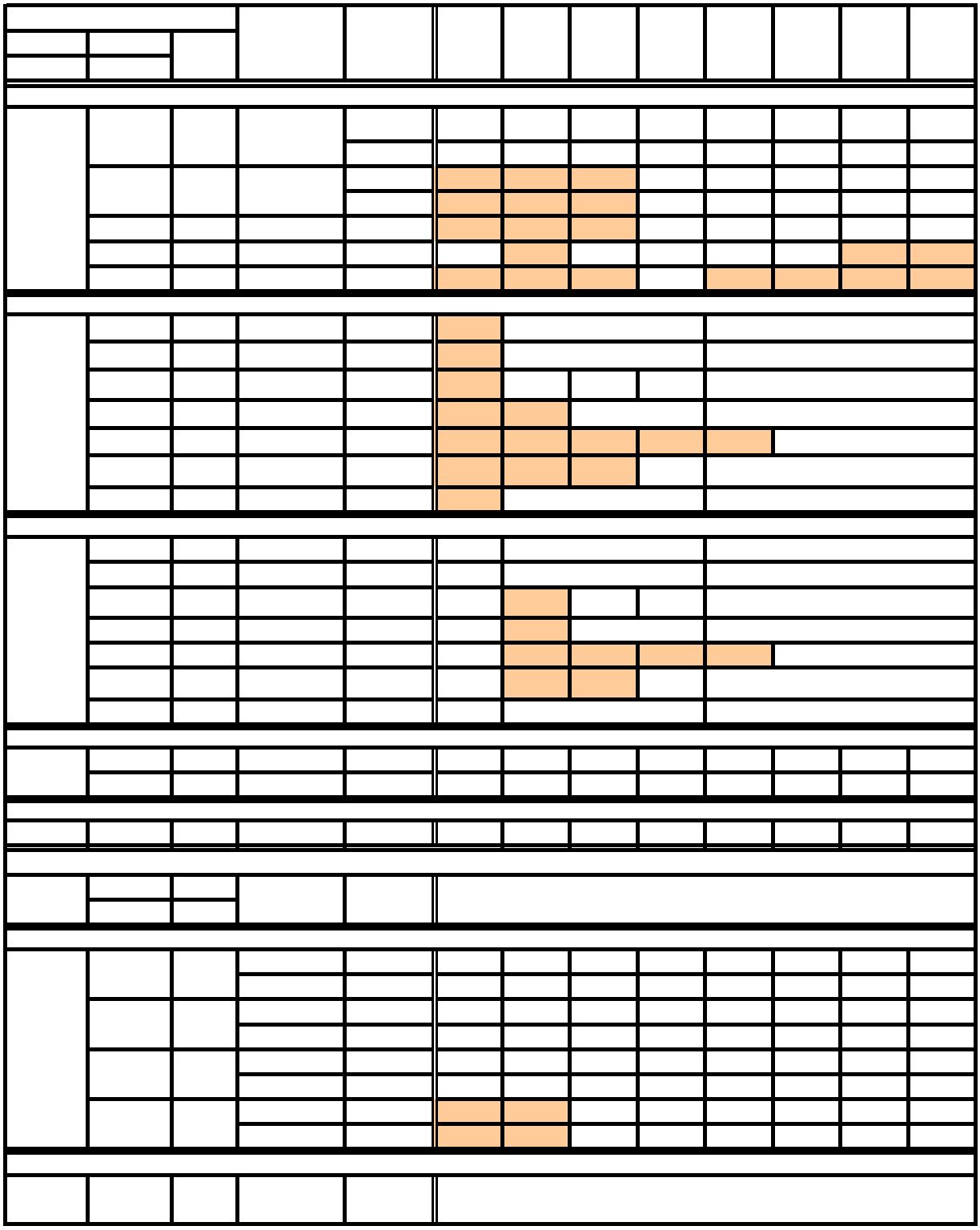


Table 8

Unused bit

Notes and Settings:

- Only pages 0 to 7 are used. Unused pages are dedicated for a future use and test purposes. The application should not write into unused page and addresses
- The XtalOffset must be set to within ± 127 ppm.
- Zero values are read from unused locations.
- Watch, Alarm, Timer pages have to be set by an application before use.
- The bit 7 (MSB) of the Alarm Registers (SecEq, MinEq.) are to be set to '1' to perform the comparison. (See Paragraph 8.3)
- The bit 7 (MSB) of the address is always zero and its value is, therefore, ignored during read/write operation.

6 Definitions of terms in the memory mapping

Control Page - Register *OnOffCtrl*

Clk/Int	Selects if clock or interrupt is applied onto the $\overline{IRQ}$/CLKOUT pin ('0' = $\overline{IRQ}$ output; '1' = CLKOUT output) - CLKOUT is the default state after reset
TD0, TD1	Selects decrement rates for Timer (32 Hz after reset)
SROn	Enables Self-Recovery function (ON after reset)
EERefOn	Enables Configuration Registers refresh each 1 hour (ON after reset);
TROn	Enables Timer Auto-reload mode ('0' – reload disabled; '1' – reload enabled)
TiOn	Enables Timer (OFF after reset)
WaOn	Enables 1 Hz clock for Watch (ON after initialisation)

Control Page - Register *IRQctrl*

SRIntE	Self-Recovery interrupt enable
V2IntE	VLOW2 interrupt enable
V1IntE	VLOW1 interrupt enable
TIntE	Timer interrupt enable
AIntE	Alarm interrupt enable

Control Page - Register *IRQflags*

SRF	Self-Recovery interrupt flag (bit is set to '1' when Self-Recovery reset is generated)
V2F	VLOW2 interrupt flag (bit is set to '1' when power drops below Vlow2)
V1F	VLOW1 interrupt flag (bit is set to '1' when power drops below Vlow1)
TF	Timer interrupt flag (bit is set to '1' when Timer reaches ZERO)
AF	Alarm interrupt flag (bit is set to '1' when Watch matches Alarm)

NOTE: *Flags can be cleared by '0' writing.*

Control Page - Register *Status*

EEBusy	EEPROM is busy (bit is set to '1' when EEPROM write or Configuration Registers refresh is in progress) (Read Only)
PON	Power ON (bit is set to '1' just during Power On; clear by '0' writing)
SR	Self-Recovery reset or System reset detected (clear by '0' writing)
VLOW2	Voltage level V_{CC} or V_{Back} below Vlow2 (clear by '0' writing)
VLOW1	Voltage level V_{CC} or V_{Back} below Vlow1 (clear by '0' writing)

Control Page - Register *RstCtrl*

SYSRes	System reset register; writing '1' will initiate restart of the logic (Watch, Alarm and Timer parts excluded). After the restart, status bit SR is set. The register is cleared after restart of the logic.

Watch Page - Registers *Watch Seconds, Watch Minutes, Watch Hours, Watch Date, Watch Days, Watch Months, Watch Years*

Watch information (BCD format)

S12/24	Run watch in 12-hours format S12/24 = '1' or 24-hours S12/24 = '0'
PM/2	S12/24 = '0' PM/2 represents 2 tens, S12/24 = '1' PM/2 = '1' represents PM (afternoon), PM/2 ='0' represents AM (morning)

Alarm Page - Registers *Alarm Seconds, Alarm Minutes, Alarm Hours, Alarm Date, Alarm Days, Alarm Months, Alarm Years*

Alarm information (BCD format)

PM/2	S12/24 = '0' PM/2 represents 2 tens, S12/24 = '1' PM/2 = '1' represents PM (afternoon), PM/2 ='0' represents AM (morning)

Timer Page - Registers *TimLow, TimHigh*

TimLow	Timer value (Low byte)
TimHigh	Timer value (High byte)

Temperature Page - Register *Temp*

Temp	Temperature (range from -60° C to 190°C with 0°C corresponding to a content of 60d)

EEPROM Data Page - Register *EEData*

EEData	EEPROM data used for user general purpose

EEPROM Control Page - Register *EECtrl*

R80k, R20k, R5k, R1.5k	Selects Trickle resistors between V_{High} and V_{Back}
FD0, FD1	Selects clocks frequency at $\overline{IRQ}$/CLKOUT pin.
ThEn	Thermometer Enable
ThPer	Selects the thermometer scan period, voltage detector scan period ('0' – 1 second; '1' – 16 seconds)

EEPROM Control Page - Register *XtalOffset*

XtalOffset — Crystal frequency deviation at Turn over temperature T_O in ppm. Example: value 63d is related to 60 ppm.

$$XtalOffset = 1.05 * XtalOffset_{real}$$

Where $XtalOffset_{real}$ is real value of crystal frequency deviation at Turn over temperature of the used crystal in ppm.

Note: *Coefficient 1.05 (exactly 1.048576) is the result of the internally used frequency compensated method.*

EEPROM Control Page - Register Q*coef*

Qcoef — Thermal quadratic coefficient of the crystal. Example: value 151d is related to 0.035 ppm/°C²;

$$Qcoef = 4096 \times 1.05 \times QCoef_{real}$$

Where $Qcoef_{real}$ is real value of thermal quadratic coefficient of the used crystal in ppm/°C².

EEPROM Control Page - Register *TurnOver*

TurnOver — Turn over temperature of the crystal (values 0 to 63d are related to temperature 4 to 67 °C). Example: value 21d is related to 25°C.

$$T_0 = T_{0\_real} - 4,$$

Where T_{0_real} is real value of Turn over temperature of the used crystal in °C.

RAM Page - Register *RAMdata*

RAMdata	RAM data used for application general purposes

7 Serial communication

Any serial communication with the chip starts with a “Transmission START” and terminates with the “Transmission STOP”.

“Transmission START”
I2C – START condition
SPI – CS goes to active

“Transmission STOP”
I2C – STOP condition
SPI – CS goes to inactive

At the same moment the “Transmission START” is detected a copy of Watch, Timer, and Temperature register content is copied into a cache memory. A following read access is provided from the cache memory.

Data in the cache for reading are stable until the “Transmission STOP”.

At the same moment the “Transmission STOP” is detected, the content of the cache memory is copied into Watch, Timer, or Temperature registers selected by the “page address” when R/W was set to ‘1’.

7.1 How to perform READ/WRITE through I2C

The I2C protocol is a bidirectional protocol using 2 wires for master-slave communication. SCL (clock) and SDA (data) signals are used. This protocol allows a connection of more slaves through a bus. The bus is pulled-up (externally by resistors) and drivers are realised by open drain drivers. This chip can work as slave only.

The communication is controlled by the master. At the beginning of each transmission a start bit is sent (transmission START). A slave address follows with last bit which selects if READ or WRITE is initiated. If slave address sent by the master is equal to the slave address of the slave then slave continues to communicate with the master. Each slave address, address or data byte is finished by an acknowledge bit (ACK). It’s possible to WRITE/READ the whole “page” during one transmission with automatic address increment feature. Only three less specified bits of the address are incremented.

In case of WRITE transmission the address byte is sent to the slave and data bytes can follow (MSB first order is used). A less significant part of the address is incremented after each data byte is received. The “page address” is fixed until a new address is received.

In case of READ transmission the slave sends data bytes. An address is defined by the last address change (WRITE transmission or a last increment). The “page address” can be changed only by WRITE transmission. A less significant part of the address is incremented also after each ACK received from the master. If ACK is not received then data are read from the same address.
At the end of each transmission a stop bit is send (transmission STOP).

I2C: Write transmission

	Slave Address	R/W										
S	**1010110**	**0**	**ACKs**	**Address**	**ACKs**	**Data Byte (1)**	**ACKs**	**Data Byte (n-1)**	**ACKs**	**Data Byte (n)**	**ACKs**	**P**

I2C: Read transmission

	Slave Address	R/W						Slave Address	R/W						
S	**1010110**	**0**	**ACKs**	**Address**	**ACKs**	**P**	**S**	**1010110**	**1**	**ACKs**	**Data byte (1)**	**ACKm**	**Data byte (n)**	**ACKm**	**P**

S ... a start condition sent by a master
ACKs ... an acknowledge from the slave
ACKm ... an acknowledge from the master
R/W ... read/write select
P ... a stop condition

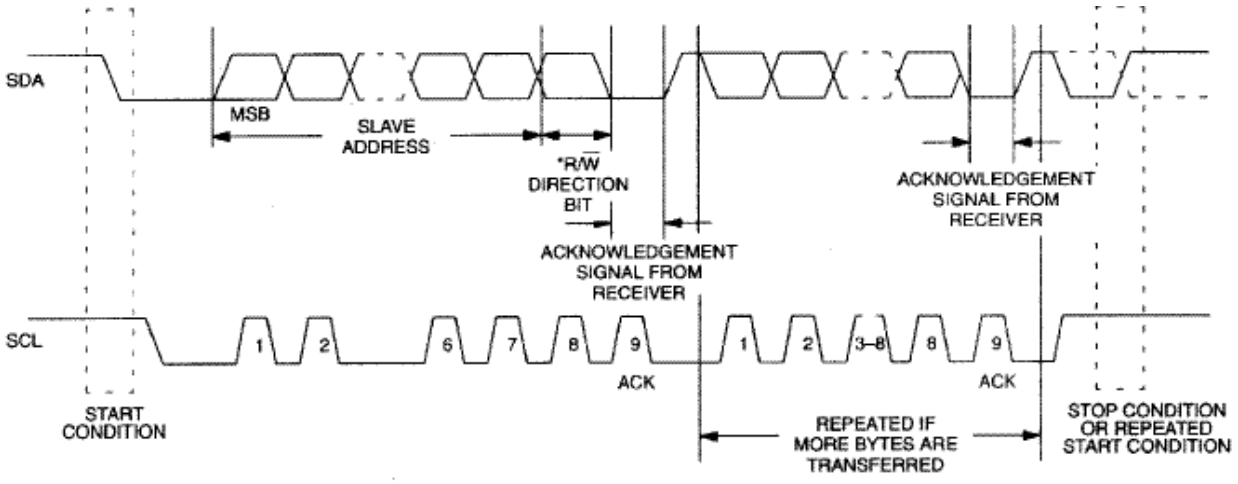


Figure 2 – I2C communication

As the EM3027 has an integrated pull up resistor (100kΩ) at SCL, the supply V_{CC} must always be applied during an I2C transmission, also if other IC's are addressed (due to EM3027 internal protection diode on SCL and SDA pins)

7.2 How to perform READ/WRITE through SPI

The SPI protocol is used to connect master and slaves. 4 wires are used: CS (Chip Select), SCK (serial clock), SI (input data) and SO (output data). This chip can work as slave only.

SPI is byte oriented protocol (MSB first order is used). Data are changing on SCK falling edge and sampled on the rising edge.

It's possible to WRITE/READ the whole "page" during one transmission with automatic address increment feature. Only three less specified bits of the address are incremented.

At the beginning of the transmission Chip Select goes to active. First bit of data selects if READ or WRITE operation will follow after an address. The address is composed of 7 bits.

If WRITE transmission is initiated then master continues with data sending byte by byte. A less significant part of the address is automatically incremented after each data byte is received. The "page address" is fixed until a new transmission is started. SO data output stays at '0' during the whole transmission.

If READ transmission is initiated then data are send after the address by the slave. A less significant part of the address is automatically incremented after each data byte sent. The "page address" is not changing until a new transmission is started. SI data input is not cared.
SO is in tri-state when CS inactive.

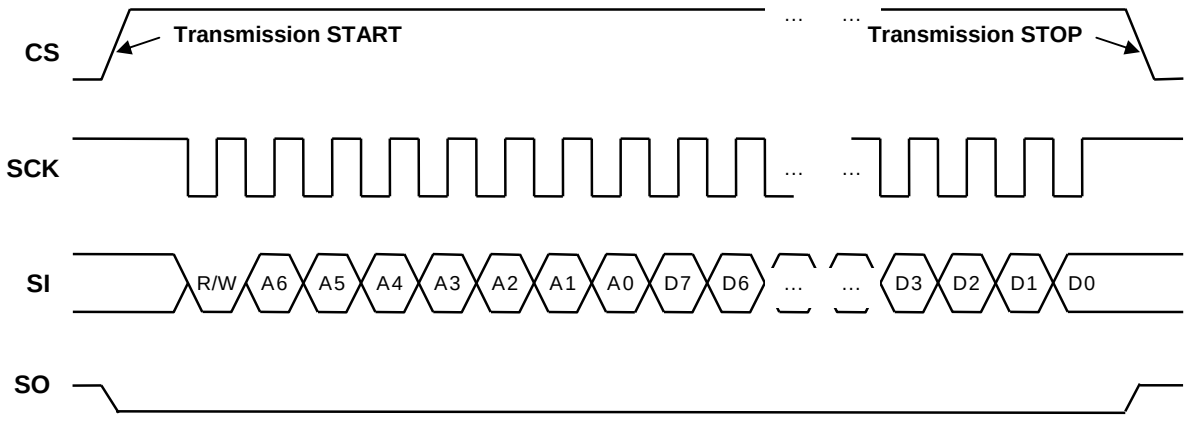


Figure 3 – SPI Write Transmission

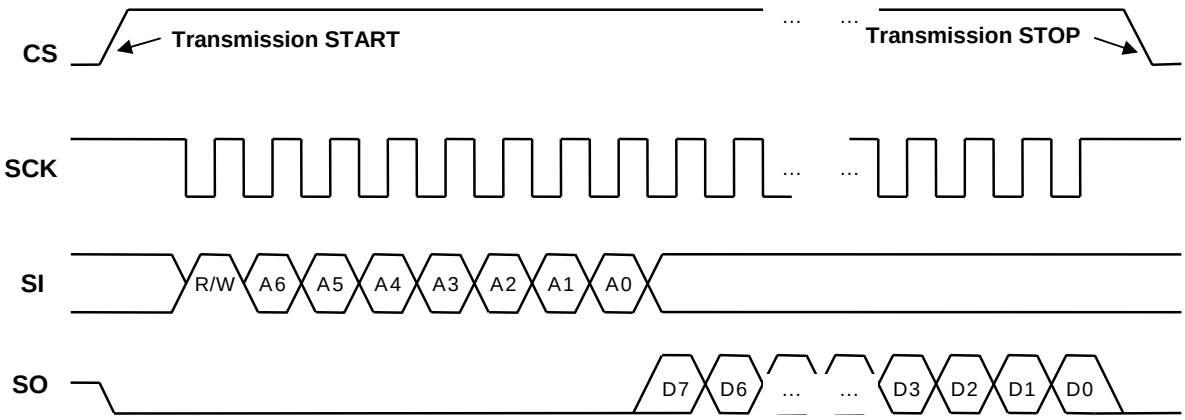


Figure 4 – SPI Read Transmission

8 Functional Description

8.1 Start after power-up

A The chip is in reset state when supply voltage (V_{CC} or V_{Back}) is below an internal threshold level (PON in Status register 0x03 goes to '1'). When the supply level is higher than this threshold voltage, the reset is released.

B When the supply voltage is higher than the oscillator start voltage, the basic clocks for Watch and control logic become active after the oscillator start time.

C With clocks present, the voltage detector starts in fast mode to measure the supply voltage. When a voltage higher than Vlow2 is detected, the fast detection mode is stopped and the EEPROM read is enabled.

D The configuration registers are loaded with the configuration data read from the EEPROM (Addresses 0x29 to 0x33). The EM3027 starts its normal function, depending on the supply voltage level applied.

8.2 Normal Mode function

The chip has following functions in Normal Mode:

1. **Voltage detection** – The voltage detection is executed each 1 or 16 seconds (depending on ThPer bit)
2. **Temperature measurement** – It is executed if voltage is above Vlow1 and thermometer is enabled (ThEn bit). With the temperature measurement result, the compensation value for frequency correction is computed.
3. **Frequency compensation** – The compensation of the oscillator frequency works continuously.
4. **Configuration Registers refresh** – The EEPROM is read each hour to refresh the content of the configuration registers (supply voltage must be above Vlow2)
5. **Watch/Alarm** – The Watch function is continously active, whereas the Alarm function depends on its activation.
6. **Timer** – Is active when enabled.
7. **Self-Recovery system** – Is enabled by default (can be disabled by the application)
8. **Serial interface** – The communication works if $V_{CC} > V_{Back}$

8.3 Watch and Alarm functionality

The Watch part provides timing information in BCD format. The timing data is composed of seconds, minutes, hours, date, weekdays, months and years. The corresponding values are updated every second.

The Watch part setup is provided by Write transmission into the Watch Page (Address 0x08h to 0x0Eh). After the transmission, the Watch is restarted from the setup values after one second.

The Alarm function is activated by setting and enabling the alarm registers (Address 0x10h to 0x16h). Each Alarm byte has its own enable bit. It is the bit 7. Recommended combinations of enabled bits are described in the table below.

Table 9 – Alarm Period Selection

SecEq	MinEq	HrsEq	DateEq	DaysEq	MonthEq	YearEq	Al_period
1	0	0	0	0	0	0	min
1	1	0	0	0	0	0	hrs
1	1	1	0	0	0	0	day
1	1	1	1	0	0	0	month
1	1	1	1	0	1	0	year
1	1	1	0	1	0	0	week

- Both Watch and Alarm parts must be set by an application before use
- The bits SecEq to YearEq enable the comparison of the corresponding registers

8.4 Timer function

The 16-bit count down timer can be enabled/disabled by TiOn bit.

It's possible to select timer frequency by TD1, TD0 bits according to the following table:

TD1	TD0	Timer frequency
0	0	32 Hz
0	1	8 Hz
1	0	1 Hz
1	1	0.5 Hz

Table 10 – Timer Frequency Selection

The timer can run in Zero-Stop or Auto-Reload mode (TROn bit; '0' – Zero-Stop mode, '1' – Auto-Reload mode).
When TROn = '0' then it's possible to read current value of the timer. If TROn = '1' then last written value is read from cache memory. The value in the cache memory is used as a new value during reloading (Auto-Reload).
Timer values (TimLow, TimHigh), frequency selection (TD1, TD0) and mode selection (TROn) can be provided only when the timer is stopped (TiOn = '0').

NOTE: *The "Timer Page" can also be used as a general purpose register when the timer function is not used.*

8.5 Temperature sensor

The integrated thermometer has a resolution of 1°C.

The thermometer is disabled when (ThEn = '0') and enabled when (ThEn = '1'). By default, the thermometer is enabled.

The thermometer is automatically disabled when VLOW1 status bit is at '1'.

When the thermometer is disabled (ThEn = '0'), the Temp register can be written. The write operation computes immediately a new compensation value for frequency correction.

Temp register uses also a cache memory to keep stable value during a whole transmission (read/write).

8.6 Temperature compensation

Compensation value (COMP_val) for temperature correction is computed each 1s or 16s (ThPer bit) when thermometer is enabled (ThEn = '1') or just once after Temp register is written and thermometer is disabled (ThEn = '0'). After power-up the compensation value is zero. The compensation value is computed according to the equation described in **chapter 4.3**.
Thermometer period is selectable by ThPer bit according to the table below:

ThPer	Period in Seconds
0	1 s
1	16 s

Table 11 – Thermometer Period

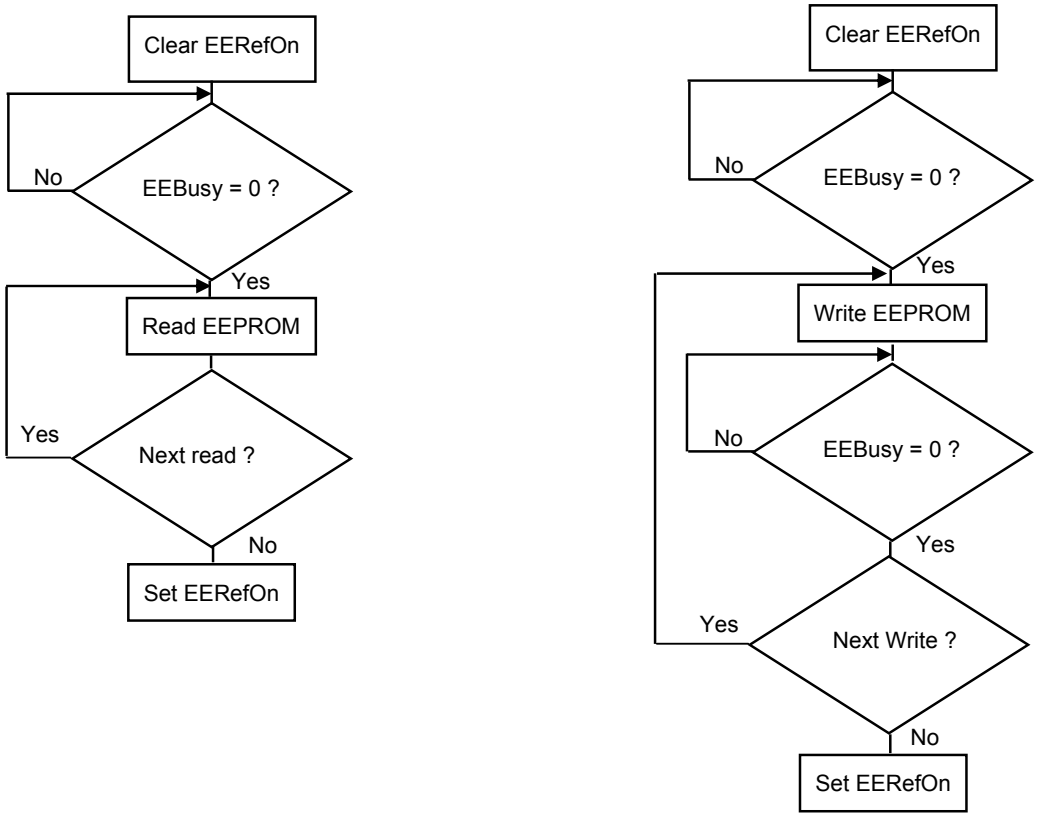
When VLOW1 status bit is at '1', the last computed compensation value is used. Temperature correction of crystal frequency is provided continuously.

8.7 EEPROM memory

Before any EEPROM access (read/write), the bit EERefOn has to be cleared by the application to prevent from access collision with the Configuration Registers. Then the application has to read EEBusy bit and if EEBusy = '0' then EEPROM access can be started.

After write command ("Transmission STOP") the current state of EEPROM writing is monitored by EEBusy register bit at '1'. EEBusy goes to '0' when EEPROM writing is finished.

NOTE: *(V_{CC} >V_{prog})* V_{CC} *must be connected during whole EEPROM write.*



8.7.1 EEPROM Control Page

This part is composed of 4 bytes purposed for miscellaneous function control and for crystal compensation constants. EEctrl byte contains: trickle charger selectors (R80k, R20k, R5k, R1.5k); output clock frequency selector (FD1, FD0); thermometer enable and thermometer period selector.

8.7.2 Clock Output

Output clock frequency is selected by FD1, FD0 bits in EEcrtl register.

FD1	FD0	Select Clocks Out	Description
0	0	32768 Hz	Crystal Oscillator without correction
0	1	1024 Hz	Compensated frequency
1	0	32 Hz	
1	1	1 Hz	

Table 12 – Output Clock frequency selector

8.7.3 Configuration Registers

All the configuration data from EEPROM (i.e. EECtrl, XTalOffset, Qcoef, TurnOver, EEData) is hold in configuration registers. Data from EEPROM is loaded to these registers during power-up sequence and is refreshed each hour, if 'Configuration Registers refresh' feature is enabled (EERefOn = '1').

Regular refresh of Configuration Registers prevents their content to be corrupted by strongly polluted electrical environment (EMC problems, disturbed power supply, etc.) It is recommended to enable 'Configuration Registers refresh' feature.

8.7.4 EEPROM User Memory

One byte of the memory is dedicated for the application.

8.8 RAM User Memory

RAM memory size is 8 bytes. The state of RAM data part after power-up is undefined.

8.9 Status Register

The purpose of EEBusy bit is to inform users about current status of the EEPROM operations.

EEBusy – status of EEPROM controller (if EEBusy = '1' then Configuration Registers refresh or EEPROM write in progress)

The purpose of the following status bits is to record status of power supply voltage and Self-Recovery system/System reset behaviour.

PON – status of Power-ON
VLOW1 – status of Vlow1 voltage detection
VLOW2 – status of Vlow2 voltage detection
SR – status of the Self-Recovery system/System reset

If one of these status bits is set, it can be cleared only by writing '0', there is no automatic reset if the set condition disappears.

8.10 Interrupts

There are five interrupt sources which can output an interrupt on ($\overline{INT}$ and/or $\overline{IRQ}$/CLKOUT) pins. The request is generated when at least one of IRQflags goes to '1' (OR function).

AF – interrupt is provided when Watch time reaches Alarm time settings and comparison is enabled
TF – interrupt is provided when Timer reaches ZERO
V1F – interrupt is provided when supply voltage is below Vlow1 (VLOW1 status "rising edge")
V2F – interrupt is provided when supply voltage is below Vlow2 (VLOW2 status "rising edge")
SRF – interrupt is provided when Self-Recovery system invoked internal reset (SR status "rising edge")

Each interrupt source has its own interrupt enable (AIntE, TIntE, V1IntE, V2IntE, SRIntE). When the interrupt enable is '1' then the appropriate interrupt source is enabled.

Interrupt flags (IRQflags) are cleared by '0' writing into the appropriate bit. In case of V1F, V2F and SRF bits, it is necessary to clear also corresponding status bits (Status) after interrupt bit.

8.11 Self-Recovery System

The purpose of the Self-Recovery System (SRS) is to generate an internal chip reset in case the on chip state machine goes into a deadlock. The function is based on an internal counter that is periodically reset by the control logic. If it is not reset properly on time, the chip reset will take place. It is executed after two voltage monitoring periods at the latest, i.e. 2s or 32s (ThPer bit).

A possible source of a deadlock could be polluted electrical environment (EMC problem, disturbed power supply, etc.).

SRS sets status bit SR and resets the whole internal logic except Watch, Alarm and Timer parts (i.e. time information are not affected). Furthermore, if the SRS interrupt is enabled (SRIntE='1'), the SRF flag is set after the internal chip reset. Note, that SROn='1' and SRIntE='0' after the reset.

After the internal chip reset, the device starts with the power-up sequence (see chapter 8).

SRS is automatically enabled after power-up (SROn bit). It can be disabled by writing '0' into the SROn.

8.12 Register Map

The address range of the EM3027 is divided into pages. The page is addressed by the five most significant bits of the address. The three low significant bits of the address provide selection of registers inside the page. During address incrementing only three low significant bits are changed. The page address part is fixed during whole data transmission.

8.13 Xtal Oscillator and Prescaler

The 32.768 kHz Xtal oscillator and the clock divider provide the timing signal for the functional blocks. Prescaler block is responsible for frequency division of the 32.768 kHz clock signal coming from the Xtal oscillator. Divided frequency is then distributed between other blocks inside the chip including Watch, Timer and control logic.
Two capacitors C_{IN} and C_{OUT} are integrated on chip – see Figure 5.

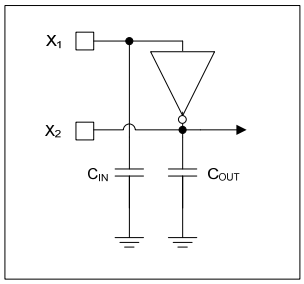


Figure 5

9 Power Management

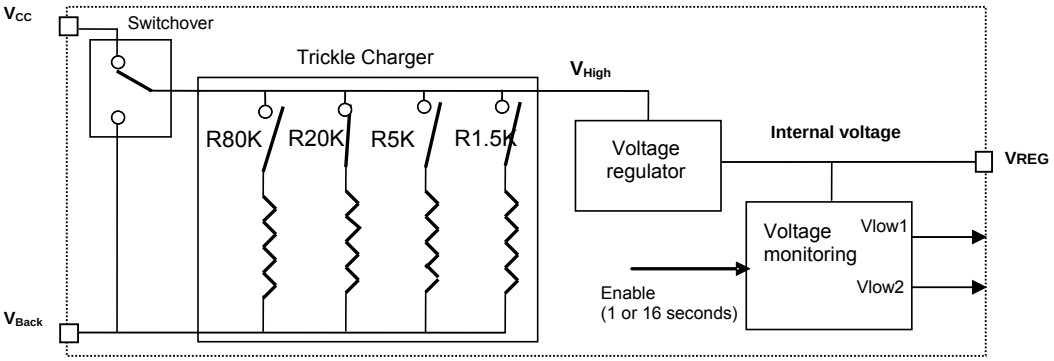


Figure 6 – Power management

9.1 Power Supplies, Switchover and Trickle Charge

The device can be supplied from the V_{CC} pin or from the V_{Back} pin. The switchover block implemented inside the chip compares V_{CC} and V_{Back} voltages and connects the higher of them to the internal V_{High} level that supplies the chip. Nevertheless, the communication pins (SCL, SDA or CS, SCK, SI, SO) are supplied from the V_{CC} pin only. For that reason, when serial interface (I2C or SPI) is used, the whole chip has to be supplied from V_{CC}. (i.e. $V_{CC} > V_{Back}$).

The serial data communication can be performed if $V_{CC} > V_{Back,}$ in this condition the input and output pins are enabled.

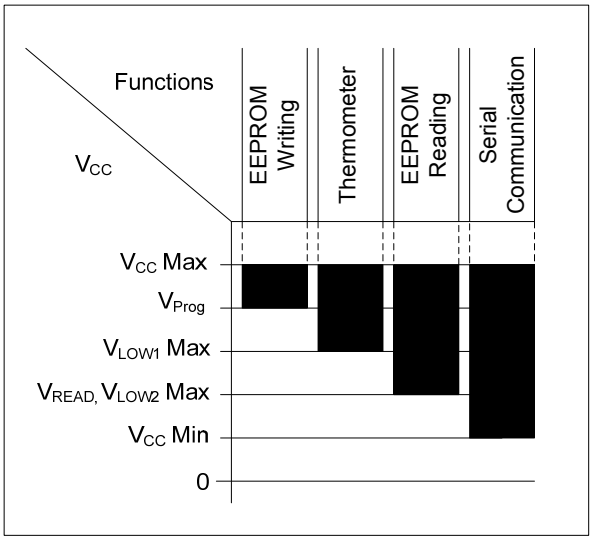


Figure 7 – Operating voltage functions

By setting of a trickle charger bit in register EECtrl a resistor can be inserted between V_{Back} and V_{High} voltage. In this way a rechargeable battery or a super-cap can be charged from the V_{CC} voltage, as long as $V_{CC} > V_{Back}$. More than one resistor can be selected or all.

There are 4 selectable resistors with a nominal value of 80kΩ, 20kΩ, 5kΩ and 1.5kΩ can be set by EEctrl bits.

9.2 Low Supply Detection

The supply voltage level is monitored periodically versus Vlow1 and Vlow2 levels. The monitoring rate is defined by the ThPer bit and is the same as the temperature monitoring rate. When the voltage monitoring is running a higher current consumption for few milliseconds occurs.

At the power-up of the device, as long as the supply voltage stays below Vlow2, the monitoring rate is speeded up. It is necessary to power up at a level above Vlow2 in order to be able to read out initialization data from EEPROM and to leave the fast monitoring rate with higher current consumption. (See chapter 8.1)

When the voltage drops below Vlow1 then the VLOW1 status bit is set to '1'. It is only possible to clear VLOW1 by increasing the supply voltage above Vlow1 and then writing '0' into the VLOW1 status bit.

When bit VLOW1 is at '1', the thermometer is disabled and the automatic computation of compensation value (COMP_val) for frequency correction is inhibited. In this case the last computed compensation value is used.

The device continues to work until the supply voltage drops below the limit Vlow2 which is the minimum supply voltage of the device with EEPROM read out function.

When bit VLOW2 is set, it can only be reset by increasing the supply above the level Vlow2 and then writing '0' into the VLOW2 status bit.

Below the Vlow2 level the EEPROM read out is disabled and the device functionality is not guaranteed.

10 AC Characteristics

10.1 AC characteristics – I2C

V_{SS} = 0V and T_A=-40 to +125°C, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Vcc ≥ 3.0V			400	kHz
		Vcc >1.8V			300	
		Vcc>1.3V			100	
Bus Free Time Between STOP and START Condition	t_{BUF}	Vcc ≥ 3.0V	0.4			µs
		Vcc >1.8V	0.5			
		Vcc>1.3V	1.0			
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Vcc ≥ 3.0V	0.2			µs
		Vcc >1.8V				
		Vcc>1.3V				
LOW Period of SCL Clock	t_{LOW}	Vcc ≥ 3.0V	1.3			µs
		Vcc >1.8V	1.7			
		Vcc>1.3V	4.5			
HIGH Period of SCL Clock	t_{HIGH}	Vcc ≥ 3.0V	0.4			µs
		Vcc >1.8V	0.5			
		Vcc>1.3V	0.6			
Setup Time START Condition	$t_{SU:STA}$	Vcc ≥ 3.0V	20			ns
		Vcc >1.8V	30			
		Vcc>1.3V	50			
Data Hold Time	$t_{HD:DAT}$	Vcc ≥ 3.0V	20			ns
		Vcc >1.8V	30			
		Vcc>1.3V	50			
Data Setup Time	$t_{SU:DAT}$	Vcc ≥ 3.0V	50			ns
		Vcc >1.8V	80			
		Vcc>1.3V	100			
Data Valid Time	$t_{VD:DAT}$	Vcc ≥ 3.0V	1.2			µs
		Vcc >1.8V	1.5			
		Vcc>1.3V	4.0			
Data Valid Acknowledge Time	$t_{VD:ACK}$	Vcc ≥ 3.0V	0.9			µs
		Vcc >1.8V	1.1			
		Vcc>1.3V	3.5			
Rise Time of Both SDA and SCL Signals	t_R	Vcc ≥ 3.0V			200	ns
		Vcc >1.8V			300	
		Vcc>1.3V			1000	
Fall Time of Both SDA and SCL Signals (See note 1)	t_F	Vcc ≥ 3.0V			200	ns
		Vcc >1.8V			300	
		Vcc>1.3V			400	
Setup Time (Repeated) STOP Condition	$t_{SU:STO}$	Vcc ≥ 3.0V	20			ns
		Vcc >1.8V	30			
		Vcc>1.3V	50			
Length of spikes suppressed by the input filter on SCL ans SDA	t_{SP}	Vcc ≥ 3.0V			50	ns
		Vcc >1.8V				
		Vcc>1.3V				
Capacitive Load For Each Bus Line	C_B	Vcc ≥ 3.0V			200	pF
		Vcc >1.8V				
		Vcc>1.3V				
I/O Capacitance (SDA, SCL)	$C_{I/O}$	Vcc ≥ 3.0V			10	pF
		Vcc >1.8V				
		Vcc>1.3V				
Internal SCL pull-up resistor	R_{PU}			100		kΩ

Table 13

Verified by design. Not tested in production.

Notes:

1) Falling time on SDA driven by EM3027 can be shorter than 20 + 0.1* C_B as required by I2C standard.
2) There are parasitic diodes between SCL, SDA pads and Vcc power supply.
3) Device does not internally provide a hold time of 300ns as required by I2C standard.

Calculation of external-pull up

All of the following conditions have to be met:

- Rise time is equal to 0.847* R_{PU} * C_B => Rpu < $t_{R\ max}$/(0.847* C_B).
- Maximum sink current driven by SDA pad in output mode => R_{PU} < Vcc / $I_{SINK\ min}$

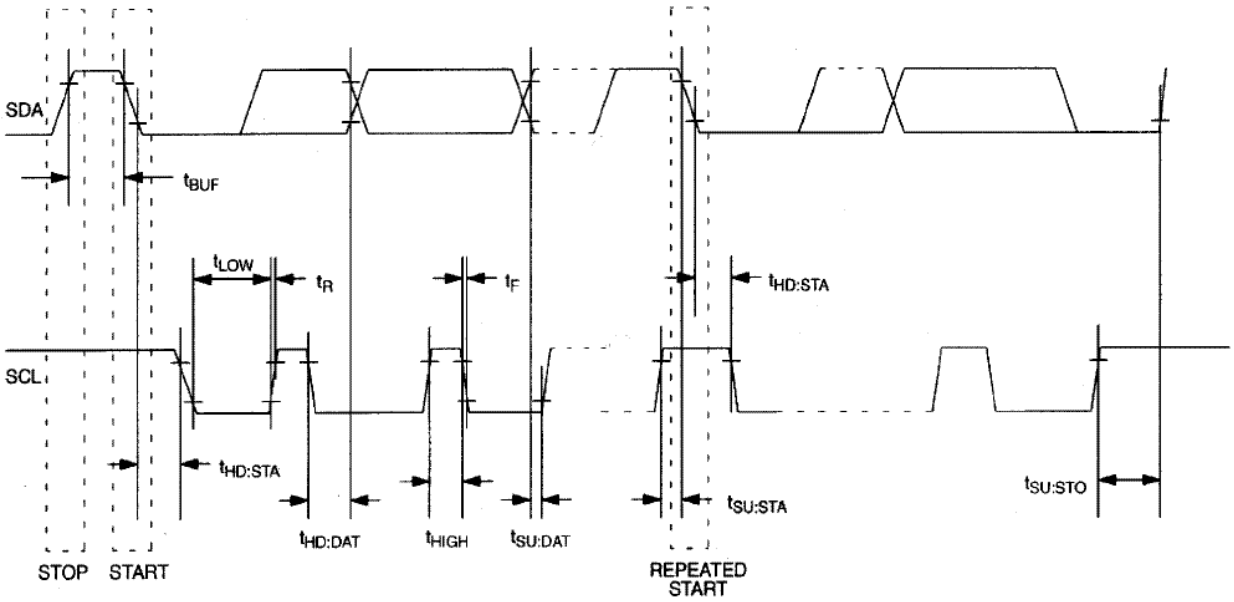


Figure 8 : Timing - I2C

10.2 AC characteristics – SPI

V_{SS} = 0V and T_A=-40 to +125°C, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Clock Frequency	f_{SCK}	Vcc ≥ 3.0V			1	MHz
		Vcc >1.8V			600	kHz
		Vcc >1.3V			200	
Data to SCK setup	t_{DC}	Vcc ≥ 3.0V	20			ns
		Vcc >1.8V				
		Vcc >1.3V				
SCK to Data Hold	t_{CDH}	Vcc ≥ 3.0V	200			ns
		Vcc >1.8V	300			
		Vcc >1.3V	500			
SCK to Data Valid	t_{CDD}	Vcc ≥ 3.0V			350	ns
		Vcc >1.8V			650	
		Vcc >1.3V			1300	
SCK Low Time	t_{CL}	Vcc ≥ 3.0V	400			ns
		Vcc >1.8V	700			
		Vcc >1.3V	1500			
SCK High Time	t_{CH}	Vcc ≥ 3.0V	400			ns
		Vcc >1.8V	700			
		Vcc >1.3V	1500			
SCK Rise and Fall	t_R , t_F	Vcc ≥ 3.0V			200	ns
		Vcc >1.8V			800	
		Vcc >1.3V				
CS to SCK Setup	t_{CC}	Vcc ≥ 3.0V	100			ns
		Vcc >1.8V				
		Vcc >1.3V				
SCK to CS Hold	t_{CCH}	Vcc ≥ 3.0V	200			ns
		Vcc >1.8V	300			
		Vcc >1.3V	500			
CS Inactive Time	t_{CWL}	Vcc ≥ 3.0V	200			ns
		Vcc >1.8V	300			
		Vcc >1.3V	400			
CS to Output High Impedance	t_{CDZ}	Vcc ≥ 3.0V			50	ns
		Vcc >1.8V			100	
		Vcc >1.3V			200	

Table 14

Verified by design. Not tested in production.

1) Max. bus capacitance on SO line shall be lower than 100pF and 50pF when Vcc > 1.8V and Vcc < 1.8V, respectively.

2) Spikes on SCK signal shorter than 50ns are suppressed.

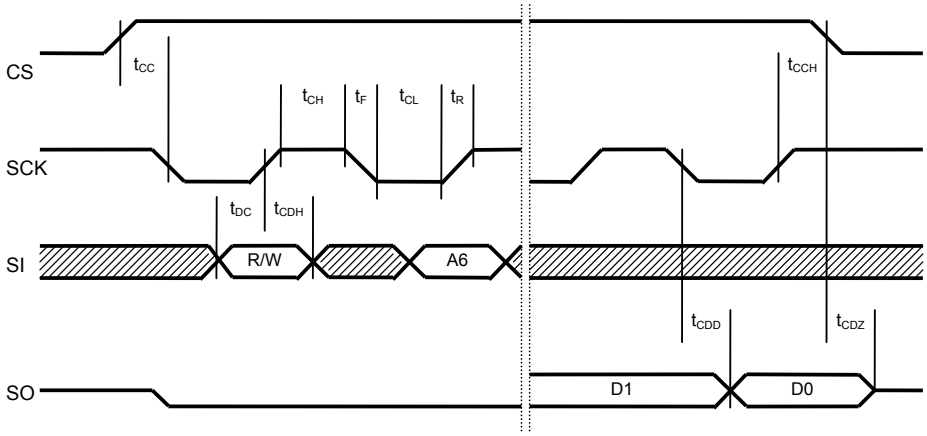


Figure 9 : Timing - SPI read

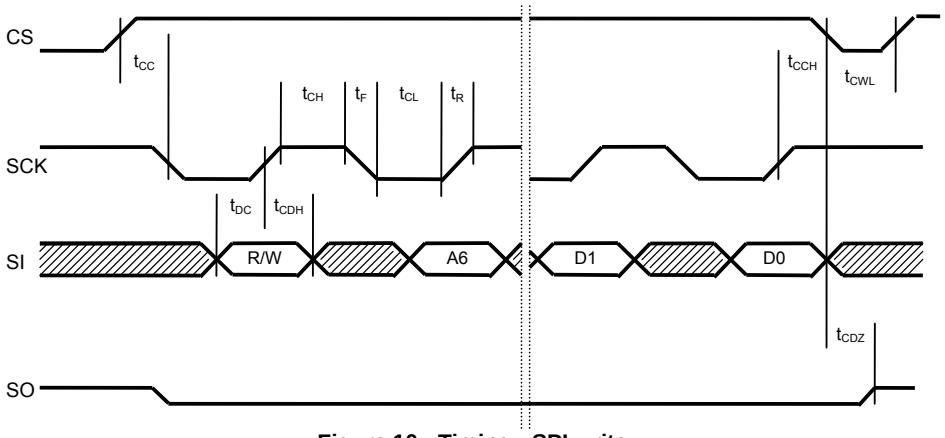


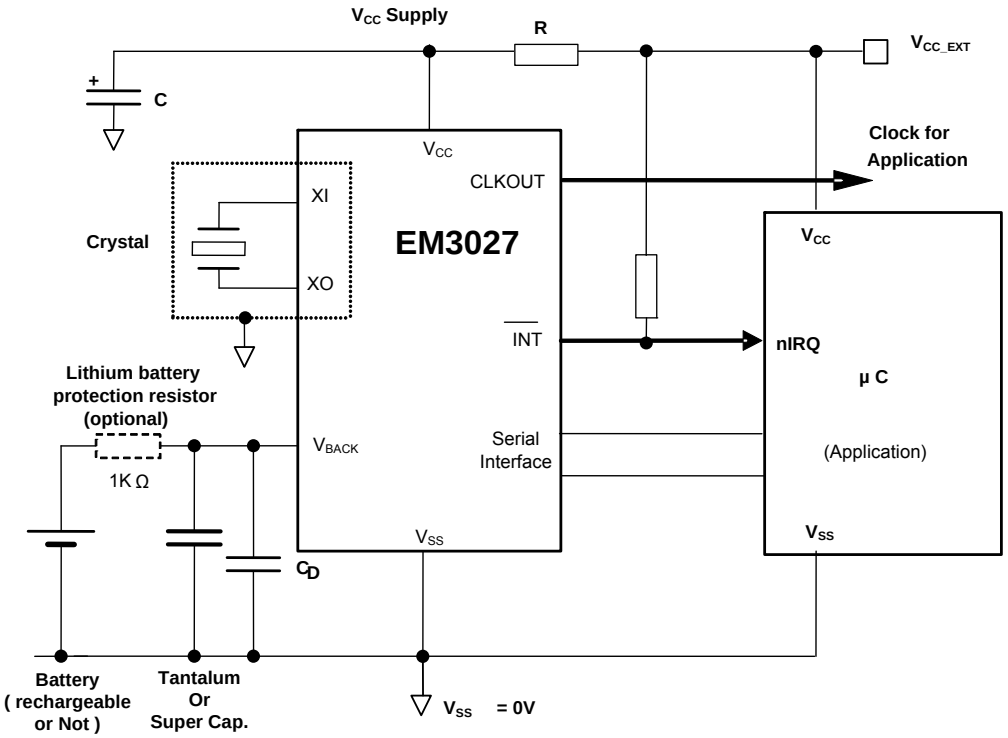
Figure 10 : Timing - SPI write

11 Using EM3027 with disturbed Supply Voltage on V_{CC}

If the power supply of the EM3027 (V_{CC}) is disturbed, the circuit must be protected against V_{CC} fast transients. As the oscillator has a very low power consumption, the clock generation is sensitive to fast supply changes and clock pulses could be lost.

If in the application, positive or negative V_{CC} fast slopes may occur, an RC low pass filter in the V_{CC} supply connection of the EM3027 must be used, according to the following figure :

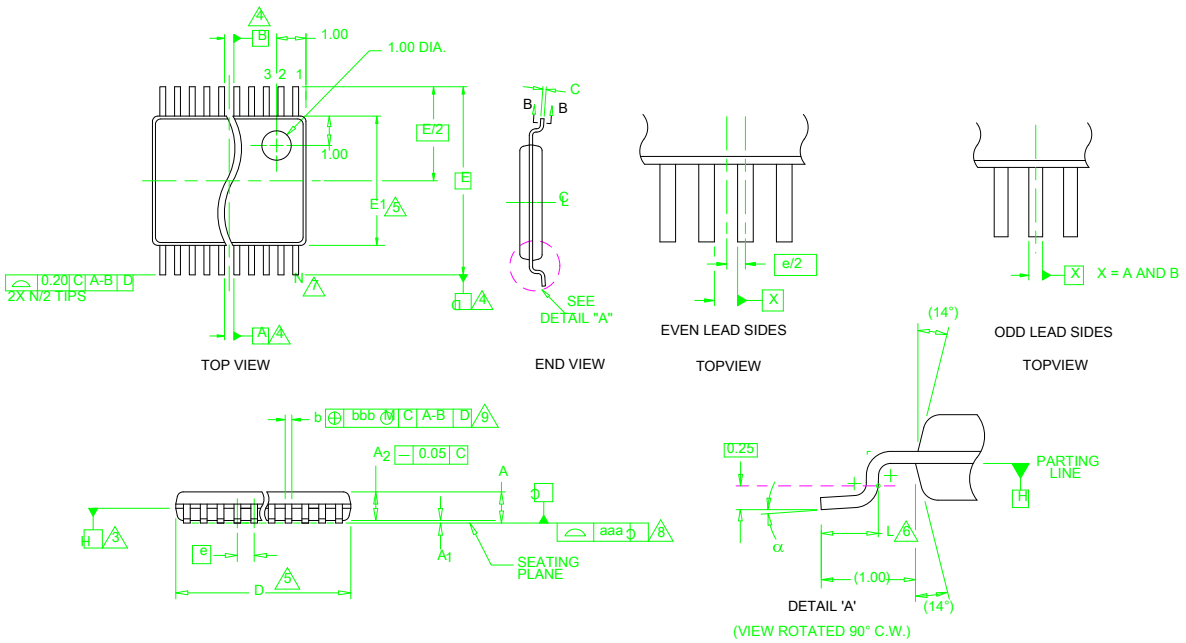
Figure 9 : Typical Schematic



The RC filter is composed of a capacitor (C) and resistor (R) implemented per example by a 2kΩ resistor and a 47 µF capacitor. The capacitor can be increased if needed.

12 Package Information

12.1 TSSOP-08/14

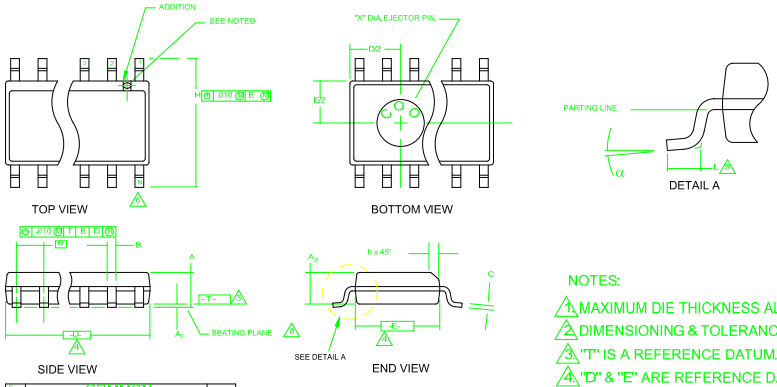


SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	5					7
	MIN.	NOM.	MAX.			D			P	P1	N
						MIN.	NOM.	MAX.	MAX.	MAX.	
A	——	——	1.10			2.90	3.00	3.10	1.59	3.2	8
A1	0.05	——	0.15			4.90	5.00	5.10	3.1	3.0	14
A2	0.85	0.90	0.95								
aaa		0.076									
b	0.19	-	0.30	9							
b1	0.19	0.22	0.25								
bbb		0.10									
c	0.09	-	0.20								
c1	0.09	0.127	0.16								
D	SEE VARIATIONS			5							
E1	4.30	4.40	4.50	5							
e	0.65 BSC										
E	6.40 BSC										
L	0.50	0.60	0.70	6							
N	SEE VARIATIONS			7							
P	SEE VARIATIONS										
P1	SEE VARIATIONS										
α	0°	——	8°								

ALL DIMENSIONS IN MILLIMETERS

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127
2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUM A-B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. "D" & "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D AND 0.25mm ON E PER SIDE.
6. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
9. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD SHOULD BE 0.07mm

12.2 SO-8

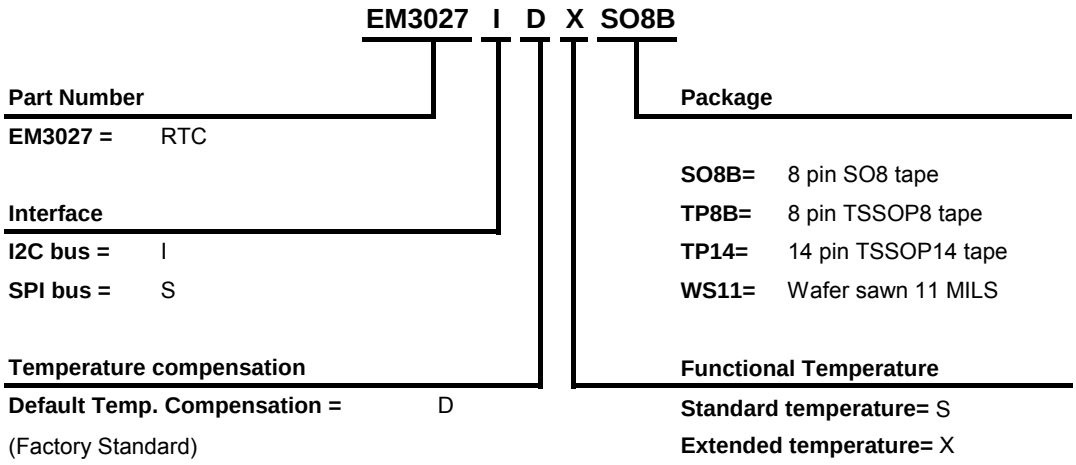


SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	1.55	1.63	1.73	
A1	0.127	0.15	0.25	
A2	1.40	1.47	1.55	
B	0.35	0.41	0.49	
C	0.19	0.20	0.25	
D	4.80	4.93	4.98	3
E	3.81	3.94	3.99	
e	1.27 BSC			
H	5.84	5.99	6.20	
h	0.25	0.33	0.41	
L	0.41	0.64	0.89	
N		8		5
α	0°	5°	8°	
X	2.16	2.36	2.54	

THIS TABLE IN MILLIMETERS

NOTES:
1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES AT END AND .010 INCHES AT WINDOW
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.

13 Ordering Information



Standard Versions

Part Number	Package	Functional Temperature	Interface	Delivery Form	Marking
EM3027IDSTP8A+	TSSOP8	-40 +85°C	I2C	Stick , 100 pcs	3027S5
EM3027IDSTP8B+	TSSOP8	-40 +85°C	I2C	Tape & Reel, 4000 pcs	3027S5
EM3027IDXTP8B+	TSSOP8	-40 +125°C	I2C	Tape & Reel, 4000 pcs	3027X5
EM3027IDSSO08A+	SO8	-40 +85°C	I2C	Stick, 97 pcs	3027S5
EM3027IDSSO08B+	SO8	-40 +85°C	I2C	Tape & Reel, 2500 pcs	3027S5
EM3027IDXSO08B+	SO8	-40 +125°C	I2C	Tape & Reel, 2500 pcs	3027X5
EM3027SDSTP14A+	TSSOP14	-40 +85°C	SPI	Stick, 96 pcs	3027S6
EM3027SDSTP14B+	TSSOP14	-40 +85°C	SPI	Tape & Reel, 3500 pcs	3027S6
EM3027SDXTP14B+	TSSOP14	-40 +125°C	SPI	Tape & Reel, 3500 pcs	3027X6

Please contact Sales office for other versions not shown here and for availability of non standard versions.