



Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, Ca 90638

Phone: (562) 404-7855 * Fax: (562) 404-1773

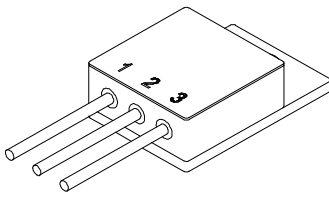
ssdi@ssdi-power.com * www.ssdi-power.com

SFF80N10M SFF80N10Z

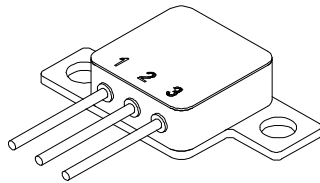
DESIGNER'S DATA SHEET

TO-254, TO254Z

Note 1: maximum current limited by package configuration



TO-254 (SFF85N10M)

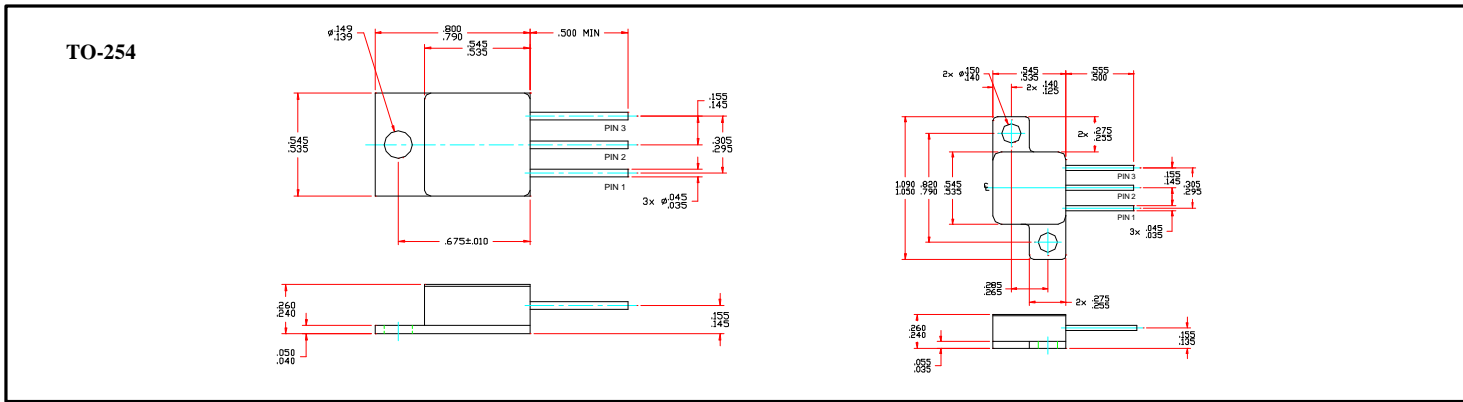


TO-254Z (SFF85N10Z)

**55 AMP (note 1) /100 Volts
12 mΩ
N-Channel Trench Gate MOSFET**

- Features:**
- Trench gate technology for high cell density
 - Lowest ON-resistance in the industry
 - Enhanced operating temperature range
 - Hermetically Sealed, Isolated Power Package
 - Low Total Gate Charge
 - Fast Switching
 - Enhanced replacement for IRM150
 - TX, TXV, S-Level screening available
 - Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings	Symbol	Value	Units
Drain - Source Voltage	V_{DSS}	100	V
Gate - Source Voltage	V_{GS}	±20	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	55 (note 1)
	@ $T_C = 125^\circ C$	I_{D2}	55 (note 1)
Max. Instantaneous Drain Current (T_j limited)	@ $T_C = 25^\circ C$	I_{D3}	110
	@ $T_C = 125^\circ C$	I_{D4}	70
Max. Avalanche current	@ $L = 0.1$ mH	I_{AR}	75
Repetitive Avalanche Energy	@ $L = 0.1$ mH	E_{AR}	280
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	250
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +200	°C
Maximum Thermal Resistance	Junction to Case	$R_{\theta JC}$	0.7 (typ 0.55)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0019A DOC



Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, Ca 90638

Phone: (562) 404-7855 * Fax: (562) 404-1773

ssdi@ssdi-power.com * www.ssdi-power.com

SFF80N10M SFF80N10Z

Electrical Characteristics ^{4/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	100	—	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 30A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 30A, T_j = 125^\circ C$ $V_{GS} = 10V, I_D = 30A, T_j = 200^\circ C$ $V_{GS} = 10V, I_D = 85A, T_j = 25^\circ C$	$R_{DS(on)}$	— — — —	9.5 16 22 10	12.0 — — —	mO
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	2.0	—	4.0	V
Gate to Source Leakage	$V_{GS} = \pm 20V$	I_{GSS}	—	—	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 80V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 80V, V_{GS} = 0V, T_j = 125^\circ C$ $V_{DS} = 80V, V_{GS} = 0V, T_j = 200^\circ C$	I_{DSS}	— — —	— — —	1 50 10	μA μA mA
Forward Transconductance	$V_{DS} = 15V, I_D = 30A, T_j = 25^\circ C$	g_{fs}	23	—	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	140	220	nC
Gate to Source Charge	$V_{DS} = 50V$	Q_{gs}	—	40	—	
Gate to Drain Charge	$I_D = 85A$	Q_{gd}	—	40	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	25	35	nsec
Rise Time	$V_{DS} = 50V$	t_r	—	115	185	
Turn off Delay Time	$I_D = 85A$	$t_{d(off)}$	—	75	110	
Fall Time	$R_G = 2.5O$	t_f	—	110	160	
Diode Forward Voltage	$I_F = 50A, V_{GS} = 0V$	V_{SD}	—	1.0	1.5	V
Diode Reverse Recovery Time	$I_F = 50A, di/dt = 100A/\mu sec$	t_{rr}	—	70	150	nsec
Peak Reverse Recovery Current		$I_{RM(rec)}$	—	5.5	10	A
Reverse Recovery Charge		Q_{rr}	—	0.2	0.35	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	8700	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	750	—	
Reverse Transfer Capacitance	$f = 1 MHz$	C_{rss}	—	450	—	

NOTES:

* Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

1/ For Ordering Information, Price, and Availability Contact Factory.

2/ Screening per MIL-PRF-19500.

3/ For Package Outlines Contact Factory.

4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO254	Pin 1	Pin 2	Pin 3
TO254Z	Pin 1	Pin 2	Pin 3

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0019A

DOC