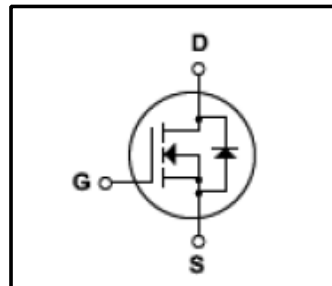
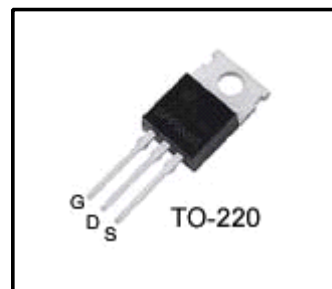


Silicon N-Channel MOSFET
Features

- 59A,100V, $R_{DS(on)}$ (Max 18m Ω)@ $V_{GS}=10V$
- Ultra-low Gate Charge(Typical 1180nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(175 $^{\circ}C$)


General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This device is specially well suited for switching regulators, switching converters, motor and relay drivers, and drivers for high power bipolar switching transistor demanding high speed and low gate drive power.


Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	100	V
I_D	Continuous Drain Current(@ $T_c=25^{\circ}C$)	59	A
	Continuous Drain Current(@ $T_c=100^{\circ}C$)	42	A
I_{DM}	Drain Current Pulsed (Note1)	240	A
V_{GS}	Gate to Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note2)	170	mJ
E_{AR}	Repetitive Avalanche Energy (Note1)	7.4	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	5.8	V/ ns
P_D	Total Power Dissipation(@ $T_c=25^{\circ}C$)	136	W
	Derating Factor above 25 $^{\circ}C$	1.3	W/ $^{\circ}C$
T_J, T_{stg}	Junction and Storage Temperature	-55~150	$^{\circ}C$
T_L	Maximum lead Temperature for soldering purposes	300	$^{\circ}C$

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance , Junction -to -Case	-	-	0.92	$^{\circ}C/W$
R_{QCS}	Thermal Resistance , Case-to-Sink	-	0.5	-	$^{\circ}C/W$
R_{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	62.5	$^{\circ}C/W$

Electrical Characteristics(Tc=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA	
Gate-source breakdown voltage	V _{(BR)GSS}	I _G =±10 μA,V _{DS} =0V	±30	-	-	V	
Drain cut -off current	I _{DSS}	V _{DS} =100V,V _{GS} =0V	-	-	20	μA	
Drain -source breakdown voltage	V _{(BR)DSS}	I _D =250 μA,V _{GS} =0V	100	-	-	V	
Break voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D =1mA, Referenced to 25°C	-	0.1	-	V/°C	
Gate threshold voltage	V _{GS(th)}	V _{DS} =10V,I _D =250 μA	2	-	4	V	
Drain -source ON resistance	R _{DS(ON)}	V _{GS} =10V,I _D =35A	-	-	18	mΩ	
Forward Transconductance	g _{fs}	V _{DS} =50V,I _D =35A	-	35	-	S	
Input capacitance	C _{iss}	V _{DS} =25V,	-	2990	-	pF	
Reverse transfer capacitance	C _{rss}	V _{GS} =0V,	-	160	-		
Output capacitance	C _{oss}	f=1MHz	-	3000	-		
Switching time	Rise time	t _r	V _{DD} =28V, I _D =75A, R _G =6.8Ω, (Note4,5)	-	18	-	ns
	Turn-on time	t _{on}		-	86	-	
	Fall time	t _f		-	47	-	
	Turn-off time	t _{off}		-	60	-	
Total gate charge(gate-source plus gate-drain)	Q _g	V _{DD} =80V, V _{GS} =10V,	-	1180	-	nC	
Gate-source charge	Q _{gs}	I _D =35A	-	190	-		
Gate-drain("miller") Charge	Q _{gd}	(Note4,5)	-	300	-		

Source-Drain Ratings and Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	-	-	-	59	A
Pulse drain reverse current	I _{DRP}	-	-	-	240	A
Forward voltage(diode)	V _{DSF}	I _S =35A,V _{GS} =0V	-	-	1.5	V
Reverse recovery time	t _{rr}	I _{DR} =75A,V _{DD} =25V,	-	56	75	ns
Reverse recovery charge	Q _{rr}	di _{DR} / dt =100 A / μs	-	106	160	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=50μH I_{AS}=59A,V_{DD}=50V,R_G=25Ω , Starting T_J=25°C

3.I_{SD}≤59A,di/dt≤300A/us,V_{DD}<BV_{DSS},STARTING T_J=25°C

4.Pulse Test:Pulse Width≤300us,Duty Cycle≤2%

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

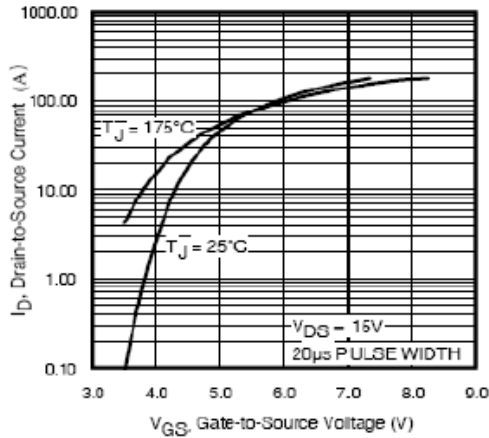


Fig.1 On -State Characteristics

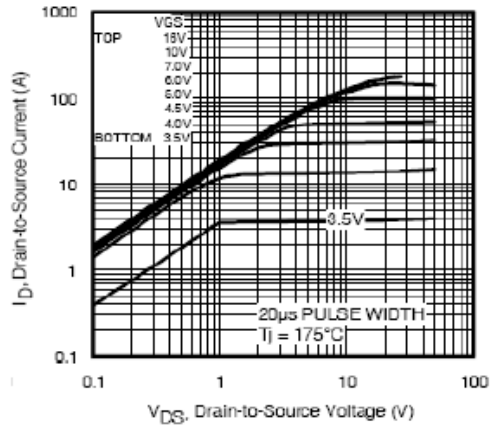


Fig.2 Typical Output Characteristics

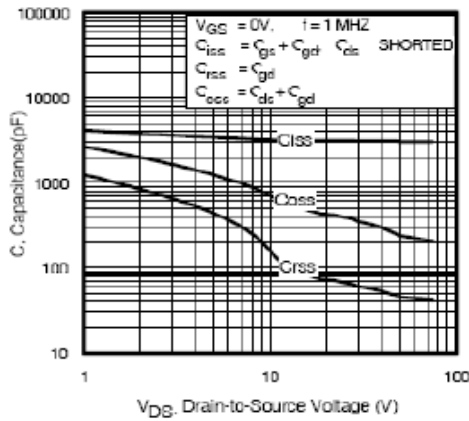


Fig.3 Typical Capacitance vs Drain Current

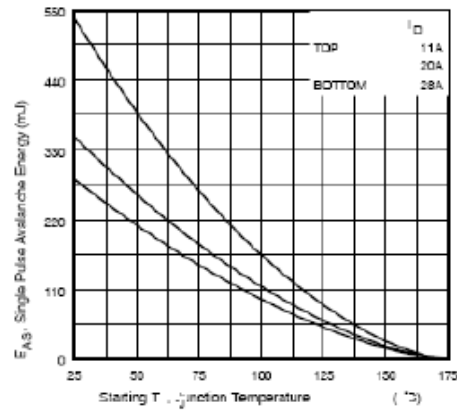


Fig.4 Maximum Avalanche Energy vs Drain Current

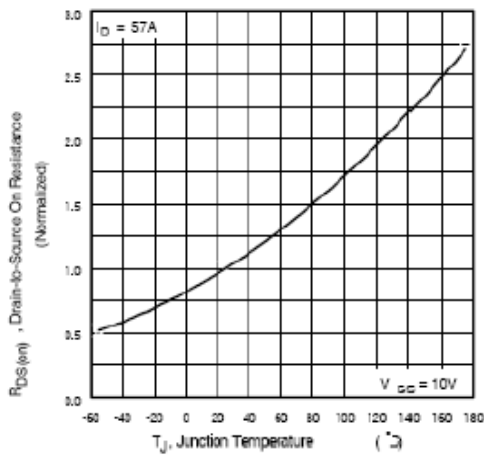


Fig.5 On-Resistance Variation vs Junction Temperature

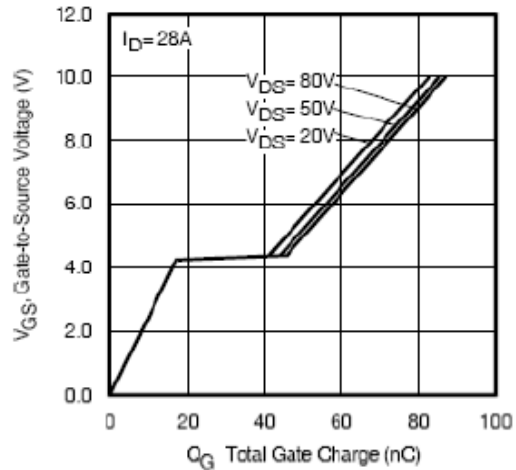


Fig.6 Gate charge Characteristics

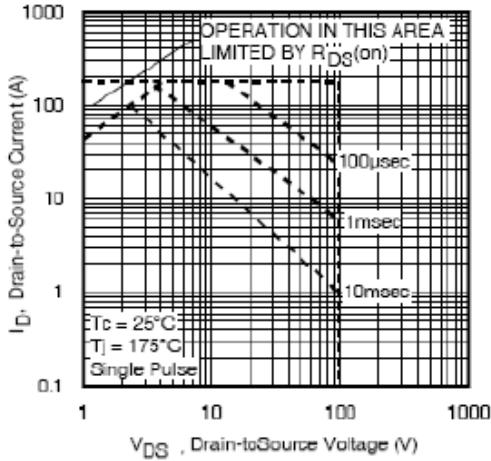


Fig.7 Maximum Safe Operation Area

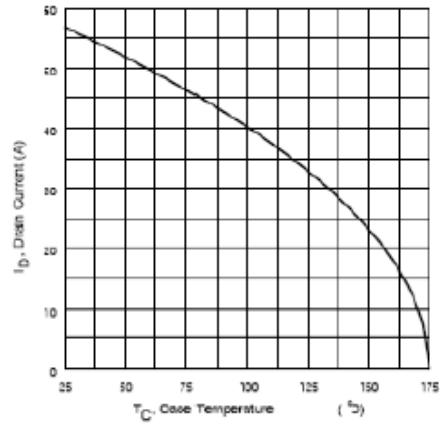


Fig.8 Maximum Drain current vs Case Temperature

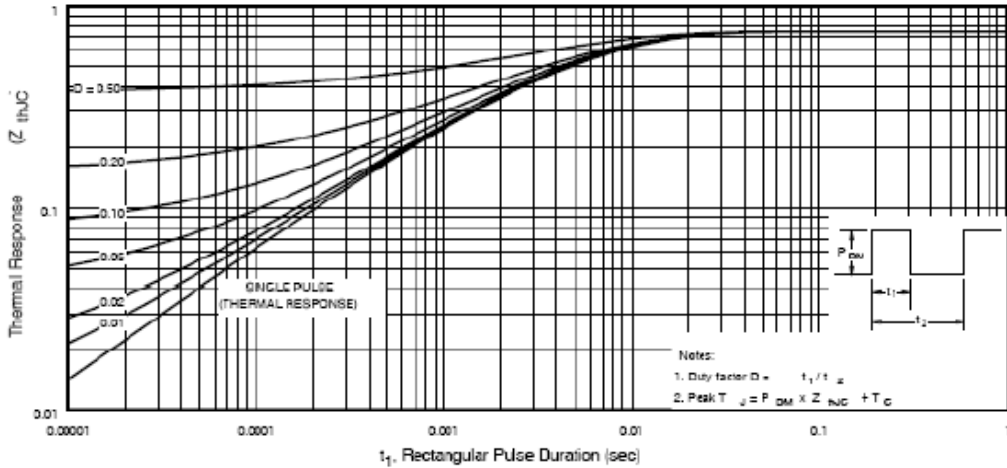


Fig.9 Transient Thermal Response Curve

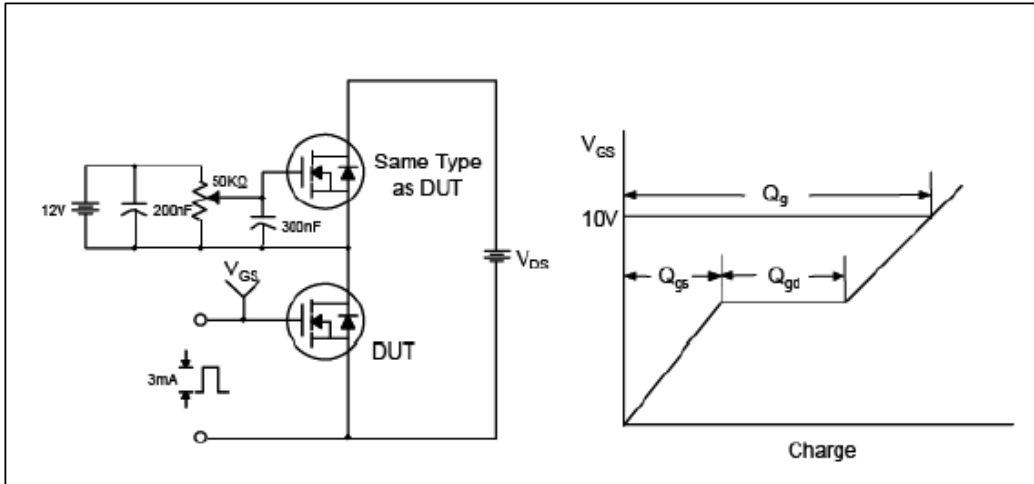


Fig.10 Gate Test circuit & Waveform

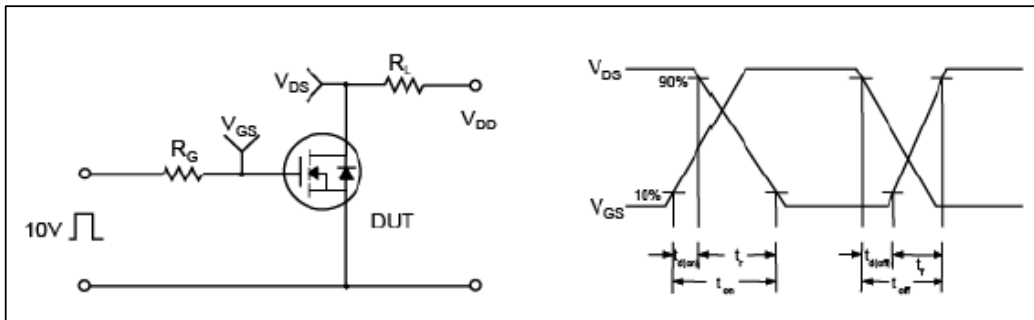


Fig.11 Resistive Switching Test Circuit & Waveform

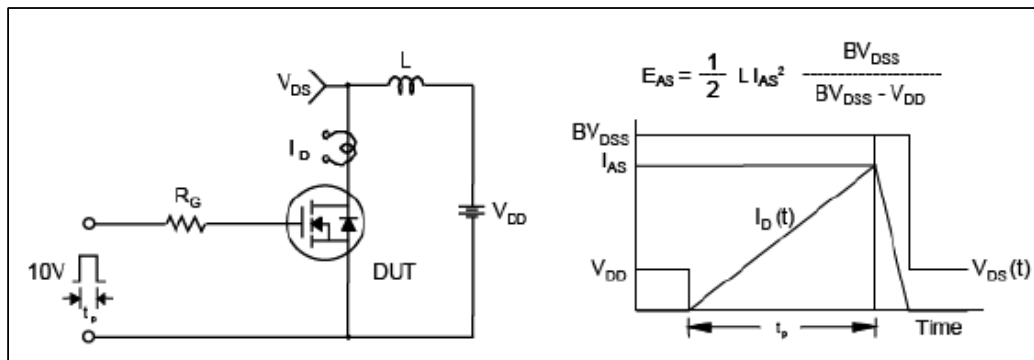


Fig.12 Uncamped Inductive Switching Test Circuit & Waveform

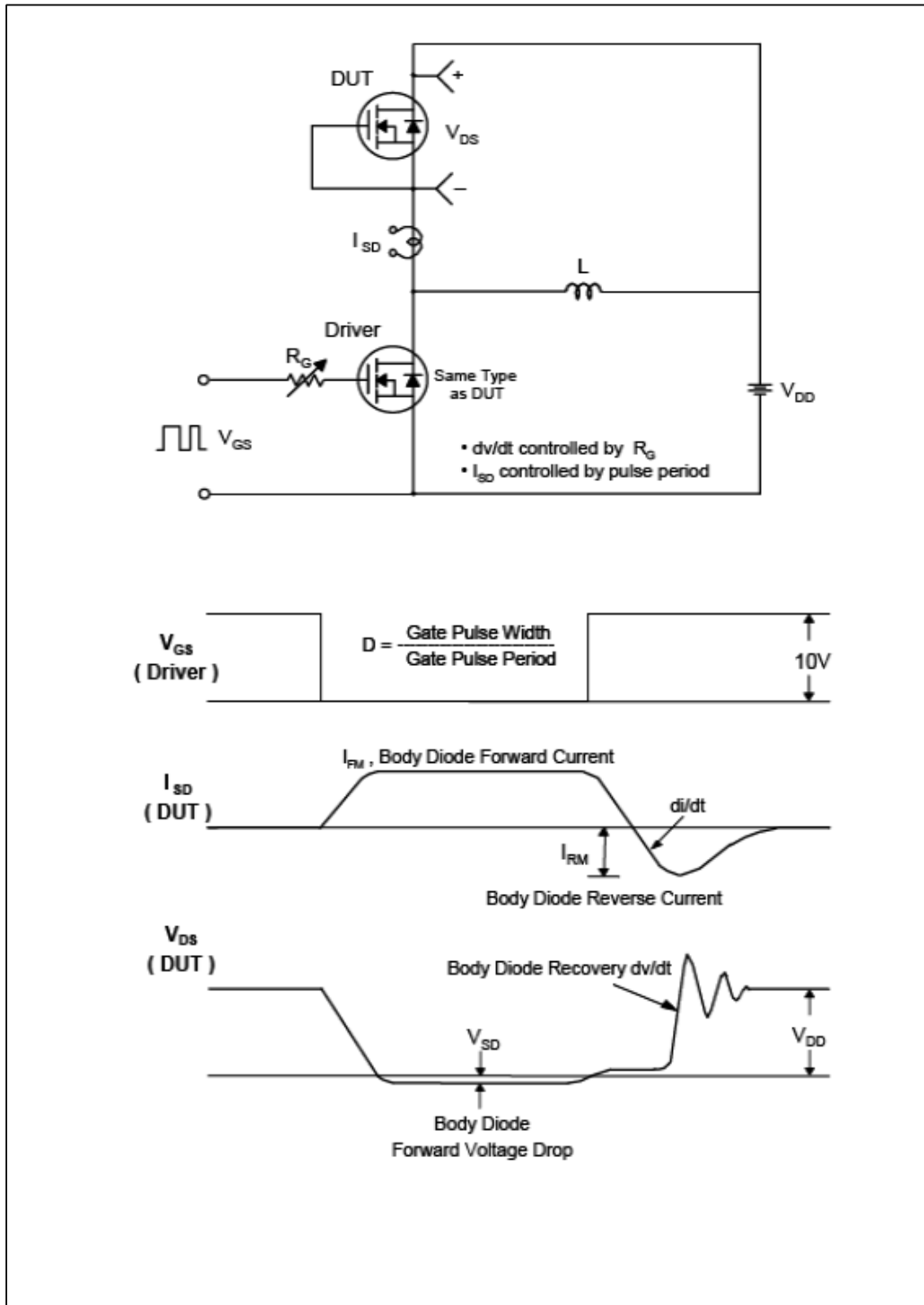


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-220 Package Dimension

