MN86075

Facsimile Image-Processing IC

■ Overview

The MN86075 is a facsimile image-processing IC that receives the analog signal from an image sensor, which performs a wide range of signal-processing operations on that data to create images with enhanced quality. The MN86075 reproduces high-quality images by applying 64-level halftone processing and two-dimensional MTF correction.

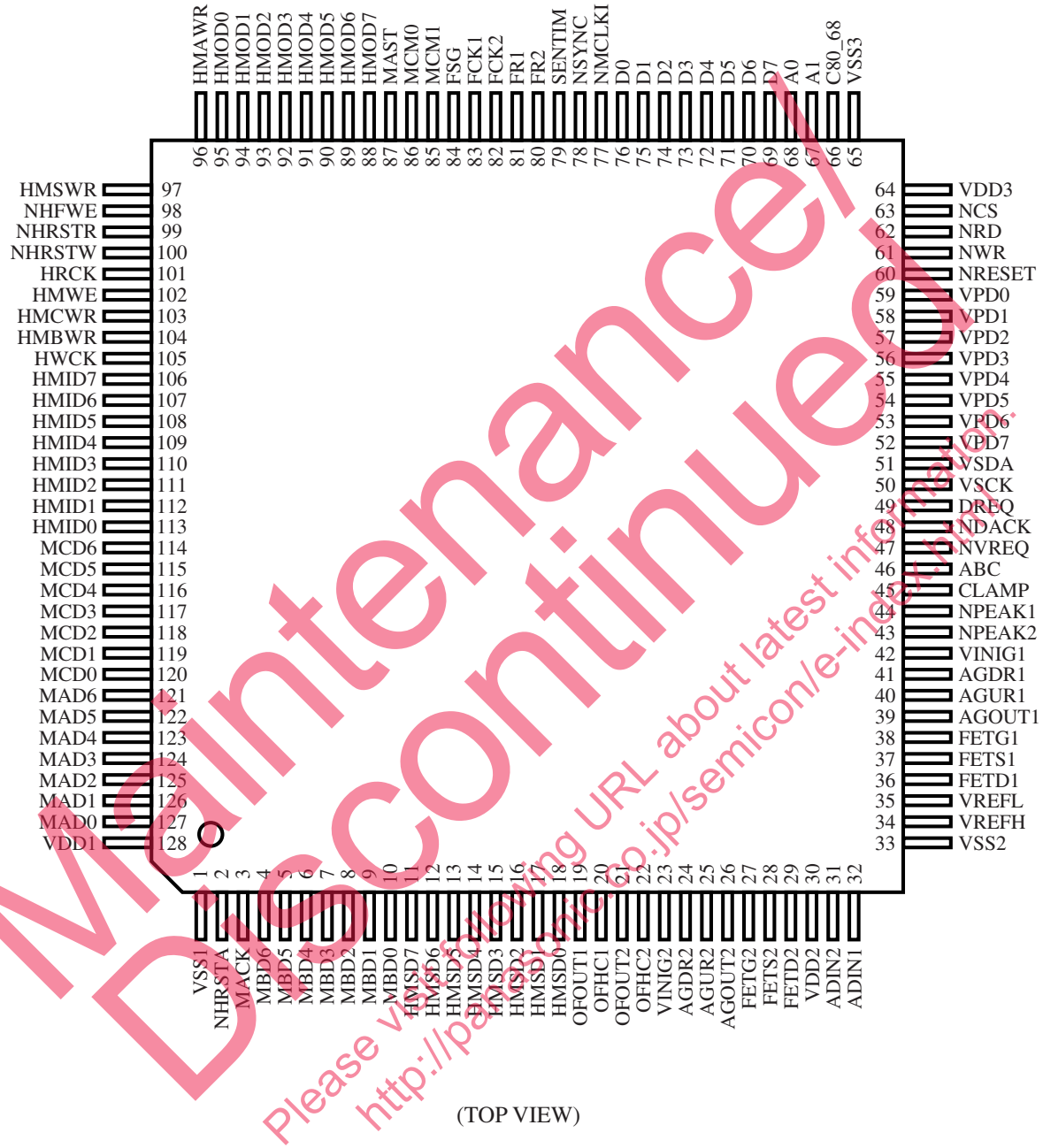
■ Features

- Image processing for high-quality image reproduction
  - Both white and black shading correction for all pixels
  - Error diffusion processing to reproduce 64-level halftone images
    Arbitrary gamma curves can be set up.
  - Two-dimensional MTF correction for text enhancement
  - Multivalued smoothing removes jagged edges of slanted lines due to magnification and resolution conversion.
  - Enlargement and reduction (line density conversion) without Moire patterns and with arbitrary magnification factors.
- Implements the high processing speed of 0.5 ms/line for A3 size at 400 dpi at an image-processing clock frequency of 12.5 MHz.
- Integrates offset correction, gain correction, and 8-bit A/D converter analog signal-processing circuits on the same chip.
- Generates drive signals for all major image sensor types (CCD and CIS).
- Provides an extensive set of memory interface functions to support a wide range of applications.
  - Standard G3 (L mode) fax (200 dpi, 1.5 ms/line)
    B4 size document image acquisition: 64K SRAM (64k-bit) × 1
    A3 size document image acquisition: pseudo SRAM (256k-bit) × 1
  - High-speed G3 (M mode) fax (200 dpi, 0.6 ms/line)
    B4 or A3 size document image acquisition: SRAM (64k-bit) × 2
  - High-resolution G3 (M mode) fax (400 dpi, 1.2 ms/line)
    B4 size document image acquisition: SRAM (64k-bit) × 2
    A3 size document image acquisition: SRAM (64k-bit) × 2 + SRAM (16k-bit) × 2 or SRAM (256k-bit) × 2
  - Ultrahigh-speed G4 (H mode) fax (400 dpi, 0.5 ms/line)
    B4 or A3 size document image acquisition: SRAM (64k-bit) × 4 + FIFO (5k × 8-bit) × 1
- 5 V single-voltage power supply

■ Applications

- Image acquisition and processing for facsimile and image scanner

■ Pin Arrangement (H mode)



(TOP VIEW)

Note) The above pin-arrangement shows a pin-name of H mode, that is often utilized compared with other modes.

■ Pin Descriptions

1. Mode description (3 pins)

Pin Name	I/O	Pin No.	Function
MAST	I	87	Clock period selection High: Master mode In master mode, the IC operates in synchronization with the internal SYNC signal. The internal SYNC signal is output from the NSYNC pin. Low: Slave mode In slave mode, the IC operates in synchronization with the external SYNC signal. The external SYNC signal is input to the NSYNC pin.
MCM0 MCM1	I I	86 85	Memory interface selection The levels applied to these pins select the memory interface pin functions. The master clock (NMCLKI pin input) frequency conditions are selected by the under table.

MAST	MCM1	MCM0	Memory interface mode	Clock mode
Low	Low	Low	L mode	Slave $f_{CKVD} \times 16$
Low	Low	High	M mode	Slave $f_{CKVD} \times 8$
Low	High	Low	H mode	Slave $f_{CKVD} \times 2$
Low	High	High	T mode	Slave $f_{CKVD} \times 2$
High	Low	Low	L mode	Master $f_{CKVD} \times 16$
High	Low	High	M mode	Master $f_{CKVD} \times 8$
High	High	Low	H mode	Master $f_{CKVD} \times 2$
High	High	High	DCTEST	—

L Mode (Low-speed mode)
Memory organization: Pseudo SRAM (256K) × 1 or SRAM (256 K) × 1
Recommended image signal frequency (f_{CKVD}): 2.0 MHz (maximum)
Master clock frequency (f_{MCLKI}): $f_{CKVD} \times 16$

M Mode (Medium-speed mode)
Memory organization: SRAM (64K) × 3 or
SRAM (64K) × 2 (no black correction or enlargement processing)
Recommended image signal frequency (f_{CKVD}): 4.0 MHz (maximum)
Master clock frequency (f_{MCLKI}): $f_{CKVD} \times 8$

H Mode (High-speed mode)
Memory organization: SRAM (64K) × 4 plus FIFO (5K × 8-bit) × 1
Recommended image signal frequency (f_{CKVD}): 12.5 MHz (maximum)
Master clock frequency (f_{MCLKI}): $f_{CKVD} \times 2$

T Mode (Test data input mode)
Inputs data used to test the internal IC functions.
Master clock frequency (f_{MCLKI}): $f_{CKVD} \times 2$

■ Pin Descriptions (continued)

1. Mode description (3 pins) (continued)

Pin Name	I/O	Pin No.	Function
MCM0 MCM1 (continued)	I I	86 85	DCTEST Mode Sets the output pins and the I/O pins to the DC test mode.

HMID0	HMID1	DC test function
0	*	Output high-impedance test
1	0	Output low test
1	1	Output high test

*: Don't care

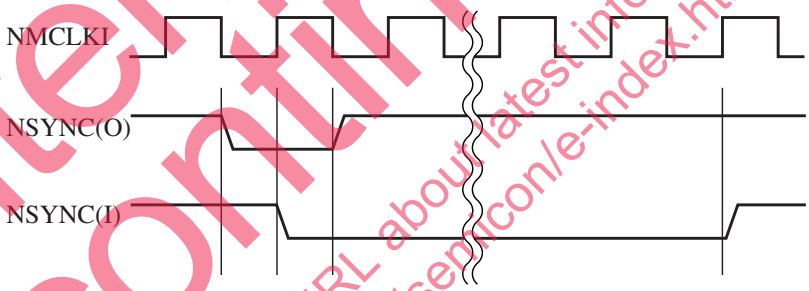
2. System interface pins (15 pins)

Pin Name	I/O	Pin No.	Function
D0 to D7	I/O	76 to 69	CPU data bus I/O
A0 A1	I	68 67	CPU address input
NCS	I	63	CPU chip select input
NWR(DS)	I	61	CPU data write input (C80 to C68 pin: High) CPU data strobe input (C80 to C68 pin: Low)
NRD(R/W)	I	62	CPU data read input (C80 to C68 pin: High) CPU data read/write input (C80 to C68 pin: Low)
C80 to C68	I	66	CPU selection Low: 68000 family CPU High: 80x86 family CPU
NRESET	I	60	System reset input

■ Pin Descriptions (continued)

3. Clock Pins (2 pins)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>NMCLKI</td><td>I</td><td>77</td><td>Master clock input
Clock frequency:
Image signal frequency × 2 (memory interface mode H)
Image signal frequency × 8 (memory interface mode M)
Image signal frequency × 16 (memory interface mode L)
Clock duty: 50 %</td></tr>
<tr><td>NSYNC</td><td>I/O</td><td>78</td><td>Clock period signal I/O

Line 1 start timing pulse
<table>
<tr><th>MAST</th><th>SYSL (TIM2_REG)</th><th></th></tr>
<tr><td>Low</td><td>*</td><td>SYNC input</td></tr>
<tr><td>High</td><td>1</td><td>SYNC output</td></tr>
</table>
*: Don't care

</td></tr>
<tr><td>NMCLKO</td><td>O</td><td></td><td>Internal master clock output
Outputs the internal master clock (the NMCLKI pin input).
<table>
<tr><th>MAST</th><th>SYSL (TIM2_REG)</th><th></th></tr>
<tr><td>High</td><td>0</td><td>MCLK output</td></tr>
</table></td></tr>
</table>

■ Pin Descriptions (continued)

4. Sensor Interface Pins (6 pins)

Pin Name	I/O	Pin No.	Function
FCK1	O	83	CCD : 1 (TIM1 REG) Reduced CCD sensor ϕ1 clock: CKVD1/2
SCLK	O		CCD : 0 (TIM1 REG) CdS or bipolar sensor SCLK clock: NCKVD
FCK2	O	82	CCD : 1 (TIM1 REG) Reduced CCD sensor ϕ2 clock: CKVD1/2
NSCLK	O		CCD : 0 (TIM1 REG) CdS, Bipolar sensor SCLK clock: CKVD
FSG	O	84	CCD : 1, CONTA : ∗ (TIM1 REG) Reduced CCD sensor ϕSG
ST	O		CCD : 0, CONTA : 0 (TIM1 REG) Bipolar sensor ST (Start pulse)
NSTPL	O		CCD : 0, CONTA : 0 (TIM1 REG) CdS sensor STPL (Start pulse)
FR1	O	81	FRM2 : 0 Reduced CCD sensor ϕR1 clock (Parallel mode) FRM2 : 1 Reduced CCD sensor ϕR clock (Serial mode)
FR2	O	80	FRM2 : 0 Reduced CCD sensor ϕR2 clock (Parallel mode) FRM2 : 1 Reduced CCD sensor ϕSP clock (Serial mode)
SENTIM	O	79	Sensor timing output

STM1 (TIM2 REG)	STM0 (TIM2 REG)	SETIM output signal
0	0	Offset enable
0	1	ABC enable
1	0	Arbitrary timing (All readout lines)
1	1	Arbitrary timing (Valid lines only)

Note) ∗: Don't care

■ Pin Descriptions (continued)

5. Sensor Drive Pins (4 pins)

Pin Name	I/O	Pin No.	Function
NPEAK1	O	44	Gain control signal 1 (Overflow 1) Low: Gain reduced. High: Gain increased.
NPEAK2	O	43	Gain control signal 2 (Overflow 2) Low: Gain reduced. High: Gain increased.
CLAMP	O	45	Clamp (offset correction) period signal Low: Hold High: Sample (Offset adjustment operation)
ABC	O	46	Valid ABC period signal Low: Gain held High: Gain adjustment

6. Image Bus Interface Pins (5 pins)

Pin Name	I/O	Pin No.	Function
NVREQ	I	47	Video request Inputs image data transfer requests from the control device. Low: Transfer requests enabled High: Transfer requests disabled In trigger scan mode, when this pin is set low, the sensor start signal (STPL) goes low and a sensor readout operation starts. Then, one line of image processing is performed and the image data is output from the VSDA pin. In cycle scan mode, when this pin is set low, the next readout line is taken to be valid, one line of image processing is performed, and the image data is output from the VSDA pin. In free scan mode, the state of this pin is ignored. Sensor readout is started at the period specified for the timing, the image processing for each line is performed, and the data is output from the VSDA pin.
DREQ	O	49	Parallel mode IPARA: 1 (IBCNT REG) Parallel data send request Low: Send requests disabled. High: Send requests enabled.
NVSEN	O		Serial mode IPARA: 0 (IBCNT REG) Video enable Low: Image data valid period High: Image data invalid period
NDACK	I	48	Parallel data acknowledge input Data send acknowledge signal for DREQ Low: Data send acknowledge enable High: Data send acknowledge disable

■ Pin Descriptions (continued)

6. Image Bus Interface Pins (5 pins) (continued)

Pin Name	I/O	Pin No.	Function
VSCK	O	50	Parallel mode IPARA: 1 (IBCNT REG) Video serial clock (External circuit support signal)  VSDA data acquisition timing
NVSCK	O		Serial mode IPARA: 0 (IBCNT REG) Video serial clock  VSDA data acquisition timing
VSDA	O	51	Parallel mode IPARA: 1 (IBCNT REG) Video serial data (External circuit support signal) Output for two-valued image data Low: white, high: black
NVSDA	O		Serial mode IPARA: 0 (IBCNT REG) Video serial data Output for two-valued image data Low: black, high: white

7. Parallel I/O Pins (8 pins)

Pin Name	I/O	Pin No.	Function
VADD7	I	52	PSD2 : 0, PSD1 : 0, PSD0 : ∗ (IBCNT REG) External A/D converter signal input
NHROCS	O		PSD2 : 0, PSD1 : 1, PSD0 : ∗ (IBCNT REG) Shading ROM chip select
VPD7	O/Hi-Z		PSD2 : 1, PSD1 : 0, PSD0 : 0 (IBCNT REG) Two-valued parallel image output (parallel interface) NDACK: low: Output mode NDACK: high: High impedance
VSCD7	O		PSD2 : 1, PSD1 : 0, PSD0 : 1 (IBCNT REG) Shading correction image signal output
CKVG	O		PSD2 : 1, PSD1 : 1, PSD0 : 0 (IBCNT REG) Multivalued image signal period clock output
SBUS7	O		PSD2 : 1, PSD1 : 1, PSD0 : 1 (IBCNT REG) Internal DBUS data output

Note) ∗: Don't care

■ Pin Descriptions (continued)

7. Parallel I/O Pins (8 pins) (continued)

Pin Name	I/O	Pin No.	Function
VADD6	I	53	PSD2 : 0, PSD1 : 0, PSD0 : ∗ (IBCNT REG) External A/D converter signal input
HKWR	O		PSD2 : 0, PSD1 : 1, PSD0 : 0 (IBCNT REG) HMKD read/write output
VPD6	O/Hi-Z		PSD2 : 1, PSD1 : 0, PSD0 : 0 (IBCNT REG) Two-valued parallel image signal output (parallel interface) NDACK: low: Output mode NDACK: high: High impedance
VSCD6	O		PSD2 : 1, PSD1 : 0, PSD0 : 1 (IBCNT REG) Shading correction image signal output
VGSD6	O		PSD2 : 1, PSD1 : 1, PSD0 : 0 (IBCNT REG) Multivalued image signal output
SBUS6	O		PSD2 : 1, PSD1 : 1, PSD0 : 1 (IBCNT REG) Internal DBUS data output
VADD5	I	54	PSD2 : 0, PSD1 : 0, PSD0 : ∗ (IBCNT REG) External A/D converter signal input
NHRSTK	O		PSD2 : 0, PSD1 : 1, PSD0 : ∗ (IBCNT REG) Black shading external address counter clear
VPD5	O/Hi-Z		PSD2 : 1, PSD1 : 0, PSD0 : 0 (IBCNT REG) Two-valued parallel image signal output (parallel interface) NDACK: low: Output mode NDACK: high: High impedance
VSCD5	O		PSD2 : 1, PSD1 : 0, PSD0 : 1 (IBCNT REG) Shading correction image signal output
VGSD5	O		PSD2 : 1, PSD1 : 1, PSD0 : 0 (IBCNT REG) Multivalued image signal output
SBUS5	O		PSD2 : 1, PSD1 : 1, PSD0 : 1 (IBCNT REG) Internal DBUS data output
VADD4 to VADD0	I	55 to 59	PSD2 : 0, PSD1 : 0, PSD0 : ∗ (IBCNT REG) External A/D converter signal input
HMKD4 to HMKD0	I/O		PSD2 : 0, PSD1 : 1, PSD0 : ∗ (IBCNT REG) Black shading correction data input and output HKWR: low: Input HKWR: high: Output
VPD4 to VPD0	O/Hi-Z		PSD2 : 1, PSD1 : 0, PSD0 : 0 (IBCNT REG) Two-valued parallel image signal output (parallel interface) NDACK: low: Output mode NDACK: high: High impedance
VSCD4 to VSCD0	O		PSD2 : 1, PSD1 : 0, PSD0 : 1 (IBCNT REG) Shading correction image signal output

Note) ∗: Don't care

■ Pin Descriptions (continued)

7. Parallel I/O Pins (8 pins) (continued)

Pin Name	I/O	Pin No.	Function
VGSD4 to VGSD0	O	55 to 59 (continued)	PSD2 : 1, PSD1 : 0, PSD0 : 0 (IBCNT REG) Multivalued image signal output
SBUS4 to SBUS0	O		PSD2 : 1, PSD1 : 1, PSD0 : 1 (IBCNT REG) Internal DBUS data output

Note) (1) VPD0 to VPD7
1: Black - Data direction: MSB first
0: White
(2) VGSD0 to VGSD7
FF: White to 00: Black
(3) VGSD0 to VGSD6
7F: White to 00: Black
(4) VADD0 to VADD7
FF: White to 00: Black

8. Memory Interface Pins (57 pins)

Mode pins: MCM0, MCM1

The function is selected by RSH, MAG, STK, and EXSCD in the memory control register (MECR)

Mode	Mode pins		MECR		Image-processing function			Other items
	MCM1	MCM0	RSH	MAG	Shading: White correction	Shading: Black correction	Enlargement processing	
L	Low	Low	0	0	●	×	×	Image signal frequencies Maximum: 625 kHz to 2.0 MHz STK (Memory selection) 0: SRAM or PSRAM 1: PSRAM EXSCD † 0: Internal SCD processing 1: External SCD input
			0	1	●	●	●	
			1	0	ROM Fixed	×	×	
			1	1	ROM Fixed	●	●	
M	Low	High	0	✻	●	●	●	Image signal frequencies Maximum: 4.0 MHz EXSCD † 0: Internal SCD processing 1: External SCD input STK: ✻ A system structure using only two SRAMs is possible if black correction and enlargement processing are not used.
			1	1	ROM Fixed	●	●	

Note) ● : can be performed
× : can not be performed
† : SCD: Shading-corrected data
✻ : Don't care

■ Pin Descriptions (continued)

8. Memory Interface Pins (57 pins) (continued)

Mode	Mode pins		MECR		Image-processing function			Other items
	MCM1	MCM0	RSH	MAG	Shading: White correction	Shading: Black correction	Enlargement processing	
H	High	High	*	*	●	●	●	Image signal frequencies Maximum: 12.5 MHz EXSCD † 0: Internal SCD processing 1: External SCD input STK : *
					ROM Fixed			

Note) ● : can be performed
† : SCD: Shading-corrected data
* : Don't care

8.1. L Mode

Pin Name	I/O	Pin No.	Function
LMXD0 to LMXD7	I/O	18 to 11	RAM data I/O I/O of white shading data, black shading data, error diffusion processing error data, and two-line image data.
LMA0 to LMA7	O	95 to 88	RAM address
LMA8		97	
LMA9		96	
LMA10		104	
LMA11		103	
LMA12		102	
LMA13		2	
LMA14		105	
NLMOE	O	99	RAM OE control
NLMWE	O	100	RAM WE control
NLMCE	O	101	Pseudo SRAM CS control
LSID0 to LSID7	I	103 to 106	White shading ROM data input or external shading-corrected data input.
NLROE	O	98	White shading ROM OE control
NLRWE	O	4	EEROM WE control
LRA10 to LRA12	O	116 to 114	EEROM address high-order bits (LMA0:9 are used for the low-order bits of the address.)
LAP0 to LAP6	O	127 to 121	Output port A (8 bits)
LAP7		10	
LBP0 to LBP4	O	9 to 5	Output port B (8 bits)
LBP5		120	
LBP6		119	
LBP7		118	

■ Pin Descriptions (continued)

8.2. M Mode

Pin Name	I/O	Pin No.	Function
MMED0 to MMED7	I/O	18 to 11	RAM data I/O White shading data and error diffusion processing error data
MMFD0 to MMFD6 MMFD7	I/O	127 to 121 10	RAM data I/O Black shading data and error diffusion processing error data (for enlargement)
MMLD0 to MMLD6	I/O	120 to 114	RAM data I/O Input and output of two-line image data
MSID0 to MSID7	I	113 to 106	White shading ROM data input or external shading-corrected data input
MMA0 to MMA7 MMA8 MMA9 MMA10 to MMA12 MMA13	O	95 to 88 97 96 104 to 102 6	RAM address
MSA0 MSA1	O	2 105	RAM address high-order bits
NMMEWE NMMFWE NMMLWE	O	101 100 99	RAM WE control
NMMOE	O	98	RAM OE control
NMROE	O	5	White shading ROM and EEROM OE control
NMRWE	O	4	EEROM WE control
MBP0 to MBP2	O	9 to 7	Output port B (3 bits)

8.3. H Mode

Pin Name	I/O	Pin No.	Function
HMSD0 to HMSD7	I/O	18 to 11	RAM data I/O White shading data
MMAD0 to MMAD6	I/O	127 to 121	RAM data I/O Input and output of single-line image data
MMBD0 to MMBD6	I/O	10 to 4	RAM data I/O Input and output of single-line image data
MMCD0 to MMCD6	I/O	120 to 114	RAM data I/O Input and output of single-line image data
HMID0 to HMID7	I	113 to 106	FIFO data input Error diffusion processing error data
HMOD0 to HMOD7	O	95 to 88	FIFO data output Error diffusion processing error data

■ Pin Descriptions (continued)

8.3. H Mode (continued)

Pin Name	I/O	Pin No.	Function
HMSWR HMAWR HMBWR HMCWR	O	97 96 104 103	RAM OE control
HMWE	O	102	RAM WE control (Requires a NAND gate.)
HWCK	O	105	FIFO WCK
HRCK	O	101	FIFO RCK
NHRSTW	O	100	FIFO RSTW
NHRSTR	O	99	FIFO RSTR
NHFWE	O	98	FIFO WE
MACK	O	3	RAM address counter clock
NHRSTA	O	2	RAM address counter clear

9. Analog Pins (20 pins)

Pin Name	I/O	Pin No.	Function
ADIN1 ADIN2	I I	32 31	A/D converter inputs • Serial mode - ADPARA: 0 (ADOFS REG = SHA3) ADIN1: Image signal input ADIN2: Unused (Must be connected to AVSS.) • Parallel mode - ADPARA: 1 (ADOFS REG = SHA3) ADIN1: Odd image signal input ADIN2: Even image signal input
FETD1	O	36	FET 1 drain
FETG1	I	38	FET 1 gate
FETS1	O	37	FET 1 source
FETD2	O	29	FET 2 drain
FETG2	I	27	FET 2 gate
FETS2	O	28	FET 2 source
AGOUT1	O	39	Gain control circuit 1 - Output
AGUR1	O	40	Gain control circuit 1 - Gain increasing resistor connection
AGDR1	O	41	Gain control circuit 1 - Gain reducing resistor connection
VINIG1	O	42	Gain control circuit 1 - Initialization control
AGOUT2	O	26	Gain control circuit 2 - Output
AGUR2	O	25	Gain control circuit 2 - Gain increasing resistor connection
AGDR2	O	24	Gain control circuit 2 - Gain reducing resistor connection
VINIG2	O	23	Gain control circuit 2 - Initialization control

■ Pin Descriptions (continued)

9. Analog Pins (20 pins) (continued)

Pin Name	I/O	Pin No.	Function
OFHC1	O	20	Offset control circuit 1 - Capacitor connection 1
OFHC2	O	22	Offset control circuit 2 - Capacitor connection 2
OFOUT1	O	19	Offset control circuit 1 - Source follower output 1
OFOUT2	O	21	Offset control circuit 2 - Source follower output 2

■ Electrical Characteristics

1. Absolute Maximum Ratings at V_{SS}† = 0.0 V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	− 0.3 to +7.0	V
Input voltage	V_{in}	V_{SS}− 0.3 to V_{DD}+0.3	V
Output voltage	V_o	V_{SS}− 0.3 to V_{DD}+0.3	V
Input/output voltage	V_{in}	V_{SS}− 0.3 to V_{DD}+0.3	V
	V_o	V_{SS}− 0.3 to V_{DD}+0.3	V
Analog voltage	V_A	V_{SS}− 0.3 to V_{DD}+0.3	V
Power dissipation	P_T	750	mW
Operating temperature	T_{OP}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note) 1. †: In the following, V_{SS} indicates the voltage applied to V_{SS}, and V_{DD} indicates the voltage applied to V_{DD}. Each of the power supply pins must be connected to V_{DD} or V_{SS}.

2. The absolute maximum ratings are limiting values under which the chip will not be destroyed. Operation is not guaranteed within these ranges.

2. Operating Conditions at V_{SS} = 0.0 V, V_{DD} = 4.75 V to 5.25 V, T_a = 0°C to 70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
External clock frequency						
Clock frequency	f_{CP}	H mode	—	—	25	MHz
		M mode	—	—	32	
		L mode	—	—	32	

■ Electrical Characteristics (continued)

3. DC Characteristics at V_{SS} = 0.0 V, V_{DD} = 4.75 V to 5.25 V, T_a = 0°C to 70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current, H mode, f_{CP} = 25 MHz						
Supply current	I_{DD}	When f_{CP} = 25 MHz	—	50	100	mA
Clock input pin NMCLKI						
High-level input voltage	V_{IH1}		0.8 × V_{DD}	—	V_{DD}	V
Low-level input voltage	V_{IL1}		V_{SS}	—	0.8	V
Input leakage current	I_{LK1}	V_{in} = 0 V to 5 V	—	—	±10	µA
Digital input pins NVREQ, NDACK, NWR, NRD, NCS, C80_68, A1, A0, MCM1, MCM0, MAST, HMID0 to HMID7						
High-level input voltage	V_{IH2}		0.7 × V_{DD}	—	V_{DD}	V
Low-level input voltage	V_{IL2}		V_{SS}	—	0.8	V
Input leakage current	I_{LK2}	V_{in} = 0 V to 5 V	—	—	±10	µA
Digital input pins (with built-in Schmitt trigger circuit) NRESET						
High-level input voltage	V_{IH3}		V_{DD} − 0.8	—	V_{DD}	V
Low-level input voltage	V_{IL3}		V_{SS}	—	0.8	V
Input leakage current	I_{LK3}	V_{in} = 0 V to 5 V	—	—	±10	µA
Digital output pins NHRSTA, MACK, NPEAK1, NPEAK2, CLAMP, ABC, DREQ, VSCK, VSDA, SENTIM, FR1, FR2, FSG, HMOD0 to HMOD7, HSWR, HAWR, HBWR, HCWR, NHFWE, NHRSTR, NHRSTW, HRCK, HWCK						
High-level output voltage	V_{OH4}	I_{OH4} = −2.0 mA	V_{DD} − 0.4	—	V_{DD}	V
Low-level output voltage	V_{OL4}	I_{OL4} = 2.0 mA	V_{SS}	—	0.4	V
Leakage current	I_{LK4}	V_{in} = 0 to V_{DD} In the high-impedance state	—	—	±10	µA
Digital output pins FCK1, FCK2						
High-level output voltage	V_{OH5}	I_{OH5} = −2.5 mA	V_{DD} − 0.4	—	V_{DD}	V
Low-level output voltage	V_{OL5}	I_{OL5} = 2.5 mA	V_{SS}	—	0.4	V
Leakage current	I_{LK5}	V_{in} = 0 to V_{DD} In the high-impedance state	—	—	±10	µA
Digital I/O pins HMSD0 to HMSD7, HMAD0 to HMAD6, HMBD0 to HMBD6, HMCD0 to HMCD6, VPD0 to VPD7, NSYNC, D0 to D7						
High-level input voltage	V_{IH6}		0.7 × V_{DD}	—	V_{DD}	V
Low-level input voltage	V_{IL6}		V_{SS}	—	0.8	V
High-level output voltage	V_{OH6}	I_{OH5} = −2.0 mA	V_{DD} − 0.4	—	V_{DD}	V
Low-level output voltage	V_{OL6}	I_{OL5} = 2.0 mA	V_{SS}	—	0.4	V
Leakage current	I_{LK6}	V_{in} = 0 to V_{DD} In the high-impedance state	—	—	±10	µA

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{IH} = 0.7 × V_{DD}†, V_{IL} = 0.8 V, V_{OH} = 0.7 × V_{DD}, V_{OL} = 0.2 × V_{DD}, T_a = 0°C to 70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1) Clock timing						
H mode NMCLK cycle time	t_{MCYC_H}	Load: 50 pF (With the same conditions for the following items of AC Characteristics.)	40	—	—	ns
H mode NMCLK high-level pulse width	t_{MCHW_H}		20	—	—	ns
H mode NMCLK low-level pulse width	t_{MCLW_H}		20	—	—	ns
M mode NMCLK cycle time	t_{MCYC_M}		31	—	—	ns
M mode NMCLK high-level pulse width	t_{MCHW_M}		15.5	—	—	ns
M mode NMCLK low-level pulse width	t_{MCLW_M}		15.5	—	—	ns
L mode NMCLK cycle time	t_{MCYC_L}		31	—	—	ns
L mode NMCLK high-level pulse width	t_{MCHW_L}		15.5	—	—	ns
L mode NMCLK low-level pulse width	t_{MCLW_L}		15.5	—	—	ns
NMCLK falling edge to SYNC setup time	t_{SYIS}		10	—	—	ns
NMCLK falling edge to SYNC hold time	t_{SYIH}		10	—	—	ns
NMCLK falling edge to SYNC delay time	t_{SYOD}		—	—	20	ns
2) Image bus interface (parallel mode)						
DREQ delay time	t_{DREQL}		—	—	50	ns
VPD delay time	t_{VPDD1}		—	—	40	ns
VPD hold time	t_{VPDH1}		10	—	—	ns
3) Image bus interface (serial mode)						
NVSCK rising edge to NVSEN rising edge delay time	t_{VSEL}		—	0	±10	ns
NVSCK rising edge to NVSEN falling edge delay time	t_{VSEH}		—	0	±10	ns
NVSCK rising edge to NVSDA falling edge delay time	t_{VSDH}		—	0	±10	ns
NVSCK rising edge to NVSDA falling edge delay time	t_{VSDL}		—	0	±10	ns
4) 68 family CPU interface						
NWR cycle time	t_{CYCE}		80	—	—	ns
NWR pulse width	t_{PWE}		40	—	—	ns
Address setup time	t_{AS}		40	—	—	ns
Address hold time	t_{AH}		10	—	—	ns
Data output delay time	t_{DDR}		—	—	50	ns
Data output hold time	t_{DHR}		10	—	—	ns
Data input setup time	t_{DSW}		20	—	—	ns
Data input hold time	t_{DHW}		10	—	—	ns

Note) †: This is V_{DD} − 0.8 V for the NRESET pin, and 0.8 × V_{DD} for the NMCLKI pin.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{IH} = 0.7 × V_{DD}†, V_{IL} = 0.8 V, V_{OH} = 0.7 × V_{DD}, V_{OL} = 0.2 × V_{DD}, T_a = 0°C to 70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
5) 80x86 family CPU interface						
Address setup time	t_{AR}		20	—	—	ns
Address hold time	t_{RA}		10	—	—	ns
Data output delay time	t_{RD}		—	—	50	ns
Data output hold time	t_{DR}		10	—	—	ns
Read pulse width	t_{RW}		50	—	—	ns
Address setup time	t_{AW}		20	—	—	ns
Address hold time	t_{WA}		10	—	—	ns
Data input delay time	t_{WD}		10	—	—	ns
Data input hold time	t_{DW}		10	—	—	ns
Write pulse width	t_{WW}		50	—	—	ns
6) Memory interface timing (L mode) (maximum = 2.0 MHz, MCLK = 32 MHz) T_{ACC} = 15 ns						
MCLK to NLMCE delay time	t_{MCED}		—	—	10	ns
MCLK to NLMWE delay time	t_{MWED}		—	—	10	ns
MCLK to NLMOE delay time	t_{MOED}		—	—	10	ns
MCLK to LMA delay time	t_{LMAD}		—	—	10	ns
MCLK to LMXD input setup time	t_{MXIS}		5	—	—	ns
MCLK to LMXD input hold time	t_{MXIH}		10	—	—	ns
NLMOE rising edge to LMXD output delay time	t_{OEMD}		—	—	20	ns
(L mode, MAG : 0, STK : 1, RSH : 0 or 1) Pseudo SRAM : T_{ACC} = 15 ns						
NLMCE high-level pulse width	t_{MCEWH1}		t_{MCYC} × 1.5 −5	—	—	ns
NLMCE falling edge to NLMWE rising edge delay time	t_{MCWD1}		—	—	t_{MCYC} × 2 +10	ns
LMA13-LMA14 to NLMWE rising edge delay time	t_{LMWED1}		—	—	t_{MCYC} × 1.5 +5	ns
NLMWE low-level pulse width	t_{MWEWL1}		t_{MCYC} −10	—	—	ns
NLMWE rising edge to LMXD output hold time	t_{MXOH1}		10	—	—	ns
(L mode, MAG : 0, STK : 0, RSH : 0 or 1) Pseudo SRAM : T_{ACC} = 15 ns						
NLMCE high-level pulse width	t_{MCEWH2}		t_{MCYC} −5	—	—	ns
NLMCE low-level pulse width	t_{MCEWL2}		t_{MCYC} × 1.5 −5	—	—	ns
NLMCE falling edge to NLMWE rising edge delay time	t_{MCWD2}		—	—	t_{MCYC} × 1.5 +5	ns

Note) †: This is V_{DD} − 0.8 V for the NRESET pin, and 0.8 × V_{DD} for the NMCLKI pin.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{IH} = 0.7 × V_{DD}†, V_{IL} = 0.8 V, V_{OH} = 0.7 × V_{DD}, V_{OL} = 0.2 × V_{DD}, T_a = 0°C to 70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(L mode, MAG : 0, STK : 0, RSH : 0 or 1) (continued) Pseudo SRAM : T_{ACC} = 15 ns						
NLMWE low-level pulse width	t_{MWEWL2}		t_{MCYC} × 1.5 −10	—	—	ns
NLMWE rising edge to LMXD output hold time	t_{MXOH2}		10	—	—	ns
(L mode, MAG : 1, STK : 0, RSH : ∗) Pseudo SRAM : T_{ACC} = 15 ns						
NLMCE high-level pulse width	t_{MCEWH3}		t_{MCYC} /2 −5	—	—	ns
NLMCE high-level pulse width 1	t_{MCEWL3}		t_{MCYC} × 1.5 −10	—	—	ns
NLMCE low-level pulse width 2	$t_{MCEWL32}$		t_{MCYC} −10	—	—	ns
NLMCE falling edge to NLMWE rising edge delay time	t_{MCWD3}		—	—	t_{MCYC} +5	ns
NLMWE low-level pulse width	t_{MWEWL3}		t_{MCYC} −5	—	—	ns
NLMWE falling edge to LMXD output hold time	t_{MXOH3}		10	—	—	ns
(L mode, MAG : 0, STK : 1, RSH : ∗) Pseudo SRAM : T_{ACC} = 15 ns						
NLMCE high-level pulse width	t_{MCEWH4}		t_{MCYC} −10	—	—	ns
NLMCE falling edge to NLMWE rising edge delay time	t_{MCWD4}		—	—	t_{MCYC} × 1.5 +5	ns
LMA12-LMA14 to NLMWE rising edge delay time	t_{LMWED4}		—	—	t_{MCYC} +5	ns
NLMWE low-level pulse width	t_{MWEWL4}		t_{MCYC} /2 −5	—	—	ns
NLMWE rising edge to LMXD output hold time	t_{MXOH4}		10	—	—	ns
(L mode, MAG : 0, STK : 0, RSH : 0 or 1 ; SRAM) (maximum 2.0 MHz, MCLK = 32 MHz) SRAM : T_{ACC} = 15 ns						
LMA−NLMWE falling edge delay time	t_{LMWED5}		—	—	t_{MCYC} +5	ns
NLMWE low-level pulse width	t_{MWEWL5}		t_{MCYC} × 1.5 −10	—	—	ns
NLMWE rising edge to LMA output hold time	t_{LMOH5}		t_{MCYC} /2 −5	—	—	ns
NLMWE rising edge to LMXD output hold time	t_{MXOH5}		t_{MCYC} /2 −5	—	—	ns

Note) †: This is V_{DD}− 0.8 V for the NRESET pin, and 0.8 × V_{DD} for the NMCLKI pin.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{IH} = 0.7 × V_{DD}†, V_{IL} = 0.8 V, V_{OH} = 0.7 × V_{DD}, V_{OL} = 0.2 × V_{DD}, T_a = 0°C to 70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(L mode, MAG : 1, STK : 0, RSH : 0 or 1) SRAM : T_{ACC} = 15 ns						
LMA to NLMWE falling edge delay time	t_{LMWED6}		—	—	t_{MCYC}/2 −5	ns
NLMWE low-level pulse width	t_{MWEWL6}		t_{MCYC} −10	—	—	ns
NLMWE rising edge to LMA output hold time	t_{LMOH6}		10	—	—	ns
NLMWE rising edge to LMXD output hold time	t_{MXOH6}		10	—	—	ns
(M mode) (maximum 4 MHz, MCLK = 32 MHz) SRAM : T_{ACC} = 30 ns						
MCLK rising edge to CKVD output delay time	t_{CKVM}		—	—	10	ns
MCLK rising edge to MMA0-MMA13 MSA0-MSA1 output delay time	t_{MMA}		—	—	10	ns
MCLK falling edge to NMMLD0-NMMLD6 input setup time NMMED0-NMMED7 NMMFD0-NMMFD7	t_{MXISM}		5	—	—	ns
MCLK falling edge to NMMLD0-NMMLD6 input hold time NMMED0-NMMED7 NMMFD0-NMMFD7	t_{MXIHM}		10	—	—	ns
MMA0-MMA13 to NMMLWE falling edge output setup time NMMEWE falling edge NMMFWE falling edge	t_{MAWE}		t_{MCYC}/2 −5	—	—	ns
MCLK falling edge to MMLWE falling edge output delay time MMEWE falling edge MMFWE falling edge	t_{MWED}		—	—	15	ns
MCLK rising edge to NMMOE output delay time	t_{MMOED}		—	—	15	ns
NMMLWE low-level pulse width NMMEWE NMMFWE	t_{MLWEW}		t_{MCYC} × 2 −10	—	—	ns
NMMLWE rising edge to NMMLD0-NMMLD6 output hold time NMMEWE rising edge to NMMED0-NMMED7 NMMFWE rising edge to NMMFD0-NMMFD7	t_{MXOHM}		t_{MCYC}/2 −5	—	—	ns
NMMOE rising edge to NMMLD0-NMMLD6 output delay time NMMED0-NMMED7 NMMFD0-NMMFD7	t_{OEMDM}		—	—	20	ns

Note) †: This is V_{DD} − 0.8 V for the NRESET pin, and 0.8 × V_{DD} for the NMCLKI pin.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{IH} = 0.7 × V_{DD}†, V_{IL} = 0.8 V, V_{OH} = 0.7 × V_{DD}, V_{OL} = 0.2 × V_{DD}, T_a = 0°C to 70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(H mode) (maximum 12.5 MHz, MCLK = 25 MHz) SRAM : T_{ACC} = 15 ns						
MCLK to MACK output delay time	t_{MACD}		—	—	15	ns
MCLK to NHRSTA output delay time	t_{STAD}		—	—	15	ns
MCLK to HMWE output delay time	t_{HMWED}		—	—	15	ns
MCLK rising edge to HMSD0-HMSD7 input setup time HMAD0-HMAD6 HMBD0-HMBD6 HMCD0-HMCD6	t_{MXISH}		10	—	—	ns
MCLK rising edge to HMSD0-HMSD7 input hold time HMAD0-HMAD6 HMBD0-HMBD6 HMCD0-HMCD6	t_{MXIHH}		15	—	—	ns
MCLK rising edge to HSWR output delay time HAWR HBWR HCWR	t_{HWRD}		—	—	15	ns
HSWR rising edge to HMSD0-HMSD7 output delay time HAWR rising edge to HMAD0-HMAD6 HBWR rising edge to HMBD0-HMBD6 HCWR rising edge to HMCD0-HMCD6	t_{HWRMD}		—	—	15	ns
HMWE pulse width	t_{HMWW}		t_{MCYC} −5	—	—	ns
7) FIFO memory interface						
NMCLKI rising edge to HWCK or HRCK falling edge output delay time	t_{MHL}		—	—	15	ns
NMCLKI falling edge to CK or HRCK rising edge output delay time	t_{MHH}		—	—	15	ns
HWCK falling edge to HRSTW falling edge output delay time HRCK falling edge to HRSTR falling edge	t_{HSL}		—	—	±8	ns
HWCK falling edge to HRSTW rising edge output delay time HRCK falling edge to HRSTR rising edge	t_{HSH}		—	—	±8	ns
HWCK or HRCK low-level pulse width	t_{HLW}		t_{MCYC} /2 −5	—	—	ns
HWCK or HRCK high-level pulse width	t_{HHW}		t_{MCYC} /2 −5	—	—	ns

Note) †: This is V_{DD} − 0.8 V for the NRESET pin, and 0.8 × V_{DD} for the NMCLKI pin.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{IH} = 0.7 × V_{DD}†, V_{IL} = 0.8 V, V_{OH} = 0.7 × V_{DD}, V_{OL} = 0.2 × V_{DD}, T_a = 0°C to 70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
7) FIFO memory interface (continuted)						
HWCK falling edge to HFWE falling edge output delay time	t_{HWL}		—	—	±8	ns
HWCK falling edge to HFWE falling edge output delay time	t_{HWH}		—	—	±8	ns
HWCK falling edge to HMOD0-HMOD7 output delay time	t_{HOD}		—	—	±8	ns
HRCK rising edge to HMID0-HMID7 setup time	t_{HIS}		—	—	10	ns
HRCK rising edge to HMID0-HMID7 hold time	t_{HIH}		—	—	0	ns
8) Multivalued output interface						
NMCLKI rising edge to CKVG falling edge output delay time	t_{MGL}		—	—	15	ns
NMCLKI falling edge to CKVG rising edge output delay time	t_{MGH}		—	—	15	ns
CKVG low-level pulse width	t_{GLW}		$t_{MCYC}/2$ −5	—	—	ns
CKVG high-level pulse width	t_{GHW}		$t_{MCYC}/2$ −5	—	—	ns
CKVG rising edge to VGSD6-VGSD0 output delay time	t_{GSD}		—	—	±10	ns
9) CCD sensor interface						
NMCLKI falling edge to FCK1 falling edge output delay time	t_{MF1L}		—	—	15	ns
NMCLKI falling edge to FCK1 rising edge output delay time	t_{MF1H}		—	—	15	ns
NMCLKI falling edge to FCK2 falling edge output delay time	t_{MF2L}		—	—	15	ns
NMCLKI falling edge to FCK2 rising edge output delay time	t_{MF2H}		—	—	15	ns
NMCLKI rising edge to FR1 rising edge output delay time	t_{MR1H}		—	—	15	ns
NMCLKI rising edge to FR1 falling edge output delay time	t_{MR1L}		—	—	15	ns
NMCLKI rising edge to FR2 rising edge output delay time	t_{MR2H}		—	—	15	ns

Note) †: This is V_{DD} − 0.8 V for the NRESET pin, and 0.8 × V_{DD} for the NMCLKI pin.

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, V_{IH} = 0.7 × V_{DD}†, V_{IL} = 0.8 V, V_{OH} = 0.7 × V_{DD}, V_{OL} = 0.2 × V_{DD}, T_a = 0°C to 70°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
9) CCD sensor interface (continued)						
NMCLKI rising edge to FR2 falling edge output delay time	t_{MR2L}		—	—	15	ns
FR1 falling edge to FCK1 falling edge or FR2 rising edge output delay time	t_{R1FM}		—	—	0	ns
FR2 falling edge to FCK1 riging edge or FR2 falling edge output delay time	t_{R2FM}		—	—	0	ns
FCK1 rising edge to FCK2 falling edge or FCK1 falling edge to FCK2 rising edge output delay time	t_{FC12}		—	—	±5	ns

Note) †: This is V_{DD} − 0.8 V for the NRESET pin, and 0.8 × V_{DD} for the NMCLKI pin.

5. Analog Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
A/D converter						
Resolution	RES		—	—	8	bit
Linearity error	EL	f = 0.1 MHz to 12.5 MHz	—	±0.5	±0.9	LSB
Differential linearity error	ED	V_{REFH} = 4.0 V, V_{REFL} = 1.0 V	—	±0.5	±0.9	LSB
Reference voltage high level	V_{REFH}		1.6	—	V_{DD}	V
Reference voltage low level	V_{REFL}		V_{SS}	—	3.4	V
Reference voltage low to high level difference	V_{REFHL}		1.6	—	V_{DD}	V
Reference ladder resistor	R_{REF}	V_{REFHL} = 3.0 V	300	450	—	Ω
Offset voltage low side	V_{ADOFF}	V_{REFHL} = 3.0 V	0	—	150	mV
FET						
Minimum channel resistance	R_{CHO}	V_{FETG} = 5.0 V, V_{FETS} = 1.5 V V_{FETD} = 1.7 V	20	30	60	Ω
Gate leakage current	I_{FETG}	V_{FETG} = V_{SS}, V_{AGOUT} = V_{DD}	—	—	±100	nA
		V_{FETG} = V_{DD}, V_{AGOUT} = V_{SS}				
FET gate control analog switch						
AGOUT to FETG on-resistance	R_{FET}	V_{AGOUT} = 2.5 V, V_{FETG} = 3.0 V	—	—	1.0	kΩ
AGOUT to FETG off-leakage	I_{AGL}	V_{AGOUT} = 2.5 V, V_{FETG} = 3.0 V	—	—	±100	nA
ABC control analog switch						
AGDR to AGOUT on-resistance	R_{DR}	V_{AGOUT} = 2.5 V, V_{AGDR} = 3.0 V	—	—	300	Ω
AGUR to AGOUT on-resistance	R_{UR}	V_{AGOUT} = 2.5 V, V_{AGUR} = 2.0 V	—	—	300	Ω
VINIG to AGOUT on-resistance	R_{INIG}	V_{AGOUT} = 2.5 V, V_{INIG} = 3.0 V	—	—	300	Ω

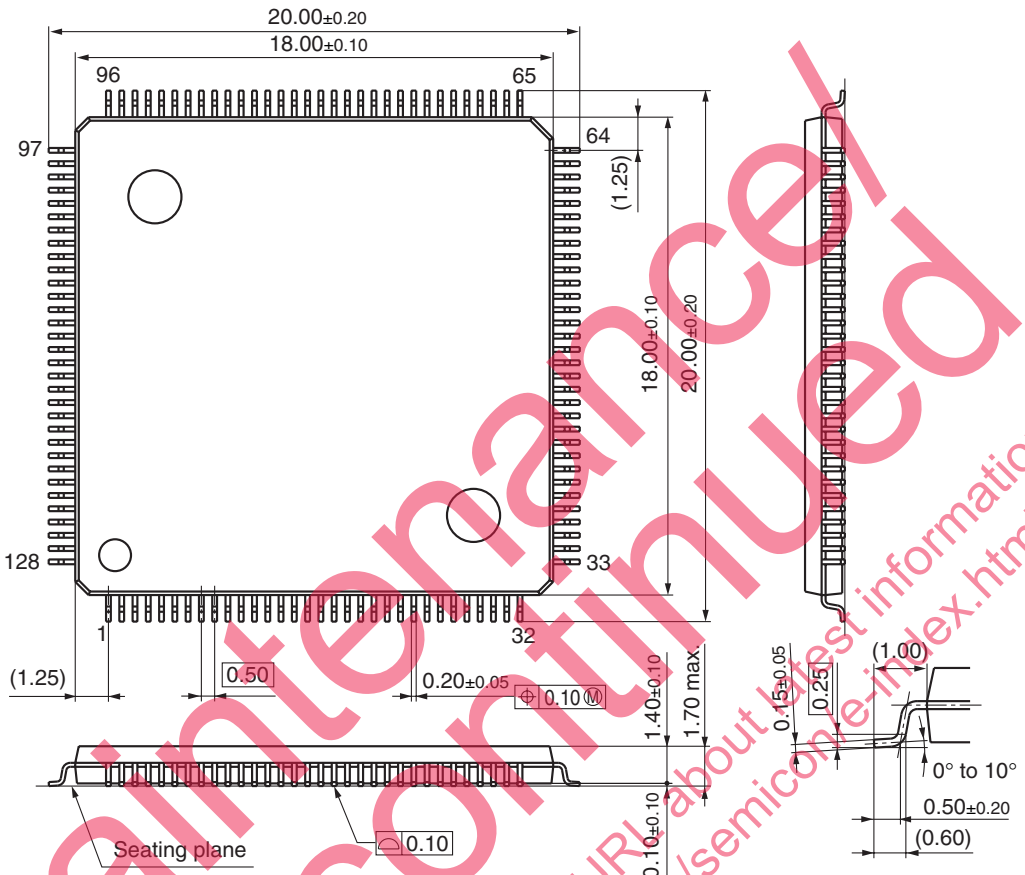
■ Electrical Characteristics (continued)

5. Analog Characteristics at V_{DD} = 5.0 V, V_{SS} = 0.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ABC control analog switch (continued)						
AGOUT off leakage current	I_{AGOUT}	$V_{AGOUT} = V_{DD}$, $V_{INIG} = V_{SS}$ $V_{AGDR} = V_{SS}$, $V_{AGUR} = V_{SS}$	—	—	±100	nA
		$V_{AGOUT} = V_{SS}$, $V_{INIG} = V_{DD}$ $V_{AGDR} = V_{DD}$, $V_{AGUR} = V_{DD}$				
Offset control analog switch						
OFHC charge resistance	R_{OFU}	V_{OFHC} = 2.5 V	—	9.5	20.0	kΩ
OFHC discharge resistance	R_{OFD}	V_{OFHC} = 2.5 V	—	11.5	20.0	kΩ
OFHC off leakage current	I_{OFHC}	$V_{OFHC} = V_{DD}$ or $V_{OFHC} = V_{SS}$	—	—	±100	nA
Offset control FET						
OFOUT on current	I_{DSOUT}	$V_{OFHC} = V_{DD}$, V_{OFOUT} = 3.0 V	1.0	3.7	—	mA
OFOUT off leakage current	I_{OFOUT}	$V_{OFHC} = V_{SS}$, V_{OFOUT} = 2.5 V	—	—	±100	nA

■ Package Dimensions (Unit: mm)

• LQFP128-P-1818C (Lead-free package)



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