

# NTR4101P

## Trench Power MOSFET –20 V, Single P–Channel, SOT–23

### Features

- Leading –20 V Trench for Low  $R_{DS(on)}$
- –1.8 V Rated for Low Voltage Gate Drive
- SOT–23 Surface Mount for Small Footprint
- Pb–Free Package is Available

### Applications

- Load/Power Management for Portables
- Load/Power Management for Computing
- Charging Circuits and Battery Protection

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain–to–Source Voltage	$V_{DSS}$	–20	V	
Gate–to–Source Voltage	$V_{GS}$	$\pm 8.0$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ –2.4	A
		$T_A = 85^\circ\text{C}$	–1.7	
		$t \leq 10$ s	$T_A = 25^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 0.73	W
		$t \leq 10$ s	1.25	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ –1.8	A
		$T_A = 85^\circ\text{C}$	–1.3	
		$T_A = 25^\circ\text{C}$	$P_D$ 0.42	
Power Dissipation (Note 2)				
Pulsed Drain Current	$t_p = 10$ $\mu\text{s}$	$I_{DM}$	–7.5	A
ESD Capability (Note 3)	$C = 100$ pF, $RS = 1500$ $\Omega$	ESD	225	V
Operating Junction and Storage Temperature	$T_J$ , $T_{STG}$	–55 to 150		$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	–2.4		A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260		$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	170	$^\circ\text{C}/\text{W}$
Junction–to–Ambient – $t < 10$ s (Note 1)	$R_{\theta JA}$	100	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	300	

1. Surface–mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface–mounted on FR4 board using the minimum recommended pad size.
3. ESD Rating Information: HBM Class 0

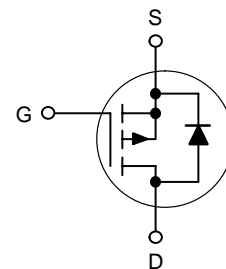


ON Semiconductor®

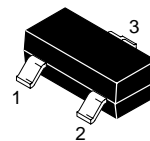
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
–20 V	70 m $\Omega$ @ –4.5 V	–3.2 A
	90 m $\Omega$ @ –2.5 V	
	112 m $\Omega$ @ –1.8 V	

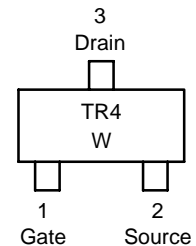
### P–Channel MOSFET



### MARKING DIAGRAM & PIN ASSIGNMENT



SOT–23  
CASE 318  
STYLE 21



TR4 = Device Code  
W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NTR4101PT1	SOT–23	3000/Tape & Reel
NTR4101PT1G	SOT–23 Pb–Free	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTR4101P

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 4) (V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA)	V <sub>(BR)DSS</sub>	-20			V
Zero Gate Voltage Drain Current (Note 4) (V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V)	I <sub>DSS</sub>			-1.0	μA
Gate-to-Source Leakage Current (V <sub>GS</sub> = ±8.0 V, V <sub>DS</sub> = 0 V)	I <sub>GSS</sub>			±100	nA

## ON CHARACTERISTICS

Gate Threshold Voltage (Note 4) (V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA)	V <sub>GS(th)</sub>	-0.40	-0.720	-1.5	V
Drain-to-Source On-Resistance (V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.6 A) (V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1.3 A) (V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -0.9 A)	R <sub>DS(on)</sub>		70 90 112	85 120 210	mΩ
Forward Transconductance (V <sub>DS</sub> = -5.0 V, I <sub>D</sub> = -2.3 A)	g <sub>FS</sub>		75		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	(V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = -10 V)	C <sub>iSS</sub>	675		pF
Output Capacitance		C <sub>oss</sub>	100		
Reverse Transfer Capacitance		C <sub>rss</sub>	75		
Total Gate Charge	(V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A)	Q <sub>G(tot)</sub>	7.5	8.5	nC
Gate-to-Source Gate Charge	(V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A)	Q <sub>GS</sub>	1.2		nC
Gate-to-Drain "Miller" Charge	(V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A)	Q <sub>GD</sub>	2.2		nC
Gate Resistance		R <sub>G</sub>	6.5		Ω

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1.6 A, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	7.5		ns
Rise Time		t <sub>r</sub>	12.6		
Turn-Off Delay Time		t <sub>d(off)</sub>	30.2		
Fall Time		t <sub>f</sub>	21.0		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	(V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.4 A)	V <sub>SD</sub>	-0.82	-1.2	V
Reverse Recovery Time	(V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = -1.6 A)	t <sub>rr</sub>	12.8	15	ns
Charge Time		t <sub>a</sub>	9.9		ns
Discharge Time		t <sub>b</sub>	3.0		ns
Reverse Recovery Charge		Q <sub>rr</sub>	1008		nC

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperature.

# NTR4101P

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

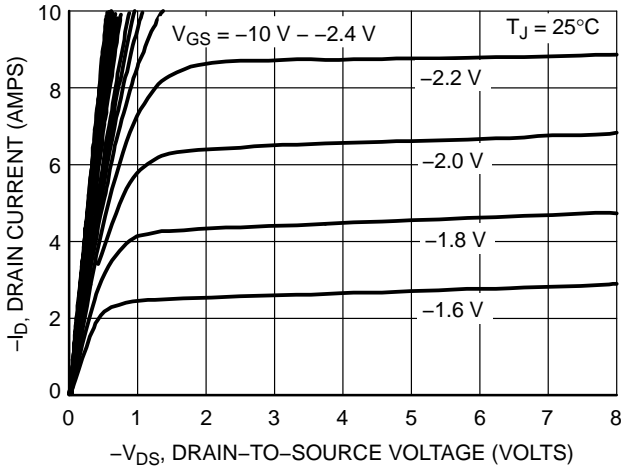


Figure 1. On-Region Characteristics

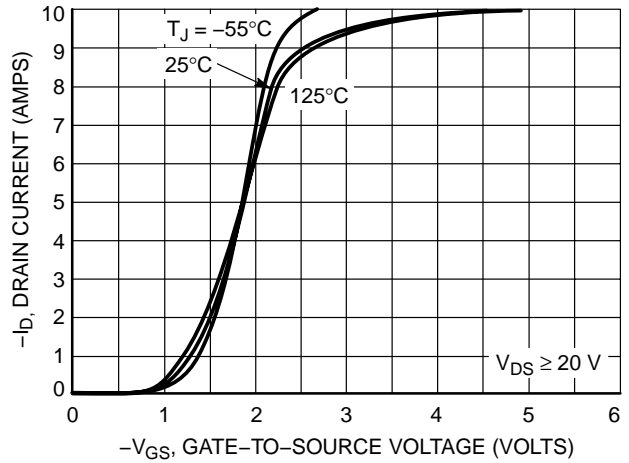


Figure 2. Transfer Characteristics

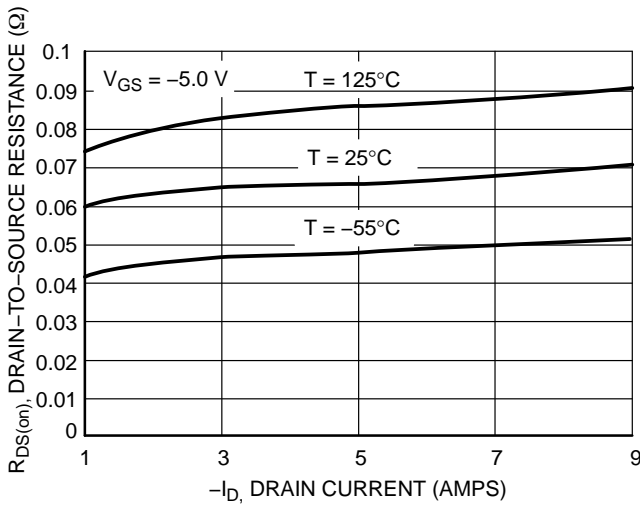


Figure 3. On-Resistance vs. Drain Current and Temperature

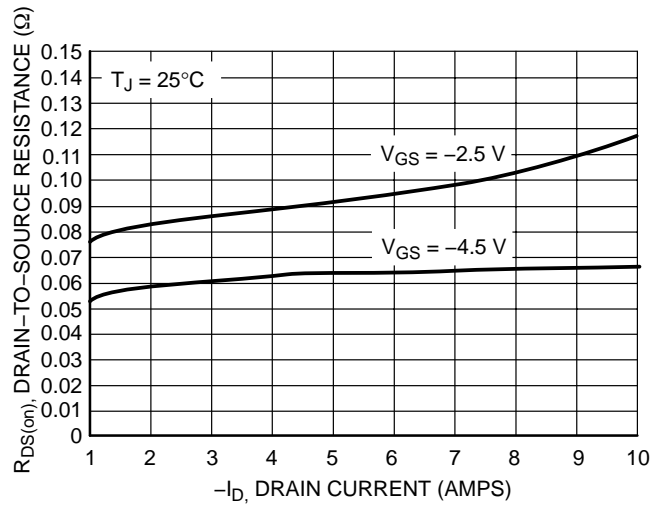


Figure 4. On-Resistance vs. Drain Current and Temperature

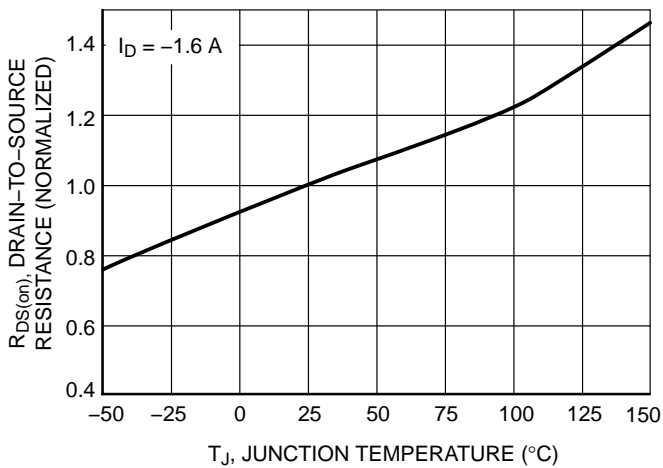


Figure 5. On-Resistance Variation with Temperature

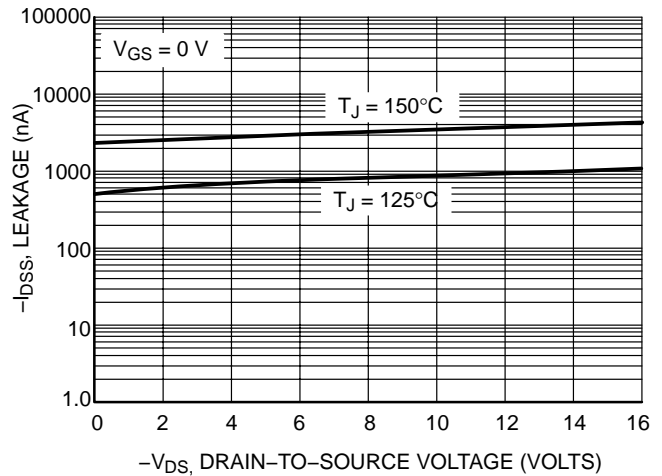


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTR4101P

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

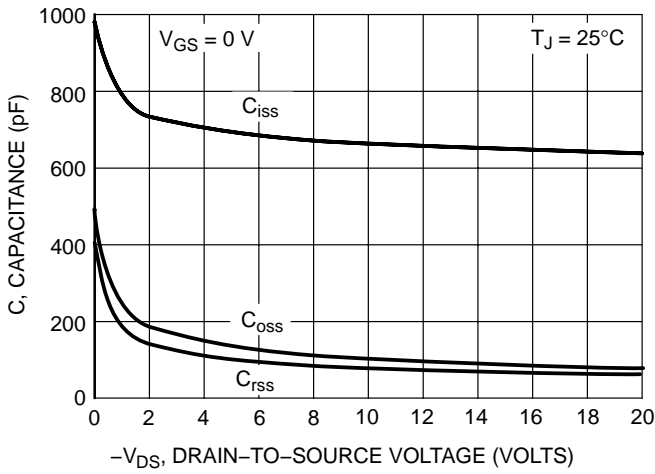


Figure 7. Capacitance Variation

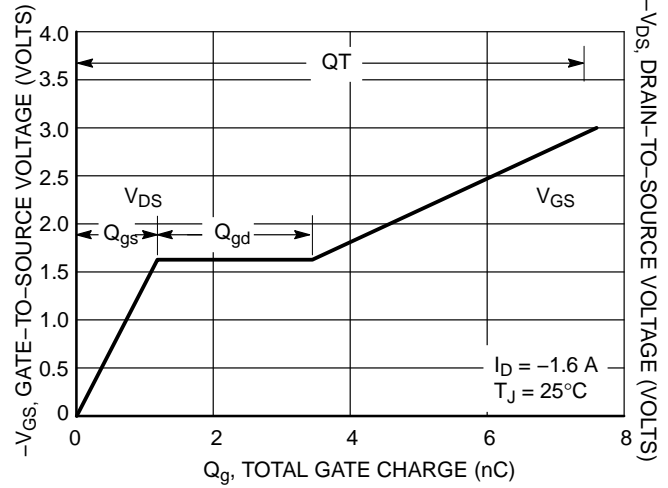


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge

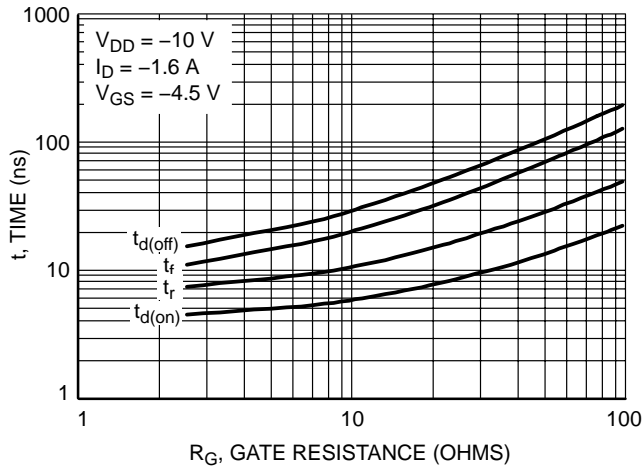


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

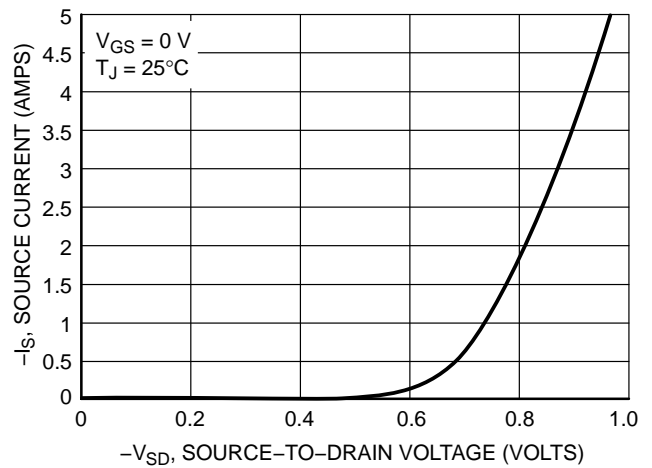
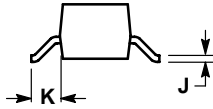
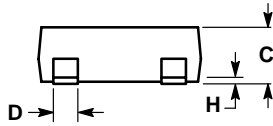
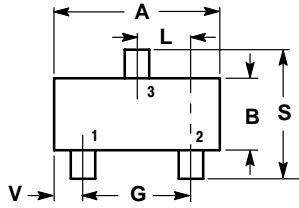


Figure 10. Diode Forward Voltage vs. Current

# NTR4101P

## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AK



NOTES:

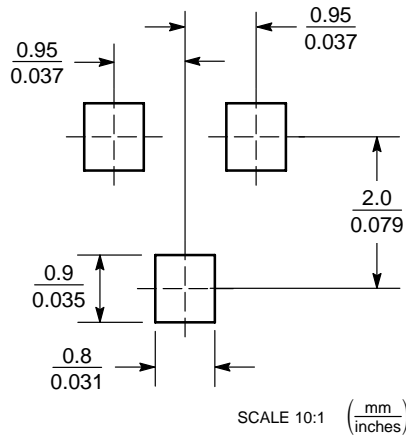
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-03 AND -07 OBSOLETE, NEW STANDARD 318-08.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60


STYLE 21:

- PIN 1. GATE
- SOURCE
- DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your  
local Sales Representative.