



STT5NF30L

N-CHANNEL 30V - 0.039Ω - 4A SOT23-6L
STripFET™II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STT5NF30L	30 V	< 0.050 Ω (@ 10V)	4 A

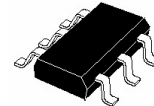
- TYPICAL R_{DS(on)} = 0.039Ω @10V
- LOW Q_g
- LOW THRESHOLD DRIVE

DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

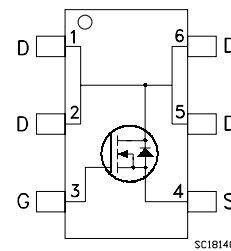
APPLICATIONS

- DC-DC CONVERTERS
- POWER MANAGEMENT IN PORTABLE/DESKTOP PCs
- SYNCHRONOUS RECTIFICATION
- DC MOTOR CONTROL (DISK DRIVERS, etc)



SOT23-6L

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STT5NF30L	STFN	SOT23-6L	TAPE & REEL

STT5NF30L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	30	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	30	V
V_{GS}	Gate- source Voltage	± 16	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	4	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM} (\bullet)$	Drain Current (pulsed)	16	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	1.6	W
$E_{AS} (1)$	Single Pulse Avalanche Energy	50	mJ

(\bullet)Pulse width limited by safe operating area

(1) Starting $T_j = 25^\circ\text{C}$, $I_d = 2 \text{ A}$, $V_{DD} = 15\text{V}$.

THERMAL DATA

$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	78	$^\circ\text{C/W}$
T_I	Max. Operating Junction Temperature		- 55 to 150	$^\circ\text{C}$
T_{stg}	Storage Temperature		- 55 to 150	$^\circ\text{C}$

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{V}$			± 100	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$ $V_{GS} = 5 \text{ V}$, $I_D = 2 \text{ A}$		0.039 0.046	0.050 0.060	Ω Ω

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25\text{ }^{\circ}\text{C}$ UNLESS OTHERWISE SPECIFIED)
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 2\text{ A}$		3		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		330		pF
C_{oss}	Output Capacitance			90		pF
C_{rss}	Reverse Transfer Capacitance			40		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 2\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		11		ns
t_r	Rise Time			100		ns
Q_g	Total Gate Charge	$V_{DD} = 24\text{ V}$, $I_D = 4\text{ A}$, $V_{GS} = 5\text{ V}$		6.5	9	nC
Q_{gs}	Gate-Source Charge			3.6		nC
Q_{gd}	Gate-Drain Charge			2		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-Off Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 5)		25		ns
t_f	Fall Time			22		ns

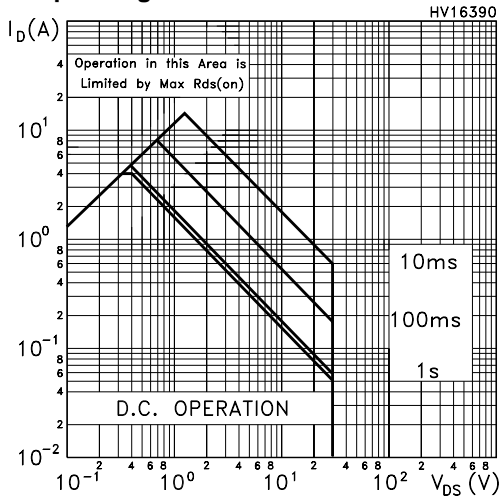
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				4	A
I_{SDM} (2)	Source-drain Current (pulsed)				16	A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 4\text{ A}$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$, $T_j = 150^{\circ}\text{C}$ (see test circuit, Figure 5)		35		ns
Q_{rr}	Reverse Recovery Charge			25		nC
I_{RRM}	Reverse Recovery Current			14		A

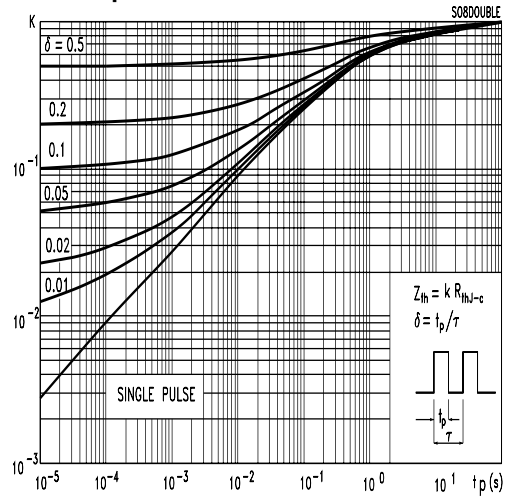
Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

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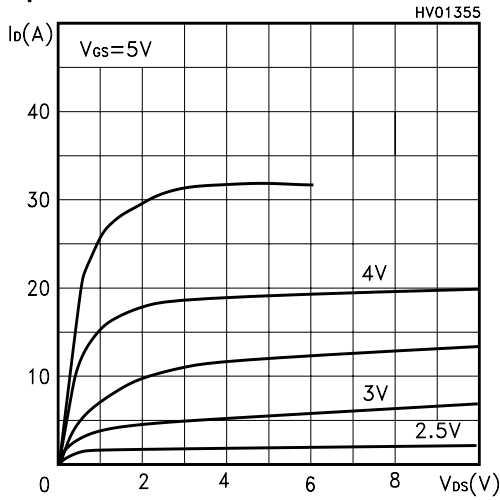
Safe Operating Area



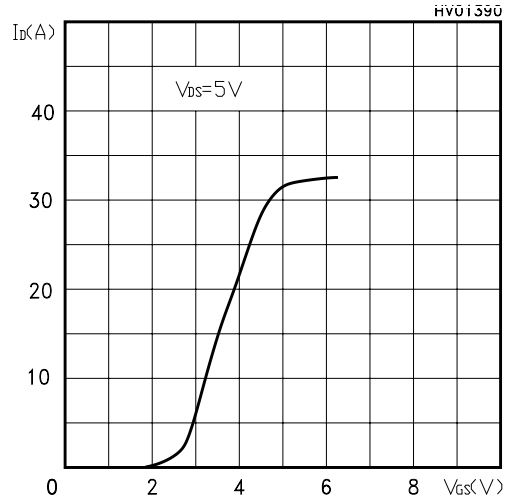
Thermal Impedance Junction-PCB



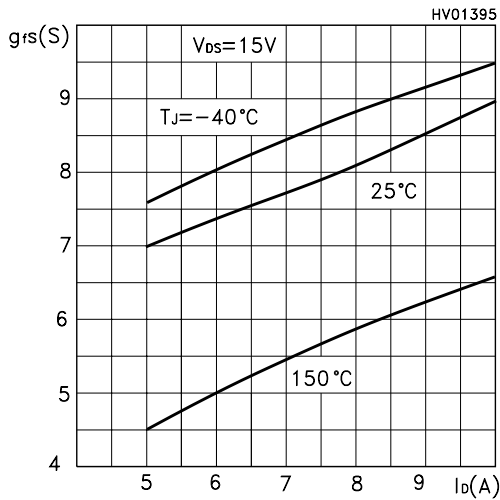
Output Characteristics



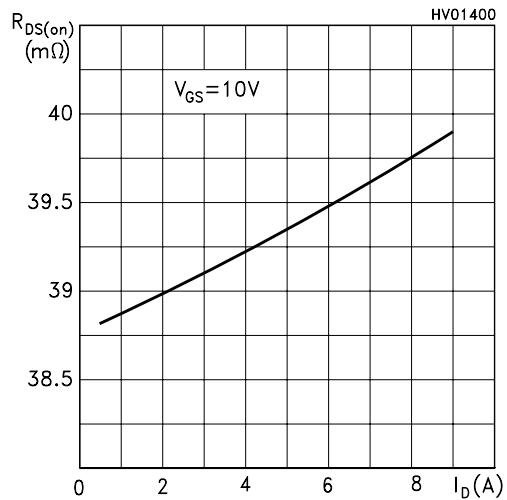
Transfer Characteristics



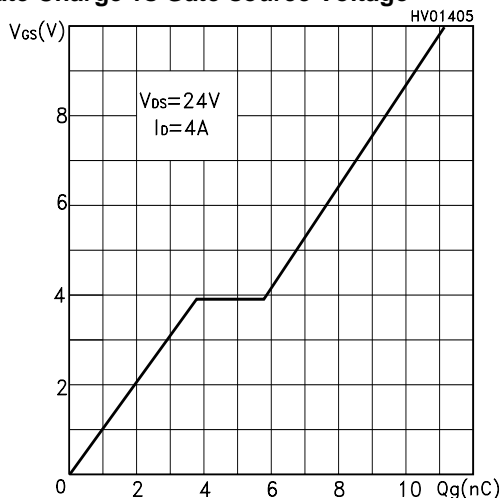
Transconductance



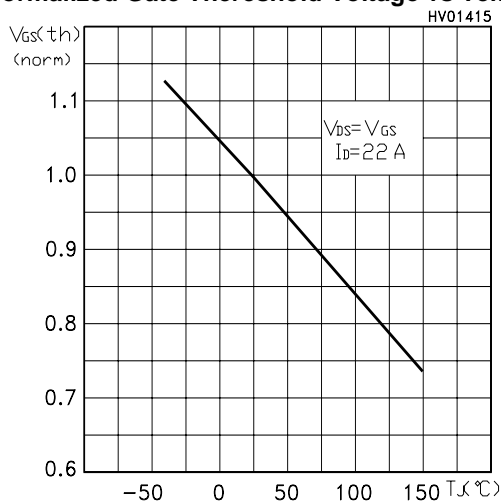
Static Drain-source On Resistance



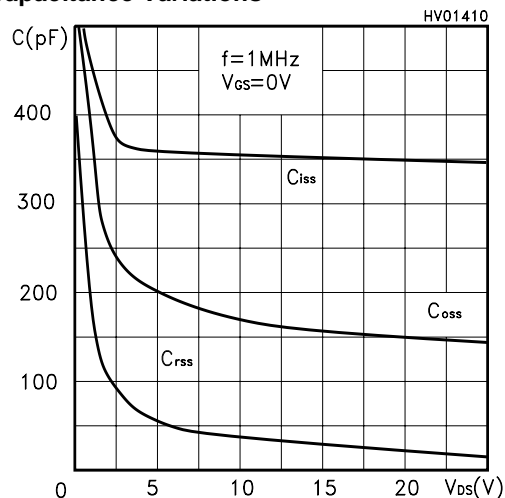
Gate Charge vs Gate-source Voltage



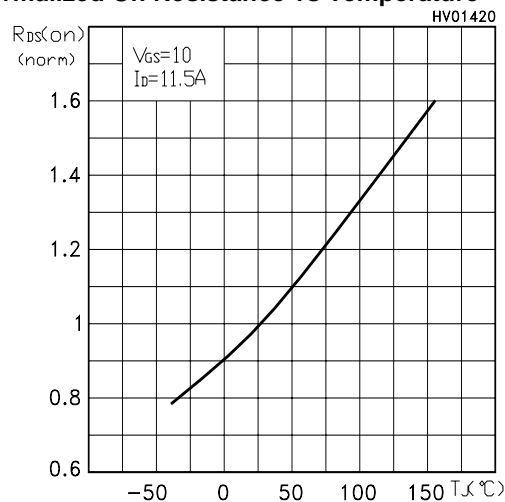
Normalized Gate Threshold Voltage vs Temp.



Capacitance Variations



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

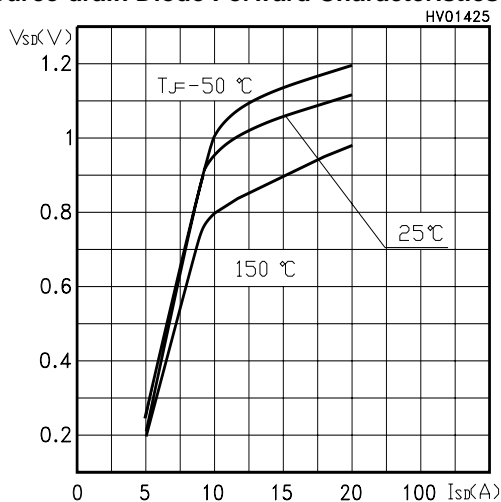


Fig. 1: Unclamped Inductive Load Test Circuit

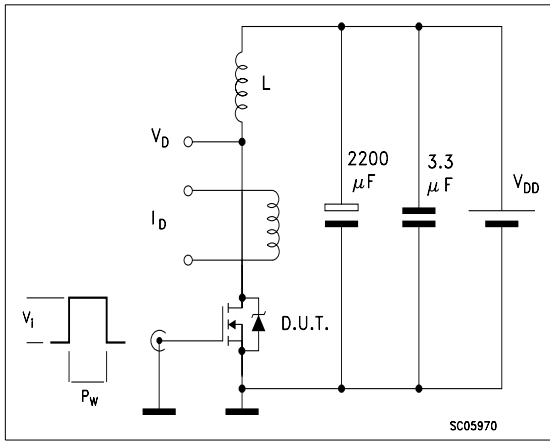


Fig. 2: Unclamped Inductive Waveform

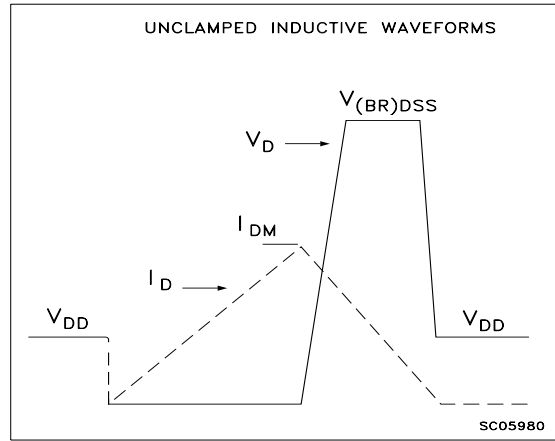


Fig. 3: Switching Times Test Circuit For Resistive Load

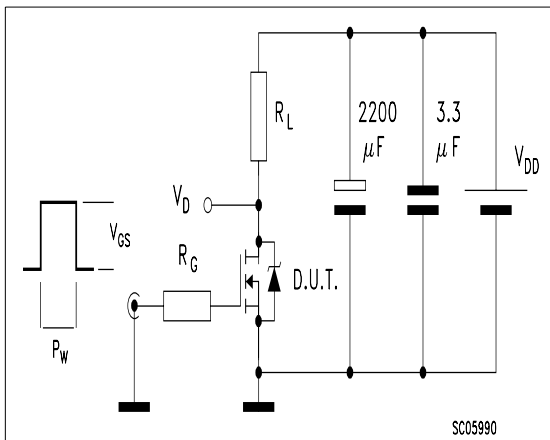


Fig. 4: Gate Charge test Circuit

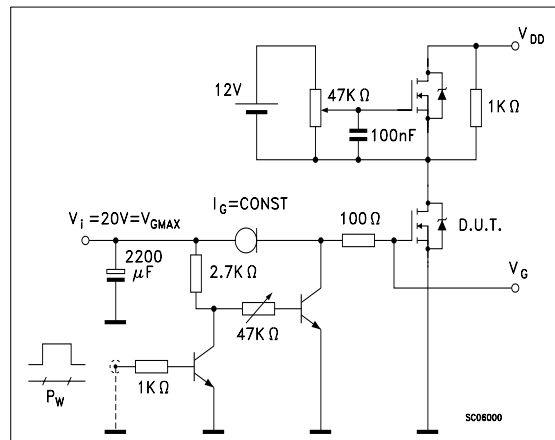
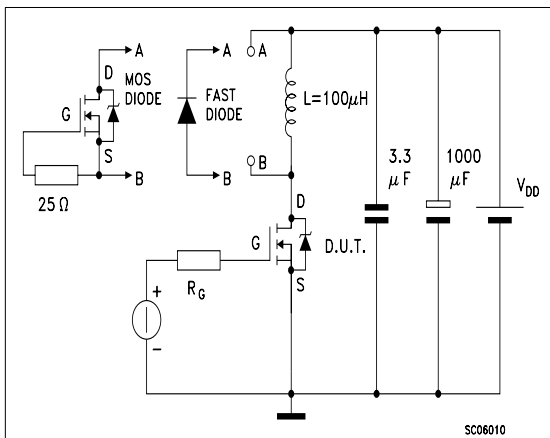
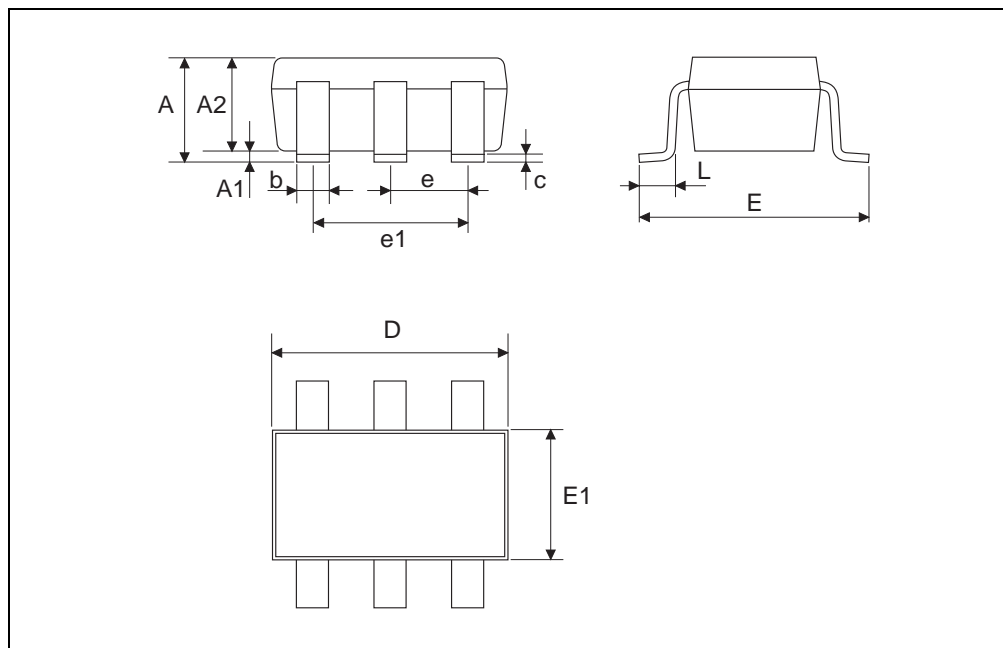


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SOT23-6L MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90		1.30	0.035		0.051
b	0.25		0.50	0.010		0.020
C	0.09		0.20	0.004		0.008
D	2.80		3.10	0.110		0.122
E	2.60		3.00	0.102		0.118
E1	1.50		1.75	0.059		0.069
L	0.35		0.55	0.014		0.022
e		0.95			0.037	
e1		1.90			0.075	



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