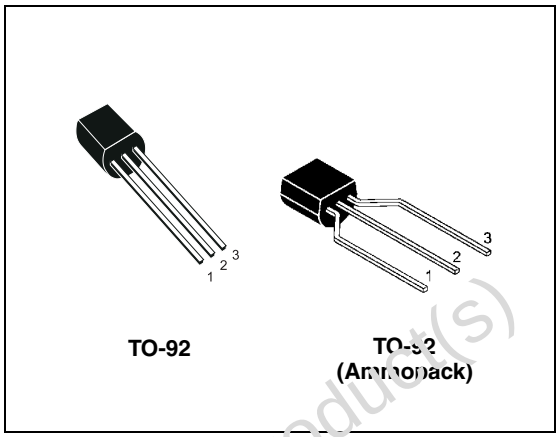
STQ1NE10L

N-channel 100V - 0.3Ω - 1A - TO-92
STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STQ1NE10L	100V	<0.4Ω	1A

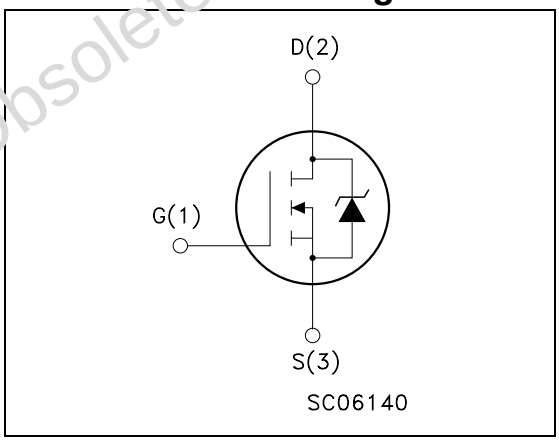
- Exceptional high dv/dt capability
- 100% avalanche tested
- Avalanche rugged technology
- Low threshold drive



Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STQ1NE10L	Q1NE10L	TO-92	Tube
STQ1NE10L-AP	Q1NE10L	TO-92	Ammopak

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at T_C = 25°C	1	A
I_D	Drain current (continuous) at T_C=100°C	0.6	A
I_{DG}	Drain gate current (continuous)	± 50	mA
I_{GS}	Gate source current (continuous)	± 50	mA
I_{DM}(1)	Drain current (pulsed)	4	A
P_{TOT}(2)	Total dissipation at T_C = 25°C	3	W
	Derating factor	0.025	W/°C
dv/dt(3)	Peak diode recovery voltage slope	6	V/ns
E_{AS}(4)	Single pulse avalanche energy	400	mJ
T_{stg}	Storage temperature	-55 to 150	°C
T_J	Operating junction temperature		

1. Pulse width limited by safe operating area.
2. Related to Rthj -l
3. $I_{SD} \leq 1A$, di/dt $\leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
4. Starting T_J = 25 °C, I_D = 1A, V_{DD} = 50V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max	40	°C/W
R_{thJA}	Thermal resistance junction-ambient max	125	°C/W
T_l	Maximum lead temperature for soldering purpose	260	°C

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DG}$	Clamped voltage	I_D = 250µA, V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1		2.5	V
$R_{DS(on)}$	Static drain-source ON resistance	V_{GS} = 10 V, I_D = 0.5 A V_{GS} = 5 V, I_D = 0.5 A		0.30 0.35	0.40 0.45	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 µA		2		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1MHz, V_{GS} = 0		345 45 20		pF pF pF
$t_{r(on)}$ t_f	Turn-on time Rise time	V_{DD} = 50 V, I_D = 0.5 A, R_G = 4.7 Ω, V_{GS} = 10 V *Figure 12*		11 12		ns ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 50 V, I_D = 0.5 A R_G = 4.7Ω, V_{GS} = 5 V *Figure 12*		20 13		ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 80 V, I_D = 1A, V_{GS} = 5V *Figure 13*		7 1.5 3.5		nC nC nC

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				1	A
I_{SDM}(1)	Source-drain current (pulsed)				4	A
V_{SD}(2)	Forward on voltage	I_{SD}=1A, V_{GS}=0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1A, di/dt = 100A/µs, V_{DD}=30V, T_J = 100°C		52 90 3.5		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

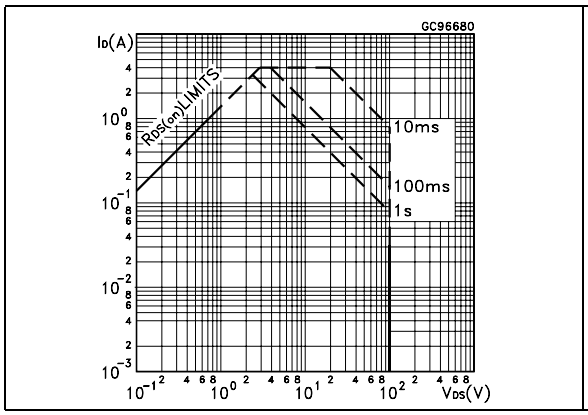


Figure 2. Thermal impedance

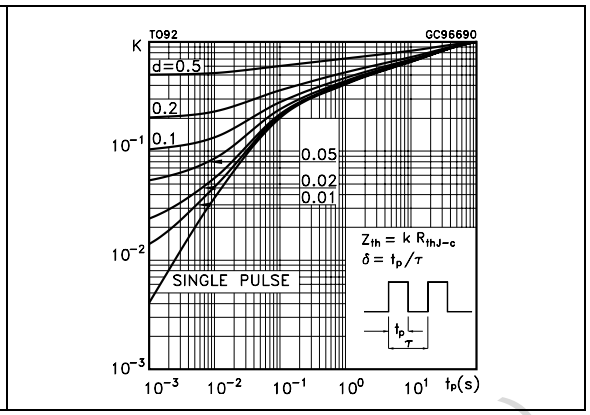


Figure 3. Output characteristics

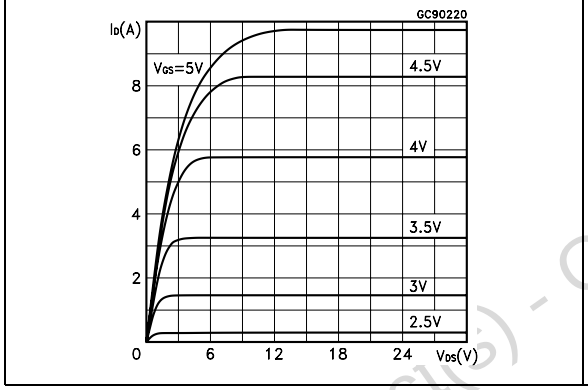


Figure 4. Transfer characteristics

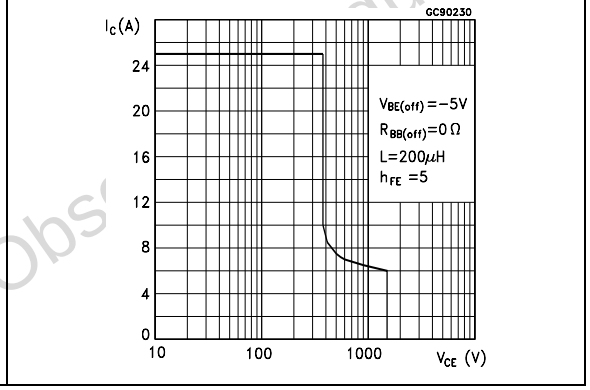


Figure 5. Transconductance

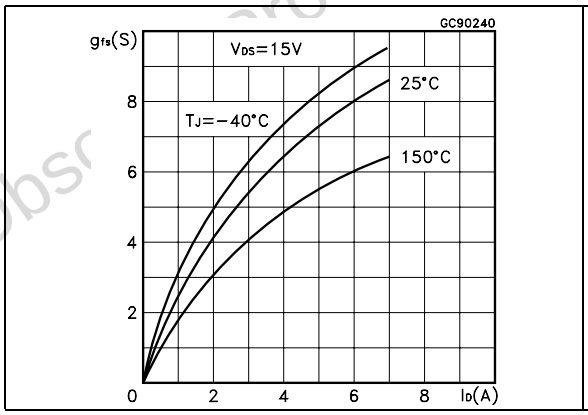


Figure 6. Static drain-source on resistance

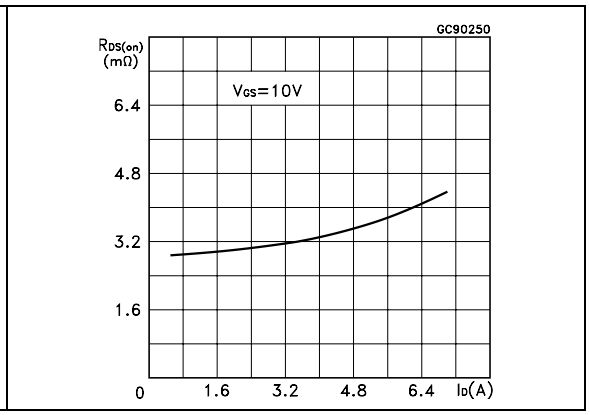


Figure 7. Gate charge vs. gate-source voltage

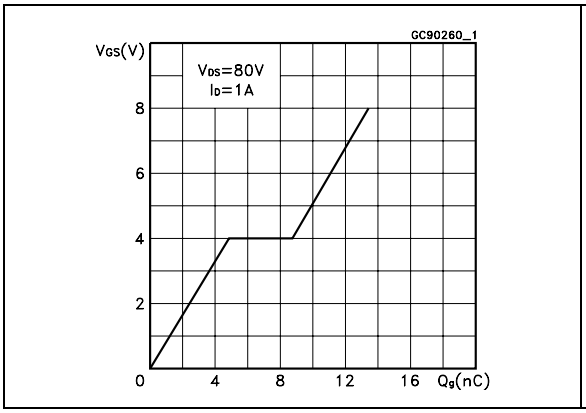


Figure 8. Capacitance variations

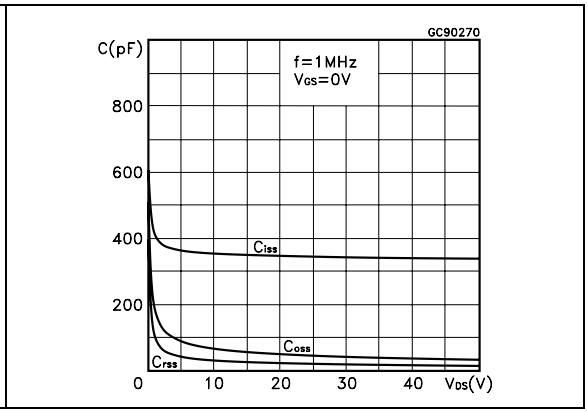


Figure 9. Normalized gate threshold voltage vs. temperature

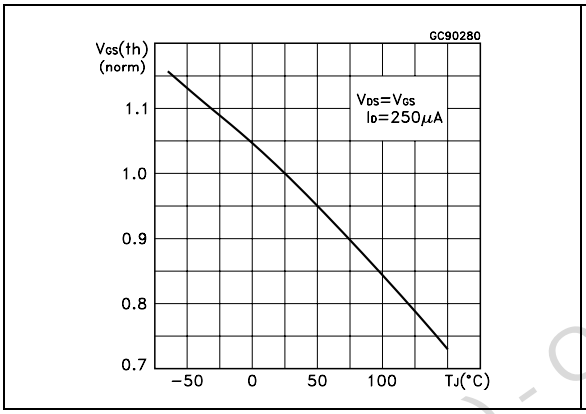


Figure 10. Normalized on resistance vs. temperature

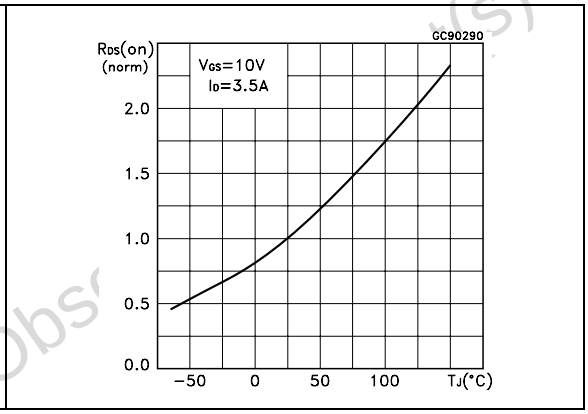
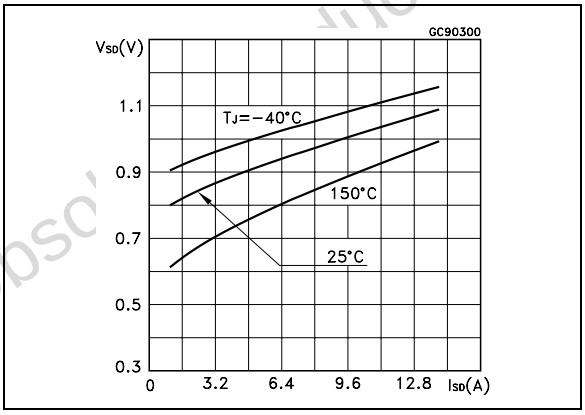


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

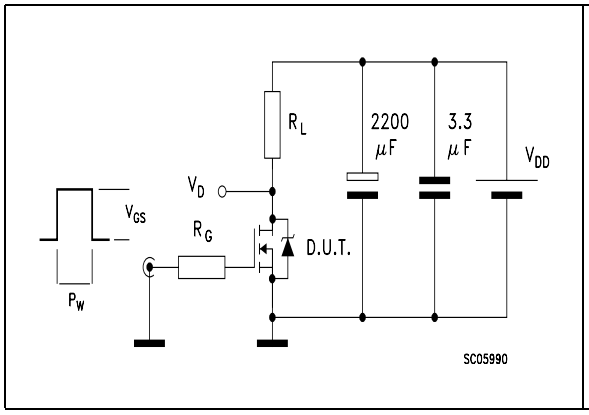


Figure 13. Gate charge test circuit

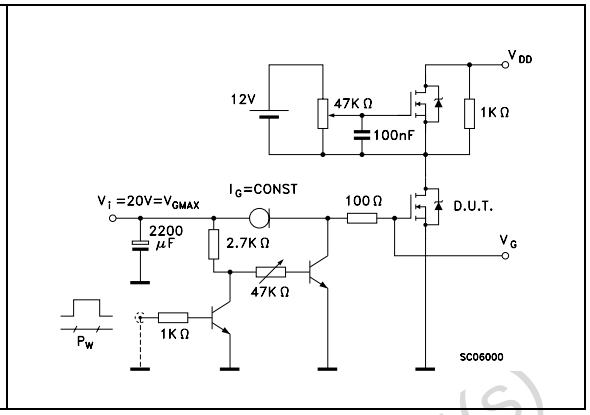


Figure 14. Test circuit for inductive load switching and diode recovery times

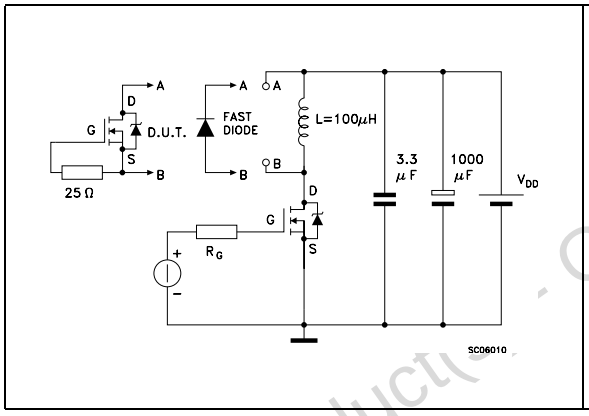


Figure 15. Unclamped Inductive load test circuit

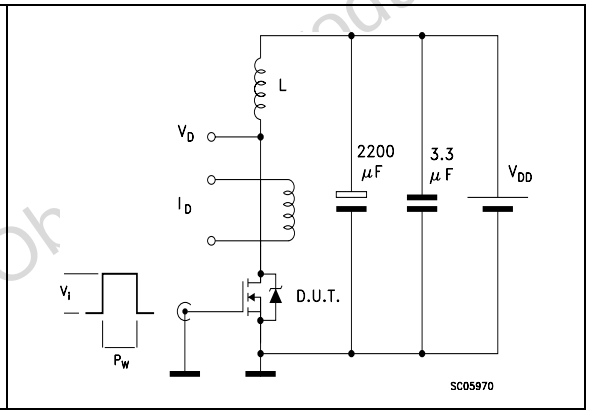
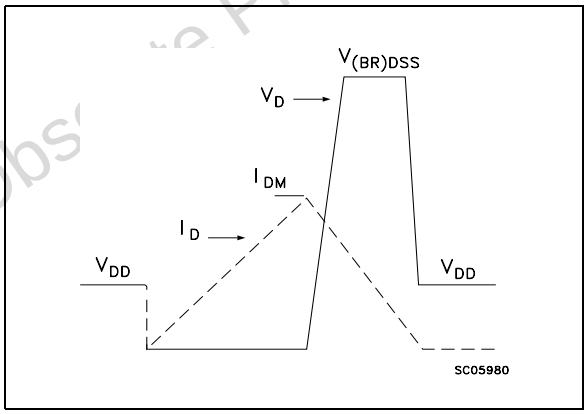


Figure 16. Unclamped inductive waveform

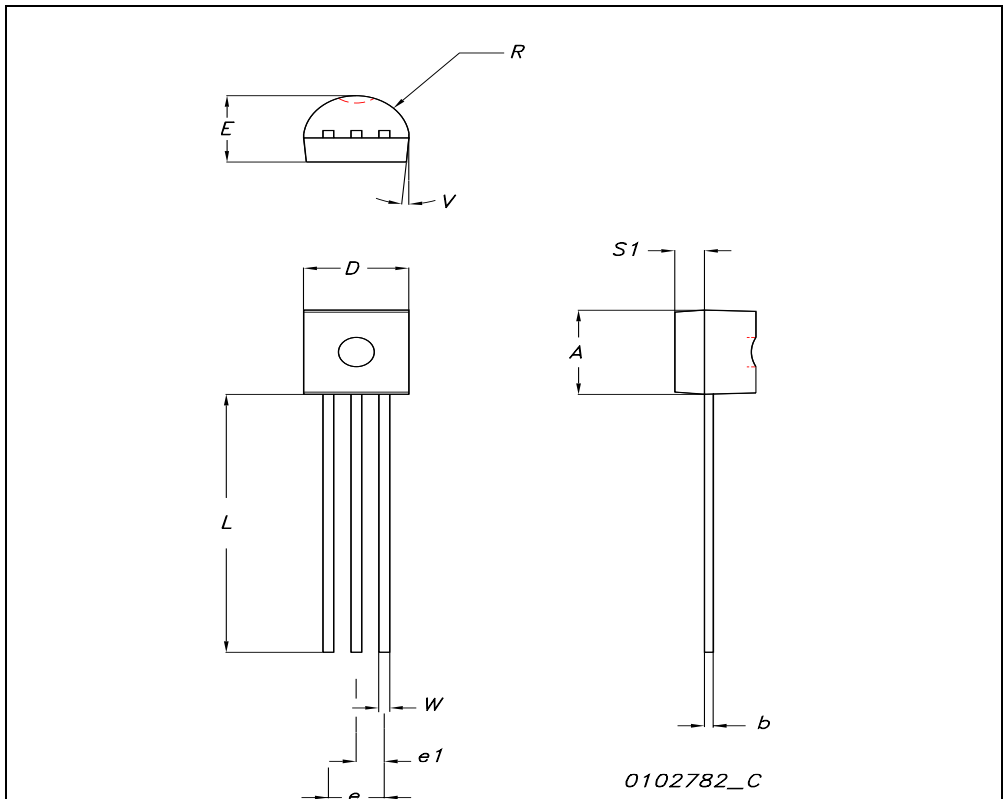


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

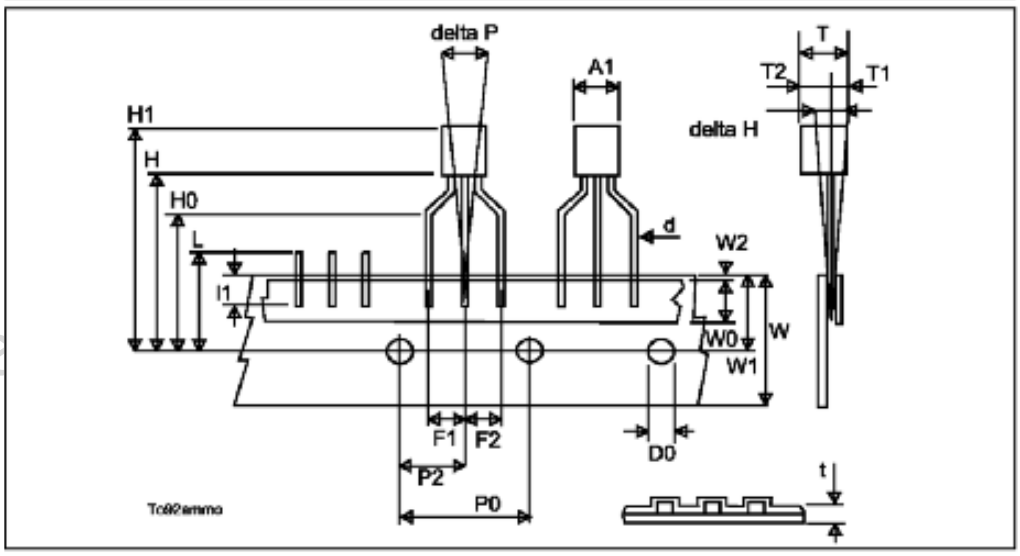
TO-92 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.32		4.95	0.170		0.194
b	0.36		0.51	0.014		0.020
D	4.45		4.95	0.175		0.194
E	3.30		3.94	0.130		0.155
e	2.41		2.67	0.094		0.105
e1	1.14		1.40	0.044		0.055
L	12.70		15.49	0.50		0.610
R	2.16		2.41	0.085		0.094
S1	0.92		1.52	0.036		0.060
W	0.41		0.56	0.016		0.022
V		5°			5°	



TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1			4.8			0.19
T			3.8			0.15
T1			1.6			0.06
T2			2.3			0.09
d			0.48			0.02
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
l1	3			0.11		
delta P	-1		1	-0.04		0.04



5 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2004	3	Complete version
31-Oct-2006	4	Document has been reformatted
31-Jan-2007	5	Typo mistake on *Table 1*.

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