SiliconMAX

PSMN063-150D

N-channel enhancement mode field-effect transistor

Rev. 03 — 31 October 2001 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS[1] technology.

Product availability:

PSMN063-150D in SOT428 (D-PAK).

1.2 Features

- TrenchMOS™ technology
- Fast Switching
- Very low on-state resistance
- Low thermal resistance

1.3 Applications

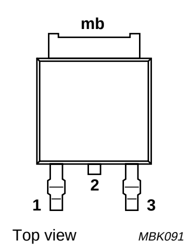
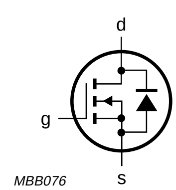
- DC to DC converters
- Switched mode power supplies

1.4 Quick reference data

- V_{DS} = 150 V
- P_{tot} = 150 W
- I_D = 29 A
- $R_{DSon} \leq$ 63 mΩ

2. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	connected to drain (d)		

[1] It is not possible to make a connection to pin 2 of the SOT428 package.

1. TrenchMOS™ is a trademark of Koninklijke Philips Electronics N.V.

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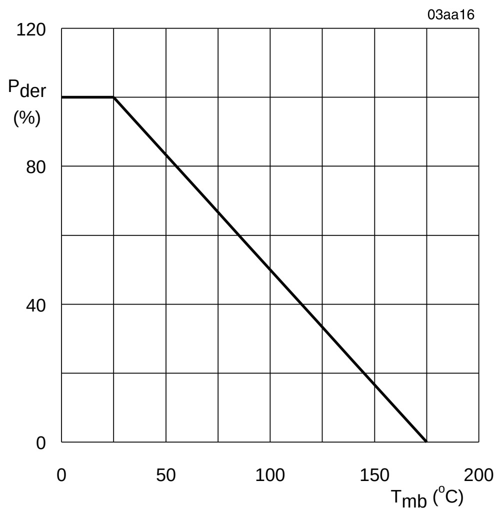
3. Limiting values

Table 2: Limiting values

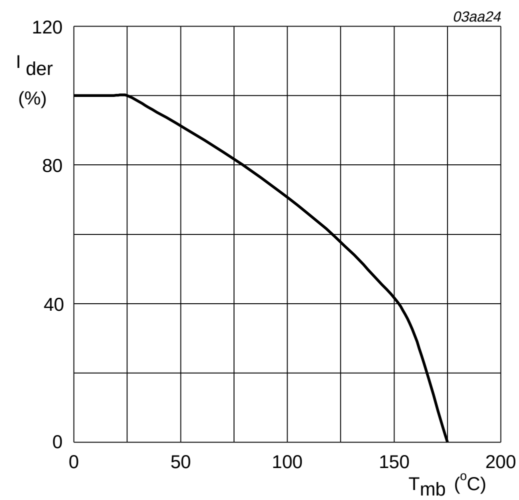
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 175 °C	–	150	V
V_{DGR}	drain-gate voltage (DC)	T_j = 25 to 175 °C; R_{GS} = 20 kΩ	–	150	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	–	29	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2 and 3	–	20	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3	–	116	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	–	150	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	–	29	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs	–	116	A
Avalanche ruggedness					
E_{AS}	non-repetitive avalanche energy	unclamped inductive load; I_D = 26 A; t_p = 0.2 ms; $V_{DD} \leq 25$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C	–	502	mJ
I_{AS}	non-repetitive avalanche current	unclamped inductive load; $V_{DD} \leq 25$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C	–	29	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

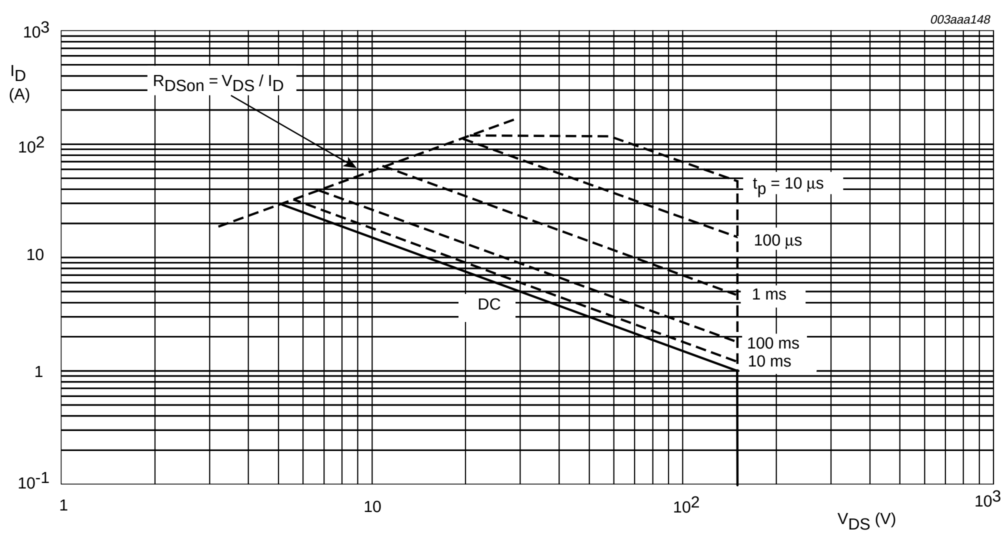
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	1.0	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Vertical in still air	50	K/W

4.1 Transient thermal impedance

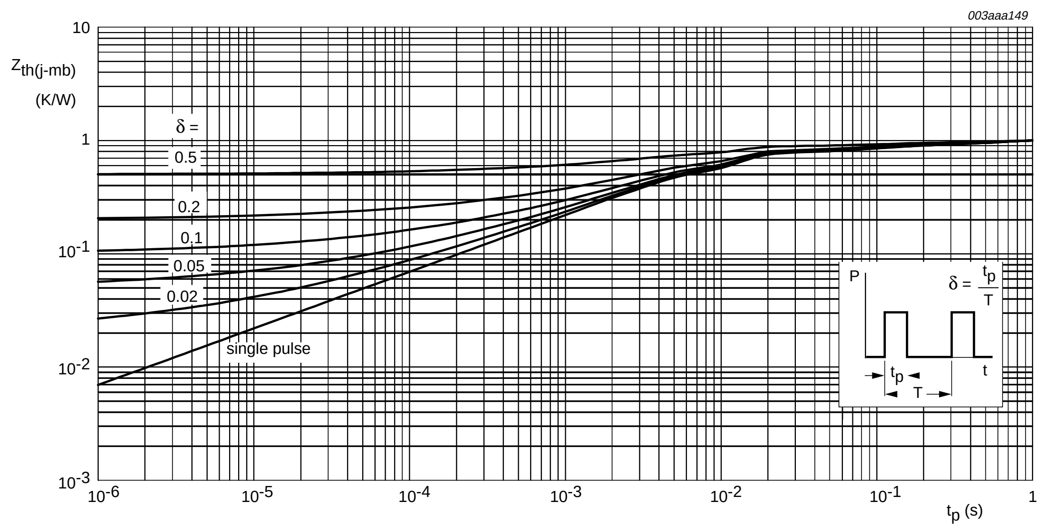


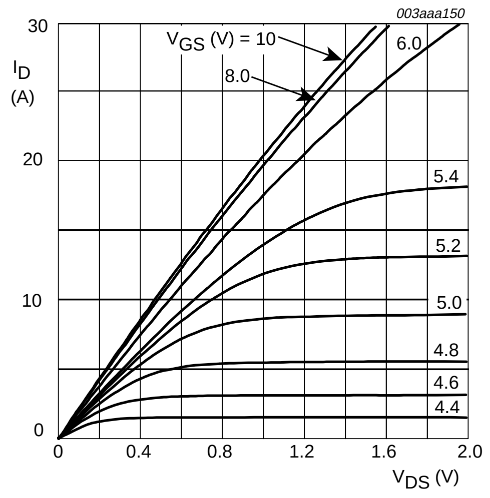
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

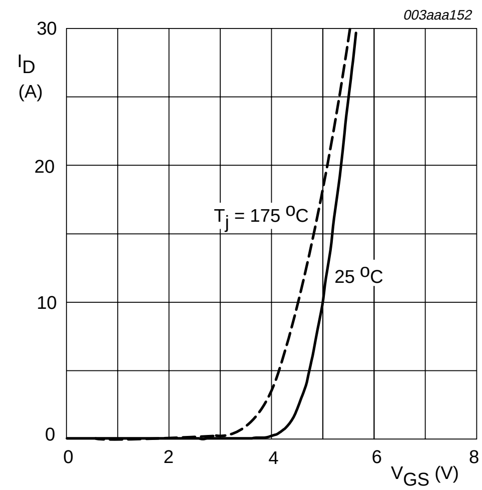
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	150	–	–	V
		T_j = –55 °C	133	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	–	–	V
		T_j = –55 °C	–	–	6	V
I_{DSS}	drain-source leakage current	V_{DS} = 150 V; V_{GS} = 0 V				
		T_j = 25 °C	–	0.05	10	µA
		T_j = 175 °C	–	–	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	–	0.02	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; Figure 7 and 8				
		T_j = 25 °C	–	60	63	mΩ
		T_j = 175 °C	–	–	176	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 30 A; V_{DS} = 120 V; V_{GS} = 10 V; Figure 14	–	55	–	nC
Q_{gs}	gate-source charge		–	10	–	nC
Q_{gd}	gate-drain (Miller) charge		–	20	27	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	–	2390	–	pF
C_{oss}	output capacitance		–	240	–	pF
C_{rss}	reverse transfer capacitance		–	98	–	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 75 V; R_D = 2.7 Ω; V_{GS} = 10 V; R_G = 5.6 Ω	–	14	–	ns
t_r	turn-on rise time		–	50	–	ns
$t_{d(off)}$	turn-off delay time		–	48	–	ns
t_f	turn-off fall time		–	38	–	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 13	–	0.9	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	–	105	–	ns
Q_r	recovered charge		–	0.55	–	µC



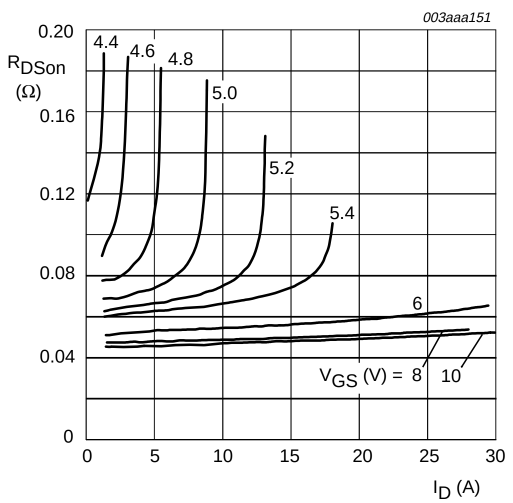
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



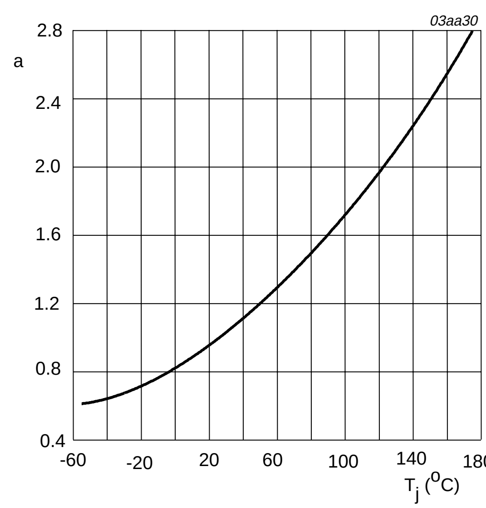
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



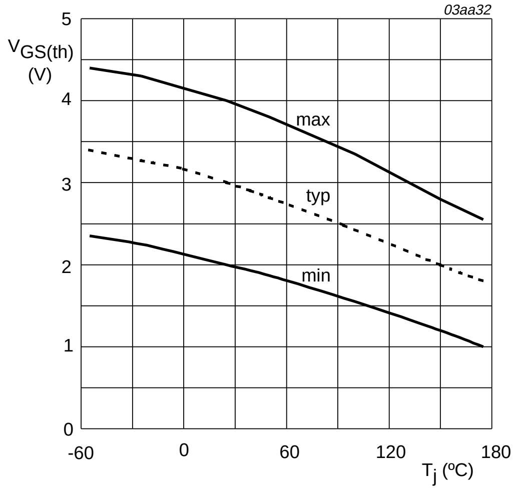
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



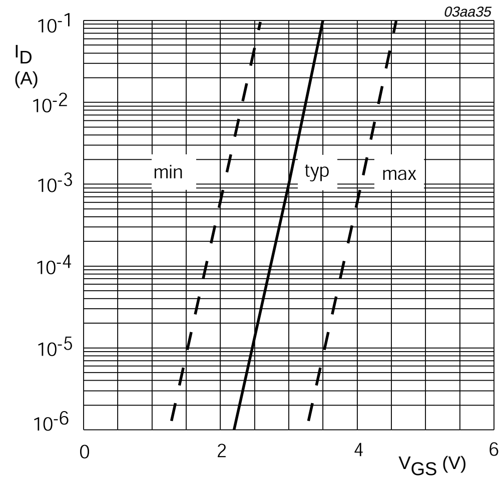
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



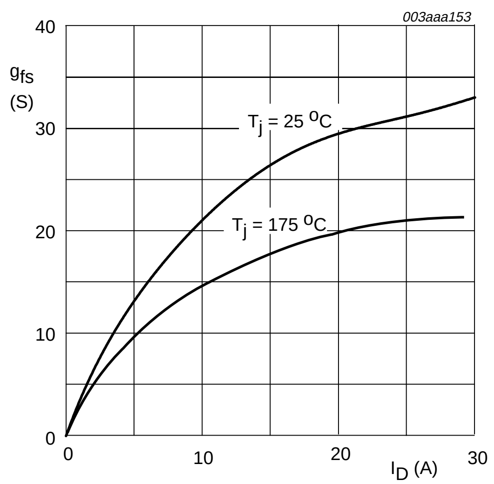
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



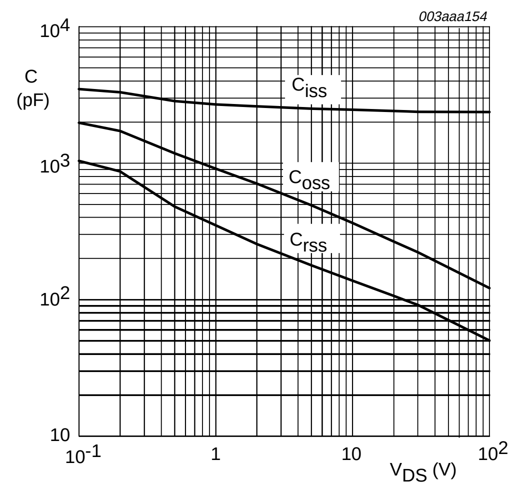
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



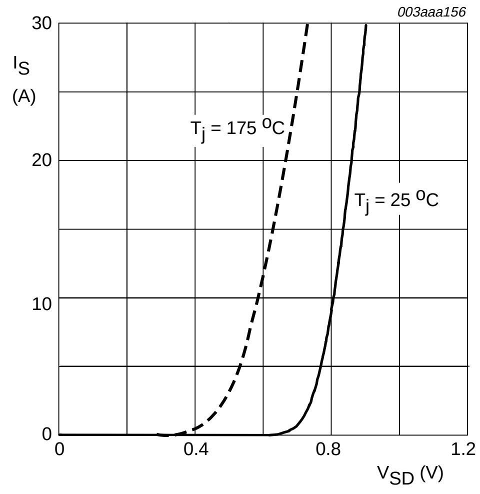
T_j = 25 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 11. Forward transconductance as a function of drain current; typical values.



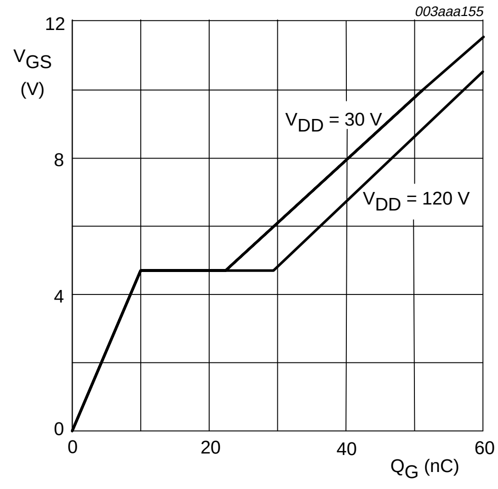
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

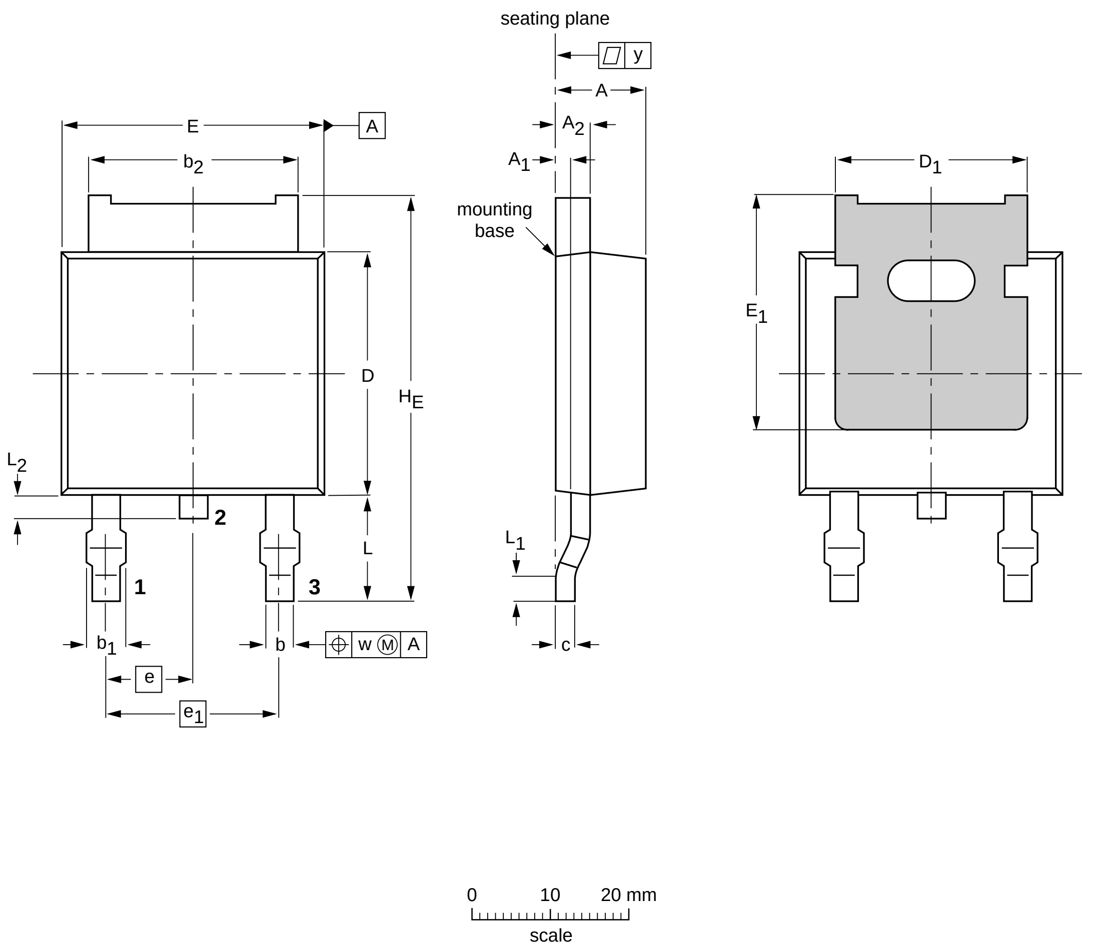


I_D = 30 A; V_{DD} = 30 V and 120 V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1(1)	A_2	b	b_1 max.	b_2	c	D max.	D_1 max.	E max.	E_1 min.	e	e_1	H_E max.	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428		TO-252	SC-63			~~98-04-07~~ 99-09-13

Fig 15. SOT428 (D-PAK).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
03	20011031	-	**Product data; third version; supersedes second version PSMN063_150D_2 of 1 August 1999.** • Max value of Q_{gd} added in table 5.
02	19990801	-	**Product specification; second version PSMN063_150D_2; supersedes initial Lotus Manuscript version of August 1999 Rev 1.000.**
01	-	-	**Initial version; not published.**

8. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

9. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 31 October 2001 **Document order number: 9397 750 08594**