Alaska® 88E1240 Technical Product Brief

Integrated 10/100/1000 Gigabit Ethernet Transceiver

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Integrated 10/100/1000 Gigabit Ethernet Transceiver

Overview

The Alaska® Quad family of single-chip devices contains four independent Gigabit Ethernet transceivers on a single monolithic IC. Each transceiver performs all the physical layer functions for 100BASE-TX and 1000BASE-T full or half-duplex Ethernet on CAT 5 twisted pair cable, and 10BASE-T full or half-duplex Ethernet on CAT 3, 4, and 5 cable.

The Alaska 88E1240 device supports the Serial Gigabit Media Independent Interface (SGMII) for direct connection to a MAC/Switch port.

The 88E1240 device is fully compliant with the IEEE 802.3 standard. The 88E1240 device includes the PMD, PMA, and PCS sublayers. The 88E1240 device performs PAM5, 8B/10B, 4B/5B, MLT-3, NRZI, and Manchester encoding/decoding; digital clock/data recovery; stream cipher scrambling/descrambling; digital adaptive equalization for the receiver data path as well as digital filtering for pulse-shaping for the line transmitter; and Auto-Negotiation and management functions.

The 88E1240 device support Auto-MDI/MDIX at all three speeds to enable easier installation and reduced installation costs.

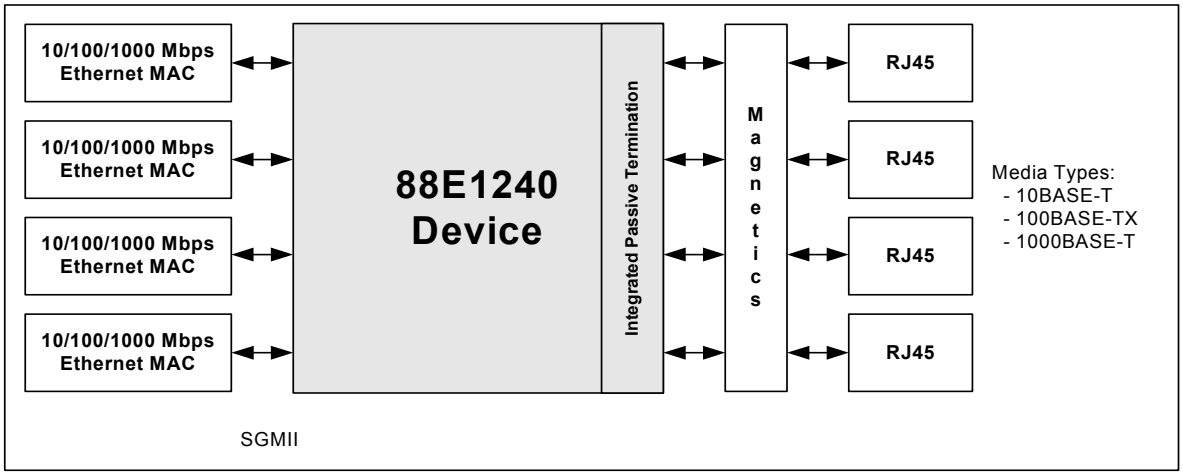
The 88E1240 device integrates MDI interface termination resistors into the PHY. This resistor integration facilitates board layout and reduces board cost by reducing the number of external components. The new Marvell® calibrated resistor scheme will achieve and exceed the accuracy requirements of the IEEE 802.3 return loss specifications.

The 88E1240 device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

The 88E1240 device is supported with an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

Features

- 10/100/1000BASE-T IEEE 802.3 compliant
- Highly integrated 4-port physical interface
- Supports Serial Gigabit Media Independent Interface (SGMII)
- Integrated MDI interface termination resistors
- Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature
- Programmable current source LED drivers
- "Downshift" mode for two-pair cable installations
- User programmable individual/group MDC/MDIO support
- Innovative power management design to reduce on-chip power by as much as 50%
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Automatic MDI/MDIX crossover for all 3 speeds of operation including 100BASE-TX and 10BASE-T
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Direct drive LED support
- Loopback mode for diagnostics
- Supports IEEE 1149.1 JTAG and 1149.6 AC JTAG
- Available in RoHS 6/6 compliant package
- Manufactured in a 15 x 15 mm 196-Pin TFBGA package



88E1240 Device Application

Table of Contents

Section 1. Signal Description

The 88E1240 device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

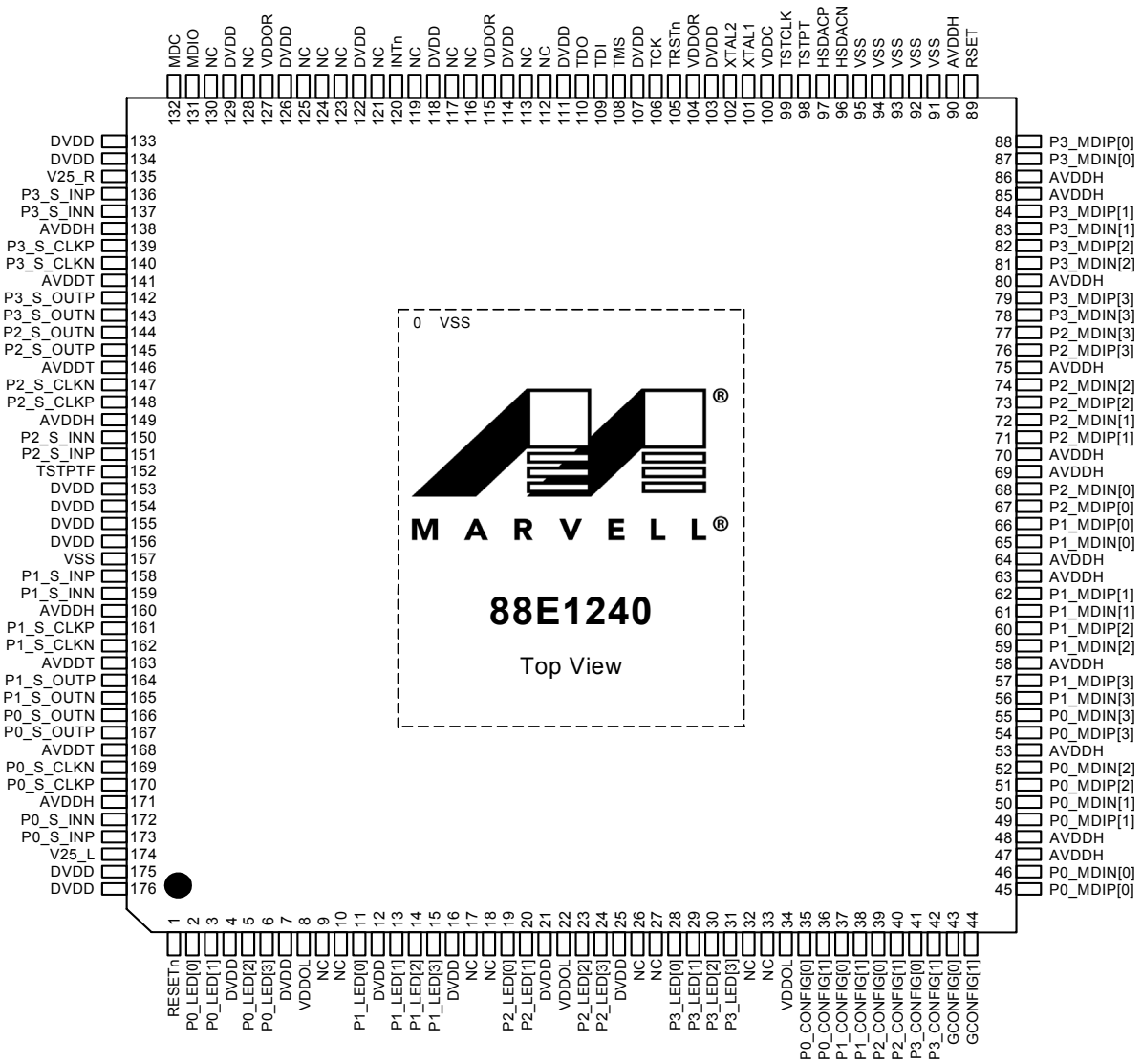
1.1 Pin Description

1.1.1 Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.2 88E1240 176-Pin TQFP Package

Figure 1: 88E1240 176-Pin TQFP Package (Top View)



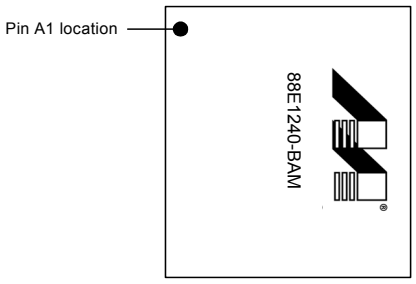
1.3 88E1240 196-Pin TFBGA Package

Due to the large number of pins, the 196-pin TFBGA package is depicted graphically over two facing pages.

	1	2	3	4	5	6	7	
A	NC	P0_S_INN	P0_S_CLKN	P0_S_OUTN	P1_S_OUTP	P1_S_CLKP	P1_S_INN	A
B	NC	P0_S_INP	P0_S_CLKP	P0_S_OUTP	P1_S_OUTN	P1_S_CLKN	P1_S_INP	B
C	P1_LED[0]	P0_LED[1]	P0_LED[0]	AVDDH	V25_L	VSS	AVDDH	C
D	P1_LED[1]	RESETn	P0_LED[3]	P0_LED[2]	AVDDT	AVDDT	DVDD	D
E	P1_LED[3]	P1_LED[2]	NC	VDDOL	VSS	VSS	VSS	E
F	NC	P2_LED[0]	DVDD	DVDD	VSS	VSS	VSS	F
G	P2_LED[1]	P2_LED[2]	DVDD	DVDD	VSS	VSS	VSS	G
H	P2_LED[3]	NC	VDDOL	VSS	VSS	VSS	VSS	H
J	NC	P3_LED[1]	P3_LED[0]	VSS	VSS	VSS	VSS	J
K	P3_LED[2]	P3_LED[3]	P0_ CONFIG[0]	VDDOL	VSS	VSS	VSS	K
L	NC	P2_ CONFIG[0]	P1_ CONFIG[0]	AVDDH	AVDDH	AVDDH	AVDDH	L
M	NC	P3_ CONFIG[1]	GCONFIG[1]	GCONFIG[0]	P0_MDIP[3]	P0_MDIN[3]	P1_MDIN[0]	M
N	P0_ CONFIG[1]	P3_ CONFIG[0]	P0_MDIP[0]	P0_MDIP[1]	P0_MDIN[2]	P1_MDIP[3]	P1_MDIP[2]	N
P	P1_ CONFIG[1]	P2_ CONFIG[1]	P0_MDIN[0]	P0_MDIN[1]	P0_MDIP[2]	P1_MDIN[3]	P1_MDIN[2]	P
	1	2	3	4	5	6	7	

(Top View)

Figure 2: Pin A1 Location



	8	9	10	11	12	13	14	
A	P2_S_INP	P2_S_CLKP	P2_S_OUTP	P3_S_OUTN	P3_S_CLKN	P3_S_INN	NC	A
B	P2_S_INN	P2_S_CLKN	P2_S_OUTN	P3_S_OUTP	P3_S_CLKP	P3_S_INP	NC	B
C	TSTPTF	AVDDH	V25_R	AVDDH	NC	NC	NC	C
D	DVDD	AVDDT	AVDDT	DVDD	MDIO	INTn	NC	D
E	VSS	VSS	VSS	VDDOR	MDC	NC	NC	E
F	VSS	VSS	VSS	DVDD	DVDD	NC	NC	F
G	VSS	VSS	VSS	DVDD	DVDD	TDO	NC	G
H	VSS	VSS	VSS	VDDOR	VDDOR	TDI	TMS	H
J	VSS	VSS	VSS	VSS	TCK	TRSTn	XTAL2	J
K	VSS	VSS	VSS	VSS	VDDC	TSTPT	XTAL1	K
L	AVDDH	AVDDH	AVDDH	AVDDH	AVDDH	RSET	TSTCLK	L
M	P1_MDIP[0]	P2_MDIP[3]	P2_MDIN[3]	P3_MDIN[1]	P3_MDIP[1]	HSDACN	HSDACP	M
N	P1_MDIP[1]	P2_MDIN[0]	P2_MDIN[1]	P2_MDIN[2]	P3_MDIP[3]	P3_MDIP[2]	P3_MDIP[0]	N
P	P1_MDIN[1]	P2_MDIP[0]	P2_MDIP[1]	P2_MDIP[2]	P3_MDIN[3]	P3_MDIN[2]	P3_MDIN[0]	P
	8	9	10	11	12	13	14	

(Top View)

Table 1: Media Dependent Interface Port 0

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
45 46	N3 P3	P0_MDIP[0] P0_MDIN[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. **NOTE:** Unused MDI pins must be left floating. The 88E1240 device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
49 50	N4 P4	P0_MDIP[1] P0_MDIN[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. **NOTE:** Unused MDI pins must be left floating. The 88E1240 device contains an internal 100 ohm resistor between the MDIP/N[1] pins.
51 52	P5 N5	P0_MDIP[2] P0_MDIN[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. **NOTE:** Unused MDI pins must be left floating. The 88E1240 device contains an internal 100 ohm resistor between the MDIP/N[2] pins.
54 55	M5 M6	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. **NOTE:** Unused MDI pins must be left floating. The 88E1240 device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

Table 2: Media Dependent Interface Port 1

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
66 65	M8 M7	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface[0] for Port 1. Refer to P0_MDI[0]P/N.
62 61	N8 P8	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface[1] for Port 1. Refer to P0_MDI[1]P/N.
60 59	N7 P7	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface[2] for Port 1. Refer to P0_MDI[2]P/N.
57 56	N6 P6	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface[3] for Port 1. Refer to P0_MDI[3]P/N.

Table 3: Media Dependent Interface Port 2

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
67 68	P9 N9	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface[0] for Port 2. Refer to P0_MDI[0]P/N.
71 72	P10 N10	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface[1] for Port 2. Refer to P0_MDI[1]P/N.
73 74	P11 N11	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface[2] for Port 2. Refer to P0_MDI[2]P/N.
76 77	M9 M10	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface[3] for Port 2. Refer to P0_MDI[3]P/N.

Table 4: Media Dependent Interface Port 3

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
88 87	N14 P14	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface[0] for Port 3. Refer to P0_MDI[0]P/N.
84 83	M12 M11	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface[1] for Port 3. Refer to P0_MDI[1]P/N.
82 81	N13 P13	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface[2] for Port 3. Refer to P0_MDI[2]P/N.
79 78	N12 P12	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface[3] for Port 3. Refer to P0_MDI[3]P/N.

Table 5: SGMII Interface Port 0

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
173 172	B2 A2	P0_S_INP P0_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
170 169	B3 A3	P0_S_CLKP P0_S_CLKN	O	SGMII 625 MHz Receive Clock output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0. The P0_S_CLKP/N pins should be left floating if not used.
167 166	B4 A4	P0_S_OUTP P0_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0.

Table 6: SGMII Interface Port 1

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
158 159	B7 A7	P1_S_INP P1_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
161 162	A6 B6	P1_S_CLKP P1_S_CLKN	O	SGMII 625 MHz Receive Clock output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0 The P1_S_CLKP/N pins should be left floating if not used.
164 165	A5 B5	P1_S_OUTP P1_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0.

Table 7: SGMII Interface Port 2

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
151 150	A8 B8	P2_S_INP P2_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
148 147	A9 B9	P2_S_CLKP P2_S_CLKN	O	SGMII 625 MHz Receive Clock output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0 The P2_S_CLKP/N pins should be left floating if not used.
145 144	A10 B10	P2_S_OUTP P2_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0.

Table 8: SGMII Interface Port 3

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
136 137	B13 A13	P3_S_INP P3_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
139 140	B12 A12	P3_S_CLKP P3_S_CLKN	O	SGMII 625 MHz Receive Clock output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0 The P3_S_CLKP/N pins should be left floating if not used.
142 143	B11 A11	P3_S_OUTP P3_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_2.2:0.

Table 9: Management Interface/Control

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
132	E12	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz.
131	D12	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.
120	D13	INTn	OD	Interrupt pin.

Table 10: JTAG

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
109	H13	TDI	I, PU	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
108	H14	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
106	J12	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
105	J13	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 kohm pull-down resistor.
110	G13	TDO	O	Boundary scan test data output.

Table 11: LED/Configuration

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
6 5 3 2	D3 D4 C2 C3	P0_LED[3] P0_LED[2] P0_LED[1] P0_LED[0]	O	Parallel LED Output port 0
15 14 13 11	E1 E2 D1 C1	P1_LED[3] P1_LED[2] P1_LED[1] P1_LED[0]	O	Parallel LED Output port 1
24 23 20 19	H1 G2 G1 F2	P2_LED[3] P2_LED[2] P2_LED[1] P2_LED[0]	O	Parallel LED Output port 2
31 30 29 28	K2 K1 J2 J3	P3_LED[3] P3_LED[2] P3_LED[1] P3_LED[0]	O	Parallel LED Output port 3
36 35	N1 K3	P0_CONFIG[1] P0_CONFIG[0]	I	Hardware configuration Port 0
38 37	P1 L3	P1_CONFIG[1] P1_CONFIG[0]	I	Hardware configuration Port 1
40 39	P2 L2	P2_CONFIG[1] P2_CONFIG[0]	I	Hardware configuration Port 2
42 41	M2 N2	P3_CONFIG[1] P3_CONFIG[0]	I	Hardware configuration Port 3
44 43	M3 M4	GCONFIG[1] GCONFIG[0]	I	Global hardware configuration
174	C5	V25_L	I	VDDOL voltage control. Tie to VSS = VDDOL operating at 2.5V/3.3V Floating = VDDOL operating at 1.8V
135	C10	V25_R	I	VDDOR voltage control. Tie to VSS = VDDOR operating at 2.5V/3.3V Floating = VDDOR operating at 1.8V

Table 12: Clock/Reset

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
101	K14	XTAL1	I	25 MHz Clock Input 25 MHz ± 50 ppm tolerance crystal reference or oscillator input. The XTAL1 input voltage should not exceed 1.8V+5%.
102	J14	XTAL2	O	25 MHz Crystal Output. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL2 pin is not connected, it should be left floating.
99	L14	TSTCLK	I	Test Clock. Must be tied to XTAL1.
1	D2	RESETn	I	Hardware reset. XTAL1 must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be in inactive state for normal operation. 1 = Normal operation 0 = Reset

Table 13: Test

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
97 96	M14 M13	HSDACP HSDACN	O	AC Test Point. Positive and Negative. These pins are also used to bring out a differential TX_TCLK. These pins can be connected to VSS through a 50 ohms termination resistor for IEEE testing and debug purposes. These pins maybe left floating if debug and IEEE testing are not of importance.
98	K13	TSTPT	O	DC Test Point. The TSTPT pin should be left floating if not used.
152	C8	TSTPTF	O	DC test point. The TSTPTF pin should be left floating if not used.

Table 14: Reference

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
89	L13	RSET	I	Resistor Reference External 5.0 kohm 1% resistor connected to ground.

Table 15: Power & Ground

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
4 7 12 16 21 25 103 107 111 114 118 122 126 129 133 134 153 154 155 156 175 176	D7 D8 D11 F3 F4 F11 F12 G3 G4 G11 G12	DVDD	Power	1.0V or 1.2V Digital Supply
47 48 53 58 63 64 69 70 75 80 85 86 90 138 149 160 171	C4 C7 C9 C11 L4 L5 L6 L7 L8 L9 L10 L11 L12	AVDDH	Power	1.8V Analog Supply.
100	K12	VDDC	Power	1.8V XTAL Supply. The maximum input voltage is 1.8V +5%.
141 146 163 168	D5 D6 D9 D10	AVDDT	Power	SGMII Output Supply
8 22 34	E4 H3 K4	VDDOL	Power	1.8V, 2.5V, or 3.3V I/O Supply[1].
104 115 127	E11 H11 H12	VDDOR	Power	1.8V, 2.5V, or 3.3V I/O Supply[2].

Table 15: Power & Ground (Continued)

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
EPAD	--	VSS	Ground	Ground to device. The 176-TQFP package contains an exposed die pad (E-PAD) at its base. The EPAD must be soldered to VSS. The location and dimensions of the EPAD can be found in Section 2.1 and Table 19, respectively.
91 92 93 94 95 157	C6 E5 E6 E7 E8 E9 E10 F5 F6 F7 F8 F9 F10 G5 G6 G7 G8 G9 G10 H4 H5 H6 H7 H8 H9 H10 J4 J5 J6 J7 J8 J9 J10 J11 K5 K6 K7 K8 K9 K10 K11	VSS	Ground	Ground

1. VDDOL supplies digital I/O pins for RESETn, LED, CONFIG, and GCONFIG.
2. VDDOR supplies digital I/O pins for MDC, MDIO, INTn, TDO, TDI, TMS, TCK, and TRST.

Table 16: No Connect

176-TQFP Pin #	196-TFBGA Pin #	Pin Name	Pin Type	Description
9	A1	NC	NC	These pins are not bonded to the die.
10	B1			
17	F1			
18	J1			
26	L1			
27	M1			
32	H2			
33	E3			
112	C12			
113	C13			
116	E13			
117	A14			
119	B14			
121	C14			
123	D14			
124	E14			
125	F13			
128	F14			
130	G14			

1.4 88E1240 176-TQFP Pin Assignment List—by Signal Name

Table 17: Package Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
47	AVDDH
48	AVDDH
53	AVDDH
58	AVDDH
63	AVDDH
64	AVDDH
69	AVDDH
70	AVDDH
75	AVDDH
80	AVDDH
85	AVDDH
86	AVDDH
90	AVDDH
138	AVDDH
149	AVDDH
160	AVDDH
171	AVDDH
141	AVDDT
146	AVDDT
163	AVDDT
168	AVDDT
4	DVDD
7	DVDD
12	DVDD
16	DVDD
21	DVDD
25	DVDD
103	DVDD
107	DVDD
111	DVDD
114	DVDD
118	DVDD
122	DVDD
126	DVDD
129	DVDD
133	DVDD
134	DVDD
153	DVDD
154	DVDD
155	DVDD
156	DVDD
175	DVDD
176	DVDD
43	GCONFIG[0]
44	GCONFIG[1]
96	HSDACN
97	HSDACP
120	INTn
132	MDC
131	MDIO
9	NC
10	NC
17	NC
18	NC
26	NC
27	NC
32	NC
33	NC
112	NC
113	NC
116	NC
117	NC
119	NC
121	NC

Pin Number	Pin Name
123	NC
124	NC
125	NC
128	NC
130	NC
35	P0_CONFIG[0]
36	P0_CONFIG[1]
2	P0_LED[0]
3	P0_LED[1]
5	P0_LED[2]
6	P0_LED[3]
46	P0_MDIN[0]
50	P0_MDIN[1]
52	P0_MDIN[2]
55	P0_MDIN[3]
45	P0_MDIP[0]
49	P0_MDIP[1]
51	P0_MDIP[2]
54	P0_MDIP[3]
169	P0_S_CLKN
170	P0_S_CLKP
172	P0_S_INN
173	P0_S_INP
166	P0_S_OUTN
167	P0_S_OUTP
37	P1_CONFIG[0]
38	P1_CONFIG[1]
11	P1_LED[0]
13	P1_LED[1]
14	P1_LED[2]
15	P1_LED[3]
65	P1_MDIN[0]
61	P1_MDIN[1]
59	P1_MDIN[2]
56	P1_MDIN[3]

Pin Number	Pin Name
66	P1_MDIP[0]
62	P1_MDIP[1]
60	P1_MDIP[2]
57	P1_MDIP[3]
162	P1_S_CLKN
161	P1_S_CLKP
159	P1_S_INN
158	P1_S_INP
165	P1_S_OUTN
164	P1_S_OUTP
39	P2_CONFIG[0]
40	P2_CONFIG[1]
19	P2_LED[0]
20	P2_LED[1]
23	P2_LED[2]
24	P2_LED[3]
68	P2_MDIN[0]
72	P2_MDIN[1]
74	P2_MDIN[2]
77	P2_MDIN[3]
67	P2_MDIP[0]
71	P2_MDIP[1]
73	P2_MDIP[2]
76	P2_MDIP[3]
147	P2_S_CLKN
148	P2_S_CLKP
150	P2_S_INN
151	P2_S_INP
144	P2_S_OUTN
145	P2_S_OUTP
41	P3_CONFIG[0]
42	P3_CONFIG[1]
28	P3_LED[0]
29	P3_LED[1]
30	P3_LED[2]

Pin Number	Pin Name
31	P3_LED[3]
87	P3_MDIN[0]
83	P3_MDIN[1]
81	P3_MDIN[2]
78	P3_MDIN[3]
88	P3_MDIP[0]
84	P3_MDIP[1]
82	P3_MDIP[2]
79	P3_MDIP[3]
140	P3_S_CLKN
139	P3_S_CLKP
137	P3_S_INN
136	P3_S_INP
143	P3_S_OUTN
142	P3_S_OUTP
1	RESETn
89	RSET
106	TCK
109	TDI
110	TDO
108	TMS
105	TRSTn
99	TSTCLK
98	TSTPT
152	TSTPTF
174	V25_L
135	V25_R
100	VDDC
8	VDDOL
22	VDDOL
34	VDDOL
104	VDDOR
115	VDDOR
127	VDDOR
91	VSS

Pin Number	Pin Name
92	VSS
93	VSS
94	VSS
95	VSS
157	VSS
101	XTAL1
102	XTAL2

1.5 88E1240 196-TFBGA Pin Assignment List—by Signal Name

Table 18: Package Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
C11	AVDDH
C4	AVDDH
C7	AVDDH
C9	AVDDH
L10	AVDDH
L11	AVDDH
L12	AVDDH
L4	AVDDH
L5	AVDDH
L6	AVDDH
L7	AVDDH
L8	AVDDH
L9	AVDDH
D10	AVDDT
D5	AVDDT
D6	AVDDT
D9	AVDDT
C5	C25_L
D11	DVDD
D7	DVDD
D8	DVDD
F11	DVDD
F12	DVDD
F3	DVDD
F4	DVDD
G11	DVDD
G12	DVDD
G3	DVDD
G4	DVDD
M4	GCONFIG[0]
M3	GCONFIG[1]
M13	HSDACN
M14	HSDACP
D13	INTn
E12	MDC
D12	MDIO
A1	NC
A14	NC
B1	NC
B14	NC
C12	NC
C13	NC
C14	NC
D14	NC
E13	NC
E14	NC
E3	NC
F1	NC
F13	NC
F14	NC
G14	NC
H2	NC
J1	NC
L1	NC
M1	NC
K3	P0_CONFIG[0]
N1	P0_CONFIG[1]
C3	P0_LED[0]
C2	P0_LED[1]
D4	P0_LED[2]
D3	P0_LED[3]
P3	P0_MDIN[0]
P4	P0_MDIN[1]
N5	P0_MDIN[2]

Pin Number	Pin Name
M6	P0_MDIN[3]
N3	P0_MDIP[0]
N4	P0_MDIP[1]
P5	P0_MDIP[2]
M5	P0_MDIP[3]
A3	P0_S_CLKN
B3	P0_S_CLKP
A2	P0_S_INN
B2	P0_S_INP
A4	P0_S_OUTN
B4	P0_S_OUTP
L3	P1_CONFIG[0]
P1	P1_CONFIG[1]
C1	P1_LED[0]
D1	P1_LED[1]
E2	P1_LED[2]
E1	P1_LED[3]
M7	P1_MDIN[0]
P8	P1_MDIN[1]
P7	P1_MDIN[2]
P6	P1_MDIN[3]
M8	P1_MDIP[0]
N8	P1_MDIP[1]
N7	P1_MDIP[2]
N6	P1_MDIP[3]
B6	P1_S_CLKN
A6	P1_S_CLKP
A7	P1_S_INN
B7	P1_S_INP
B5	P1_S_OUTN
A5	P1_S_OUTP
L2	P2_CONFIG[0]
P2	P2_CONFIG[1]
F2	P2_LED[0]
G1	P2_LED[1]

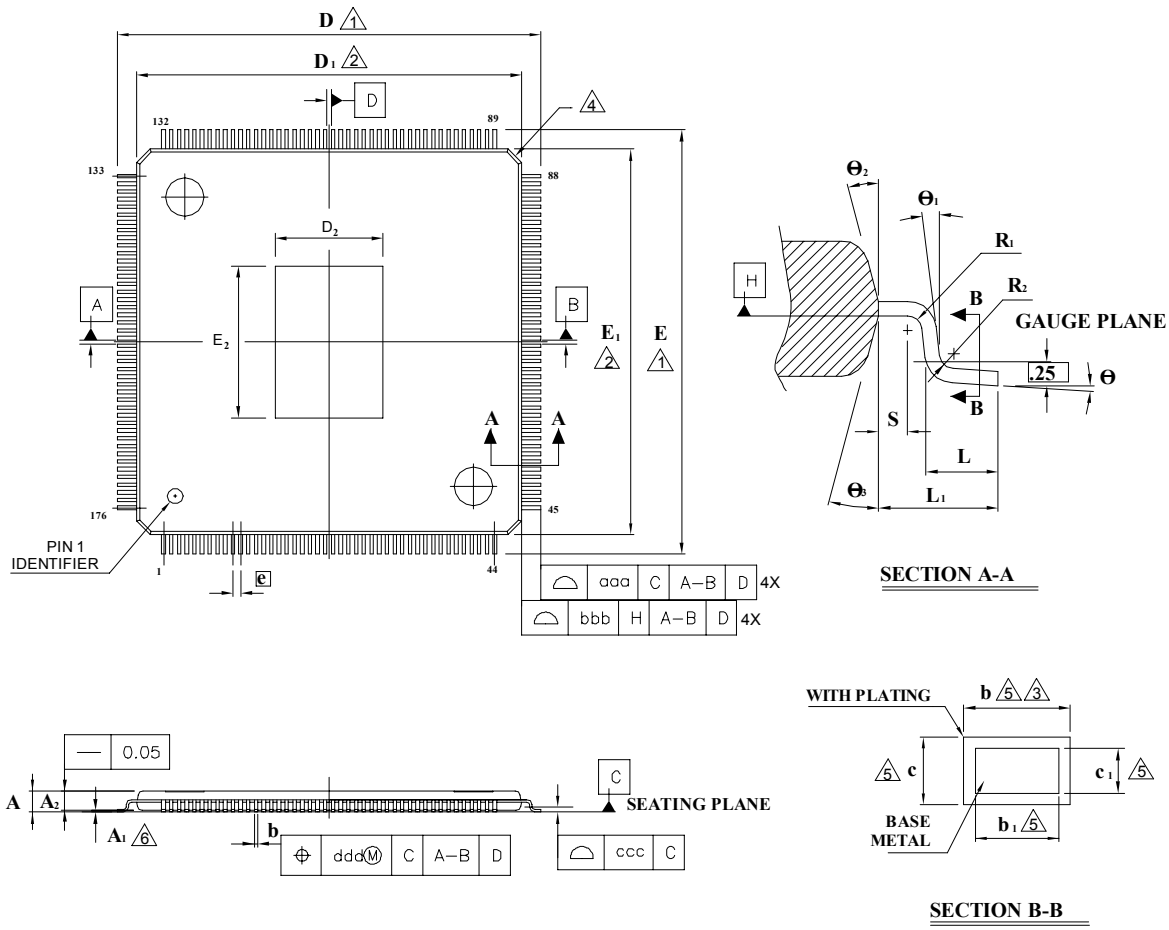
Pin Number	Pin Name
G2	P2_LED[2]
H1	P2_LED[3]
N9	P2_MDIN[0]
N10	P2_MDIN[1]
N11	P2_MDIN[2]
M10	P2_MDIN[3]
P9	P2_MDIP[0]
P10	P2_MDIP[1]
P11	P2_MDIP[2]
M9	P2_MDIP[3]
B9	P2_S_CLKN
A9	P2_S_CLKP
B8	P2_S_INN
A8	P2_S_INP
B10	P2_S_OUTN
A10	P2_S_OUTP
N2	P3_CONFIG[0]
M2	P3_CONFIG[1]
J3	P3_LED[0]
J2	P3_LED[1]
K1	P3_LED[2]
K2	P3_LED[3]
P14	P3_MDIN[0]
M11	P3_MDIN[1]
P13	P3_MDIN[2]
P12	P3_MDIN[3]
N14	P3_MDIP[0]
M12	P3_MDIP[1]
N13	P3_MDIP[2]
N12	P3_MDIP[3]
A12	P3_S_CLKN
B12	P3_S_CLKP
A13	P3_S_INN
B13	P3_S_INP
A11	P3_S_OUTN

Pin Number	Pin Name
B11	P3_S_OUTP
D2	RESETn
L13	RSET
J12	TCK
H13	TDI
G13	TDO
H14	TMS
J13	TRSTn
L14	TSTCLK
K13	TSTPT
C8	TSTPTF
C10	V25_R
K12	VDDC
E4	VDDOL
H3	VDDOL
K4	VDDOL
E11	VDDOR
H11	VDDOR
H12	VDDOR
C6	VSS
E10	VSS
E5	VSS
E6	VSS
E7	VSS
E8	VSS
E9	VSS
F10	VSS
F5	VSS
F6	VSS
F7	VSS
F8	VSS
F9	VSS

Pin Number	Pin Name
G10	VSS
G5	VSS
G6	VSS
G7	VSS
G8	VSS
G9	VSS
H10	VSS
H4	VSS
H5	VSS
H6	VSS
H7	VSS
H8	VSS
H9	VSS
J10	VSS
J11	VSS
J4	VSS
J5	VSS
J6	VSS
J7	VSS
J8	VSS
J9	VSS
K10	VSS
K11	VSS
K5	VSS
K6	VSS
K7	VSS
K8	VSS
K9	VSS
K14	XTAL1
J14	XTAL2

Section 2. Mechanical Drawings

2.1 88E1240 176-Pin TQFP Package Drawing



NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
   INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD
   BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE
   TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Table 19: 176-Pin TQFP Package Dimensions (mm)

Symbol	Dimension in mm		
	Min	Nom	Max
A	1.00	1.10	1.20
A_1	0.05	0.10	0.15
A_2	0.95	1.00	1.05
b	0.13	0.18	0.23
b_1	0.13	0.16	0.19
c	0.09	—	0.20
c_1	0.09	—	0.16
D	22.00 BSC		
D_1	20.00 BSC		
E	22.00 BSC		
E_1	20.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	—	—
R_2	0.08	—	0.20
S	0.20	—	—
θ	0°	3.5°	7°
$θ_1$	0°	—	—
$θ_2$	11°	12°	13°
$θ_3$	11°	12°	13°
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.07		

Symbol	Dimension in mm
D_2	4.01 BSC
E_2	6.86 BSC

2.2 88E1240 196-Pin TFBGA Package Drawing

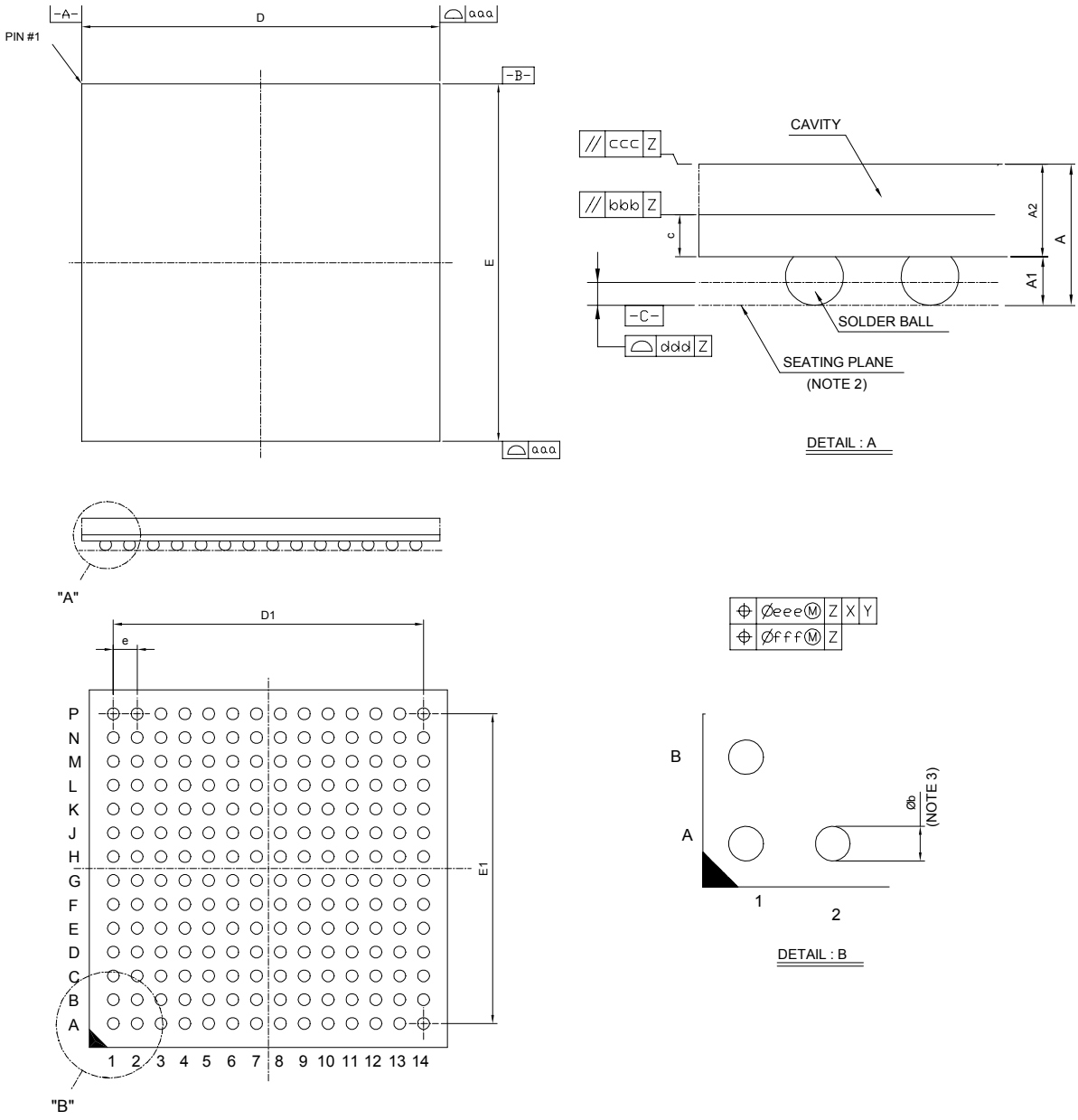


Table 20: 196-Pin TFBGA Package Dimensions (mm)

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.50
A1	0.30	0.40	0.50
A2	---	0.89	---
c	---	0.36	---
D	14.90	15.00	15.10
E	14.90	15.00	15.10
D1	---	13.00	---
E1	---	13.00	---
e	---	1.00	---
b	0.40	0.50	0.60
aaa	0.20		
bbb	0.25		
ccc	0.35		
ddd	0.12		
eee	0.25		
fff	0.10		
MD/ME	14/14		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

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