Alaska® 88E1118R Technical Product Brief

Gigabit Ethernet Transceiver

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OVERVIEW

The Alaska® 88E1118R Gigabit Ethernet Transceiver is a physical layer device containing a single Gigabit Ethernet transceiver. The transceiver implements the Ethernet physical layer portion of the 1000BASE-T, 100BASE-TX, and 10BASE-T standards. It is manufactured using standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 5 unshielded twisted pair.

The 88E1118R device supports the RGMII (Reduced pin count GMII) for direct connection to a MAC/Switch port.

The 88E1118R device integrates MDI interface termination resistors into the PHY. This resistor integration simplifies board layout and reduces board cost by reducing the number of external components. The new Marvell® calibrated resistor scheme will achieve and exceed the accuracy requirements of the IEEE 802.3 return loss specifications.

The 88E1118R device can run off a single 1.8V, 2.5V, or 3.3V supply. Alternatively if the regulators are not used then the 88E1118R device can run off 1.8V and 1.2V supply.

The 88E1118R device has two regulators to generate all required voltages. The 88E1118R device supports 1.8V, 2.5V, and 3.3V HSTL/SSTL and 2.5V LVCMOS I/O Standards

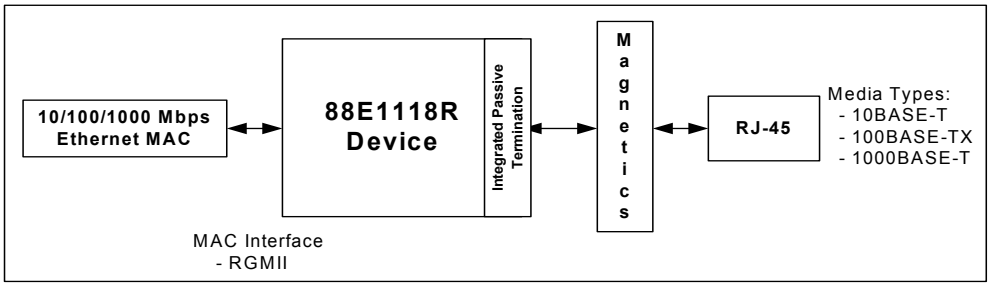
The 88E1118R device incorporates the Marvell® Virtual Cable Tester® (VCT™) feature, which uses Time Domain Reflectometry (TDR) technology for the remote identification of potential cable malfunctions, thus reducing equipment returns and service calls. Using VCT, the Alaska 88E1118R device detects and reports potential cabling issues such as pair swaps, pair polarity and excessive pair skew. The device will also detect cable opens, shorts or any impedance mismatch in the cable and reporting accurately within one meter the distance to the fault.

The 88E1118R device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

FEATURES

- 10/100/1000BASE-T IEEE 802.3 compliant
- Four RGMII timing modes - This eliminates the need for adding trace delays on the PCB
- Supports LVCMOS, SSTL, and HSTL I/O Standards on the RGMII interface
- Integrated MDI interface termination resistors that eliminate twelve passive components
- Energy Detect and Energy Detect+ low power modes
- Three loopback modes for diagnostics
- “Downshift” mode for two-pair cable installations
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic MDI/MDIX crossover at all speeds of operation
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes including LED testing
- Supports IEEE 1149.1 JTAG
- MDC/MDIO Management Interface
- CRC checker, packet counter
- Packet generation
- Virtual Cable Tester (VCT)
- Auto-Calibration for MAC Interface outputs
- 125 MHz Clock Output
- Requires a single 1.8V supply
- I/O pads can be supplied with 1.8V, 2.5V, or 3.3V
- Two regulators generate all required voltages. Regulator can be supplied with 1.8V, 2.5V or 3.3V.
- Commercial grade
- 64-Pin QFN package

88E1118R Device used in Copper Application



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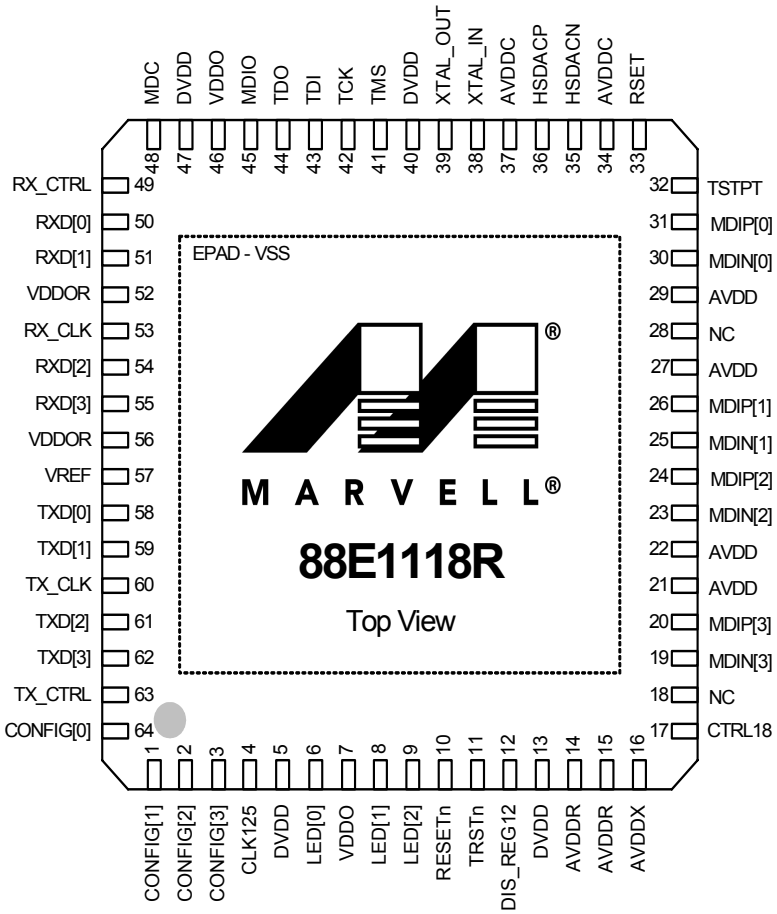
Section 1. Signal Description

The 88E1118R device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

Figure 1: 88E1118R Device 64-Pin QFN Package (Top View)



1.1 Pin Description

1.1.1 Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull up
PD	Internal pull down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

Table 1: Media Dependent Interface

64-QFN Pin #	Pin Name	Pin Type	Description
30 31	MDIN[0] MDIP[0]	I/O, D	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIN/P[0] correspond to BI_DA±. In MDIX configuration, MDIN/P[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[0] are used for the transmit pair. In MDIX configuration, MDIN/P[0] are used for the receive pair. “The unused MDI pins cannot be connected to ground. They need to be left floating, because they have internal bias.The 88E1118R device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
25 26	MDIN[1] MDIP[1]	I/O, D	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIN/P[1] correspond to BI_DB±. In MDIX configuration, MDIN/P[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[1] are used for the receive pair. In MDIX configuration, MDIN/P[1] are used for the transmit pair. “The unused MDI pins cannot be connected to ground. They need to be left floating, because they have internal bias.The 88E1118R device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
23 24	MDIN[2] MDIP[2]	I/O, D	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIN/P[2] correspond to BI_DC±. In MDIX configuration, MDIN/P[2] corresponds to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIN/P[2] are not used. “The unused MDI pins cannot be connected to ground. They need to be left floating, because they have internal bias.The 88E1118R device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
19 20	MDIN[3] MDIP[3]	I/O, D	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIN/P[3] correspond to BI_DD±. In MDIX configuration, MDIN/P[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIN/P[3] are not used. “The unused MDI pins cannot be connected to ground. They need to be left floating, because they have internal bias.The 88E1118R device contains an internal 100 ohm resistor between the MDIP/N[0] pins.

The RGMII interface supports 10/100/1000BASE-T mode of operation.

Table 2: RGMII Interface

64-QFN Pin #	Pin Name	Pin Type	Description
60	TX_CLK	I	RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed.
63	TX_CTRL	I	RGMII Transmit Control. TX_EN is presented on the rising edge of TX_CLK. A logical derivative of TX_EN and TX_ER is presented on the falling edge of TX_CLK.
62 61 59 58	TXD[3] TXD[2] TXD[1] TXD[0]	I	RGMII Transmit Data. TXD[3:0] run at double data rate with bits [3:0] presented on the rising edge of TX_CLK, and bits [7:4] presented on the falling edge of TX_CLK. In 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of TX_CLK.
53	RX_CLK	O	RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed.
49	RX_CTRL	O	RGMII Receive Control. RX_DV is presented on the rising edge of RX_CLK. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK.
55 54 51 50	RXD[3] RXD[2] RXD[1] RXD[0]	O	RGMII Receive Data. RXD[3:0] run at double data rate with bits [3:0] presented on the rising edge of RX_CLK, and bits [7:4] presented on the falling edge of RX_CLK. In 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK.

Table 3: Management Interface and Interrupt

64-QFN Pin #	Pin Name	Pin Type	Description
48	MDC	I	MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz.
45	MDIO	I/O	MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.

Table 4: LED Interface

64-QFN Pin #	Pin Name	Pin Type	Description
6 8 9	LED[0] LED[1] LED[2]	O	LED/Interrupt outputs.

Table 5: JTAG Interface

64-QFN Pin #	Pin Name	Pin Type	Description
43	TDI	I	Boundary scan test data input.
41	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
42	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
11	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor as per the 1149.1 specification. After power up, the JTAG state machine should be reset by applying a low signal on this pin, or by keeping TMS high and applying 5 TCK pulses, or by pulling this pin low by a 4.7 kohm resistor.
44	TDO	O	Boundary scan test data output.

Table 6: Clock/Configuration/Reset/I/O

64-QFN Pin #	Pin Name	Pin Type	Description
64	CONFIG[0]	I	Hardware Configuration
1	CONFIG[1]	I	Hardware Configuration
2	CONFIG[2]	I	Hardware Configuration
3	CONFIG[3]	I	Hardware Configuration
4	CLK125	O	125 MHz Clock Output. When Hardware reset is asserted, a 25 MHz clock is generated output, otherwise a 125 MHz clock is output.
38	XTAL_IN	I	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference or oscillator input. **NOTE:** If AVDDC is tied to 1.8V, then the XTAL_IN pin is not 2.5V/3.3V tolerant. If AVDDC is tied to 2.5V, then the XTAL_IN pin is not 3.3V tolerant.
39	XTAL_OUT	0	Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating.
10	RESETn	I	Hardware reset. Active low. 0 = Reset 1 = Normal
57	VREF	I	RGMII input voltage reference. Must be set to VDDOR/2 when used as 1.8V HSTL, 2.5V SSTL_2, and 3.3V. Set to VDDOR when used as 2.5V LV CMOS.

Table 7: Test

64-QFN Pin #	Pin Name	Pin Type	Description
35 36	HSDACN HSDACP	O O	AC Test Point. Positive and Negative. These pins are also used to bring out a differential TX_TCLK. Connect these pins with a 50 ohm termination resistor to VSS for IEEE testing and debug purposes. If debug and IEEE testing are not of importance, these pins can be left floating.
32	TSTPT	O	Test Point.

Table 8: Control and Reference

64-QFN Pin #	Pin Name	Pin Type	Description
33	RSET	I	Constant voltage reference. External 4.99 kohm 1% resistor connection to VSS required for each pin.
17	CTRL18	O	1.8V Regulator Control. This signal ties to the base of the BJT. If the 1.8V regulator is not used it can be left floating.
12	DIS_REG12	I	1.2V Regulator Disable. Tie to VDDO to disable, tie to VSS to enable.

Table 9: Power & Ground

64-QFN Pin #	Pin Name	Pin Type	Description
21 22 27 29	AVDD	Power	Analog supply. 1.8V[1]. AVDD can be supplied externally with 1.8V, or via the 1.8V regulator.
34 37	AVDDC		Analog supply - 1.8V or 2.5V, or 3.3V[2]. AVDDC must be supplied externally. Do not use the 1.8V regulator to power AVDDC.
14 15	AVDDR		1.2V Regulator supply - 1.8V AVDDR can be supplied externally with 1.8V, or via the 1.8V regulator. If the 1.2V regulator is not used, AVDDR must still be tied to 1.8V.
16	AVDDX	Power	1.8V Regulator supply - 2.5V, 3.3V, (or 1.8V). AVDDX must be supplied externally. Note that this supply must be the same voltage as AVDDC. If the 1.8V regulator is not used, then it means a 1.8V supply is in the system. AVDDX (along with AVDDC) would be tied to 1.8V in this case.
5 13 40 47	DVDD	Power	Digital core supply - 1.2V. DVDD can be supplied externally with 1.2, or via the 1.2V regulator.
7 46	VDDO	Power	1.8V, 2.5V, or 3.3V non-RGMII digital I/O supply[3]. VDDO must be supplied externally. Do not use the 1.8V regulator to power VDDO.
52 56	VDDOR	Power	1.8V, 2.5V, or 3.3V RGMII digital I/O supply[4]. VDDOR must be supplied externally. Do not use the 1.8V regulator to power VDDOR.
EPAD	VSS	GND	Ground to device. The 64-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD.
18 28[5]	NC	NC	No connect. These pins are not connected to the die so they can be connected to anything on the board.

1. AVDD supplies the MDIP/N[3:0] pins.
2. AVDDC supplies the XTAL_IN and XTAL_OUT pins.
3. VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG[3:0], TDI, TMS, TCK, TRSTn, TDO, DIS_REG12, CTRL18, HSDAC, and TSTPT
4. VDDOR supplies the TXD[3:0], TX_CLK, TX_CTRL, RXD[3:0], RX_CLK, and RX_CTRL pins.
5. Pin 28 must be connected to AVDD in Revision A0. Refer to the Rev A0 Release Notes for Pin 28 connection details.

1.2 64-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
21	AVDD	24	MDIP[2]
22	AVDD	20	MDIP[3]
27	AVDD	18	NC
29	AVDD	28	NC
34	AVDDC	53	RX_CLK
37	AVDDC	49	RX_CTRL
14	AVDDR	10	RESETn
15	AVDDR	33	RSET
16	AVDDX	50	RXD[0]
4	CLK125	51	RXD[1]
64	CONFIG[0]	54	RXD[2]
1	CONFIG[1]	55	RXD[3]
2	CONFIG[2]	42	TCK
3	CONFIG[3]	43	TDI
17	CTRL18	44	TDO
12	DIS_REG12	41	TMS
5	DVDD	11	TRSTn
13	DVDD	60	TX_CLK
40	DVDD	63	TX_CTRL
47	DVDD	58	TXD[0]
35	HSDACN	59	TXD[1]
36	HSDACP	61	TXD[2]
6	LED[0]	62	TXD[3]
8	LED[1]	32	TSTPT
9	LED[2]	7	VDDO
48	MDC	46	VDDO
30	MDIN[0]	52	VDDOR
25	MDIN[1]	56	VDDOR
23	MDIN[2]	57	VREF
19	MDIN[3]	EPAD	VSS
45	MDIO	38	XTAL_IN
31	MDIP[0]	39	XTAL_OUT
26	MDIP[1]		

Section 2. Package Mechanical Dimensions

2.1 64-Pin QFN Package

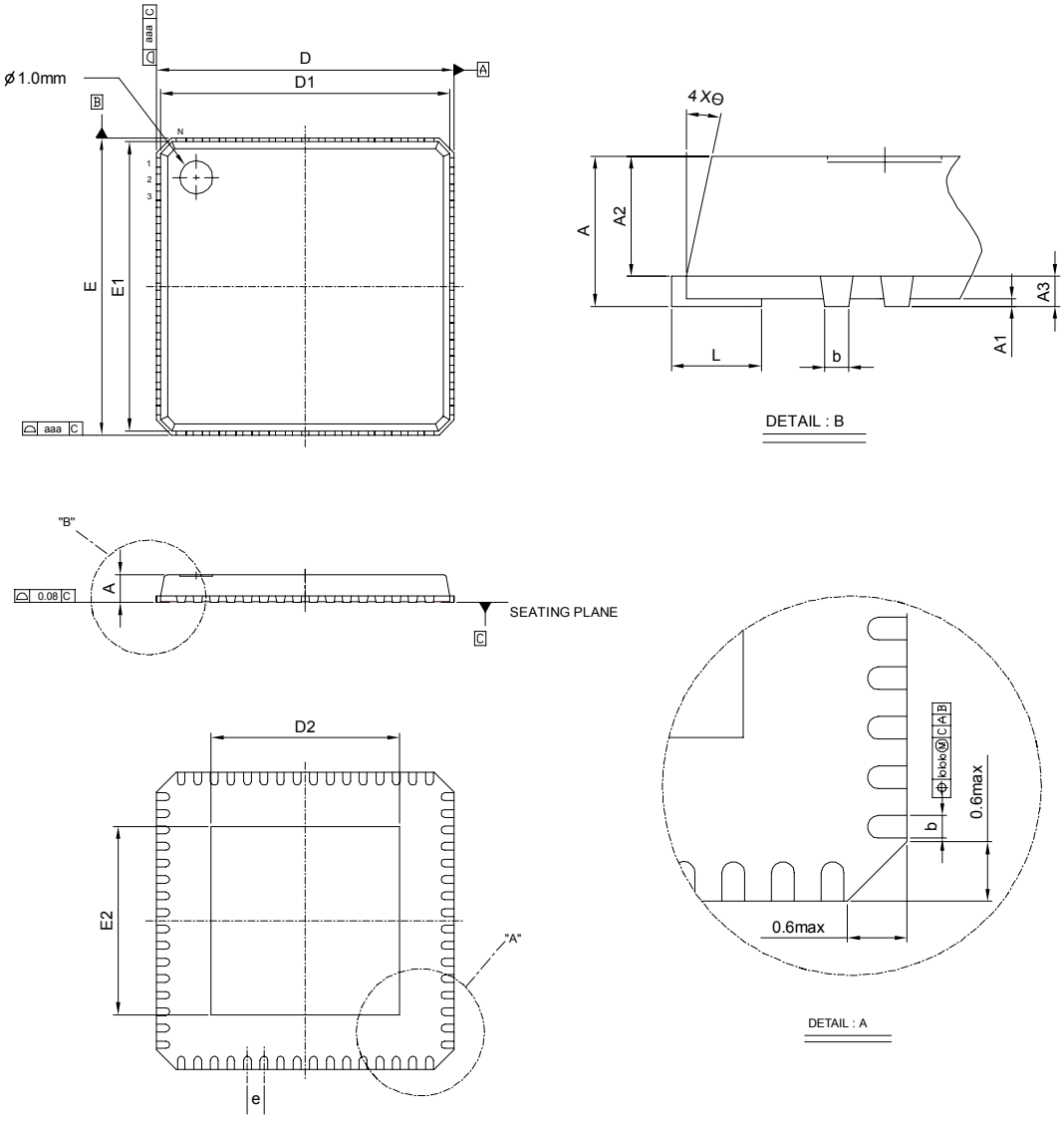


Table 10: 64-Pin QFN Mechanical Dimensions

	Dimensions in mm		
Symbol	**MIN**	**NOM**	**MAX**
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A2	--	0.65	1.00
A3		0.20 REF	
b	0.18	0.23	0.30
D		9.00 BSC	
D1		8.75 BSC	
E		9.00 BSC	
E1		8.75 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
θ	0°	--	12°
aaa	--	--	0.25
bbb	--	--	0.10
chamfer	--	--	0.60

Die Pad Size	
Symbol	**Dimension in mm**
D_2	5.21 ± 0.20
E_2	6.25 ± 0.20

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