PLL520-40

CMOS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

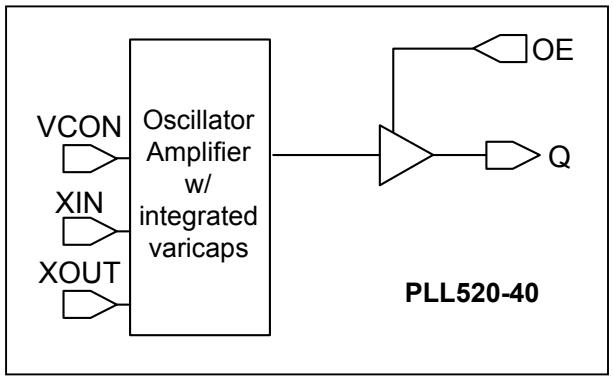
FEATURES

- 65MHz to 130MHz Fundamental Mode Crystal.
- Output range: 65MHz – 130MHz (no PLL).
- Low Injection Power for crystal 50uW.
- CMOS outputs (High Drive (30mA) or Standard Drive (10mA) output).
- Integrated variable capacitors.
- Supports 2.5V or 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

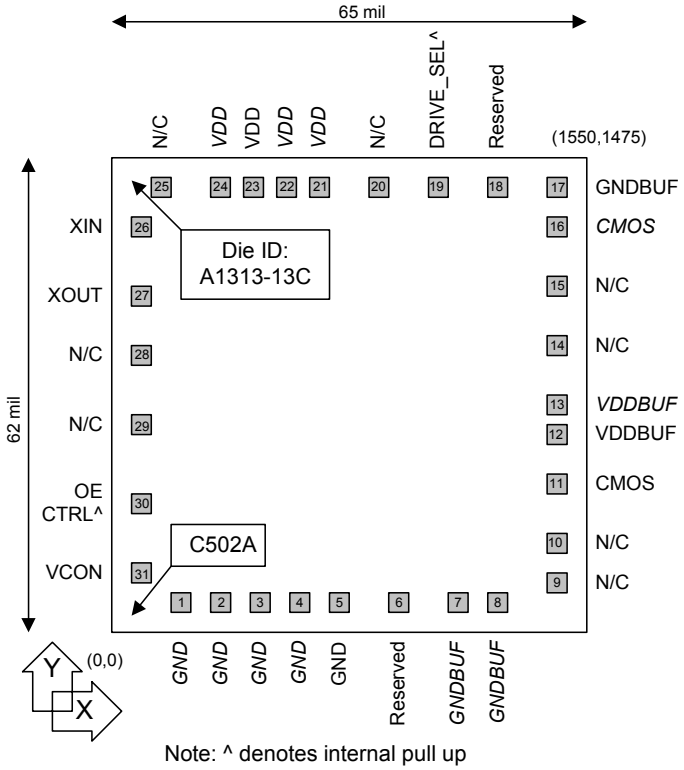
DESCRIPTION

The PLL520-40 is a VCXO IC specifically designed to pull frequency fundamental crystals from 65MHz to 130MHz, with CMOS outputs. Its design was optimized to tolerate higher limits of interelectrode capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. Its internal varicaps allow an on chip frequency pulling, controlled by the VCON input.

BLOCK DIAGRAM



DIE CONFIGURATION



Note: ^ denotes internal pull up

DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

DRIVE_SEL AND OE_CTRL TABLE

DRIVE_SEL (Pad #19)	Output Drive
0	High Drive CMOS
1	Standard CMOS (default)

OE_CTRL (Pad #30)	State
0	Tri-state
1	Output enabled (default)

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ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Built-in Capacitance	CX+	65MHz to 130MHz (VDD=3.3V)			2	pF
	CX-				2	
Inter-electrode capacitance	C_0			2.6		
C0/C1 ratio (gamma)	γ				300	-
Oscillation Frequency	OF	Fund.	65		130	MHz

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 100 – 200MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		200*		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±100*			ppm
On-chip Varicaps control range		VCON = 0 to 3.3V		4 – 18*		pF
Linearity					10*	%
VCXO Tuning Characteristic				65		ppm/V
VCON input impedance				60		kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

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4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}				40	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 50% V_{DD} (CMOS)	45	50	55	%
Short Circuit Current				±50		mA

5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	77.76MHz		2.5		ps
Period jitter peak-to-peak	77.76MHz		18.5		ps
Integrated jitter RMS	Integrated 12 kHz to 20 MHz at 77.76MHz		0.5		ps

6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	77.76MHz	-75	-95	-125	-145	-155	dBc/Hz

Note: Phase Noise at VCON = 0V

7. CMOS Output Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		

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PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)	Description
1	*Optional GND*	248	109	Optional Ground.
2	*Optional GND*	361	109	Optional Ground.
3	*Optional GND*	473	109	Optional Ground.
4	*Optional GND*	587	109	Optional Ground.
5	GND	702	109	Ground.
6	*Reserved*	874	109	Reserved for future use.
7	*Optional GNDBUF*	1042	109	Optional Ground, buffer circuitry.
8	*Optional GNDBUF*	1171	109	Optional Ground, buffer circuitry.
9	*Not connected*	1400	125	Not Connected.
10	*Not connected*	1400	259	Not Connected..
11	CMOS OUT	1400	476	CMOS output.
12	VDDBUF	1400	616	Power supply, buffer circuitry.
13	*Optional VDDBUF*	1400	716	Optional power supply, buffer circuitry.
14	*Not connected*	1400	871	Not Connected.
15	*Not connected*	1400	1089	Not Connected.
16	*Optional CMOS OUT*	1400	1227	Optional CMOS output.
17	GNDBUF	1389	1365	Ground, buffer circuitry.
18	*Reserved*	1232	1365	Reserved for future use.
19	DRIVE_SEL	1042	1365	Used to select drive strength. See DRIVE_SEL AND OE_CTRL TABLE on page 1.
20	*Not connected*	854	1365	Not Connected.
21	*Optional VDD*	659	1365	Optional power supply.
22	*Optional VDD*	559	1365	Optional power supply.
23	VDD	459	1365	Power supply.
24	*Optional VDD*	358	1365	Optional power supply.
25	*Not connected*	194	1365	Not Connected.
26	XIN	109	1223	Crystal input. See Crystal Specifications on page 2.
27	XOUT	109	1017	Crystal output. See Crystal Specifications on page 2.
28	*Not connected*	109	858	Not Connected.
29	*Not connected*	109	646	Not Connected.
30	OE_CTRL	109	397	Used to enable/disable the output(s). See DRIVE_SEL AND OE_CTRL TABLE on page 1. Internal pull up.
31	VCON	109	181	Voltage control input.

Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

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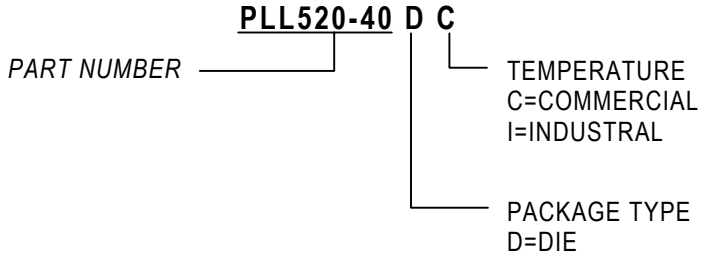
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PLL520-40DC	P520-40DC	Die – Waffle Pack