CT1775N
Universal MacAir/1553 Dumb RTU Hybrid

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FEATURES

- CT1775N replaces DDC BUS-65201
- Includes:
  - Universal transceiver
  - Encoder/Decoder
  - Dual rank I/O registers
  - Fail-safe timer
  - Clock oscillator
- Simple controls for single or dual redundant data bus configurations
- Provides Flags for:
  - Own Address (with parity)
  - Mode code
  - Broadcast
  - Time out
  - Valid word
  - Sync type
- 16 Bit or 8 Bit 3-state
  - Parallel I/O and serial out
- Wraparound built-in test
- MIL-PRF-38534 compliant circuits available
- Designed for commercial, industrial and aerospace applications
- Packaging – Hermetic metal
  - 68 Pin, 1.85" x 1.6" x .19" Plug-In type package

DESCRIPTION

The CT1775N Universal MACAIR/1553 Dumb Remote Terminal Unit (RTU) consists of a transceiver, and encoder/decoder, control logic, dual rank I/O registers and internal clock oscillator packaged in a 1.6" x 1.9" hermetic hybrid. It provides all the functions required to interface between a MACAIR (sinusodial) or MIL-STD-1553 (Trapezoidal) serial MUX data bus and a subsystem parallel 3-state data highway. Utilizing several ASIC ICs, the CT1775N provides sufficient handshaking, control and data lines to permit versatile operation as a remote terminal, a bus controller or a bus monitor, in either single or dual redundant data bus configurations.

As a transmitter, the CT1775N accepts 8 bit or 16 bit parallel date from the subsystem, and outputs serial Manchester II coded Command, Status or Data words, under subsystem control. As a receiver, it accepts serial MIL-STD-1553 or MACAIR transmissions and transfers all Command, Status and Data words to the 8 bit or 16 bit data highway, under subsystem control. The CT1775N also provides flags to the subsystem when Broadcast, Mode Code, and Own Address (with parity) commands are decoded.

The CT1775N contains a terminal fail-safe timeout circuit which flags message lengths exceeding 768µs, and terminates serial data transmission. Wraparound selftest is initiated by a control line which causes the encoder serial output to be connected to the decoder input. The CT1775N provides a serial output of decoded words, thus allowing Command Word look ahead, for the fastest terminal response.

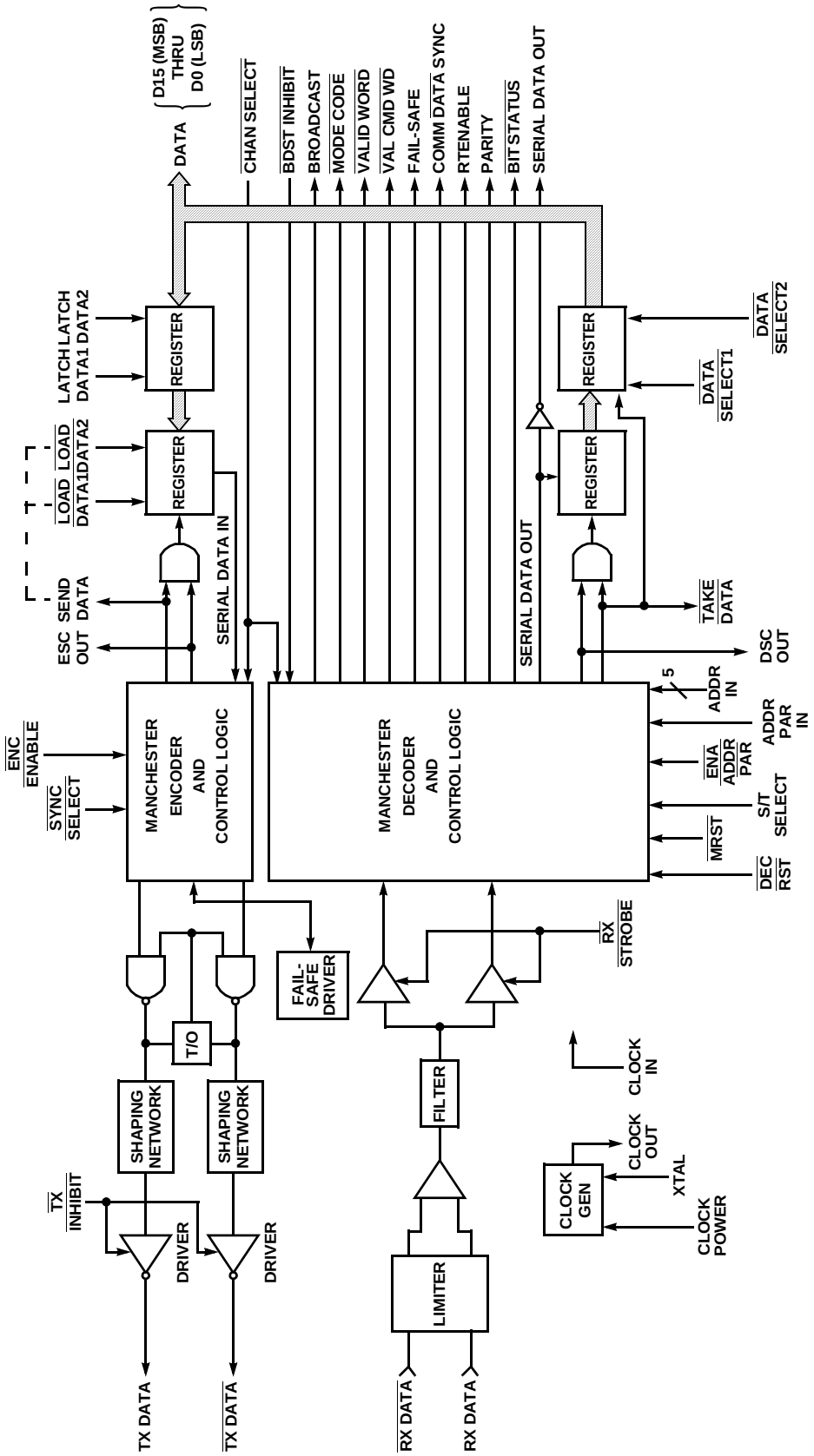


FIGURE 1 – CT1775N BLOCK DIAGRAM

VALUES AT NOMINAL POWER SUPPLY VOLTAGES UNLESS OTHERWISE SPECIFIED

PARAMETER	VALUE	UNITS
Receiver		
Differential Input Impedance (DC to 1MHz)	4 min	KΩ
Differential Input Voltage	40 max	V_{P-P}
Input Threshold (Direct Coupled)	1 typ	V_{P-P}
CMRR (DC to 2MHZ)	40 min	dB
CMV (DC to 2MHZ)	±10 min	V
RX STROBE Characteristics	1 typ	TTL Loads
Transmitter		
Differential Output Voltage		
Direct Coupled (across 145Ω Load)	30 typ	V_{P-P}
Transformer Coupled (at stub)	21 typ	V_{P-P}
Output Rise and Fall time	130 typ	ns
Output Noise	10 max	mV_{P-P}
TX INHIBIT Characteristics	1 typ	TTL Loads
Logic		
I_{IH}, I_{IL}, I_{OH}, I_{OL}	See pin function & loading Table	
V_{OH}	2.5 min	V
V_{OL}	0.4 max	V
V_{IH}	2.0 min	V
V_{IL}	0.7 max	V
Clock		
V_{OHC} (Internal Clock)	Supply -0.3 min	V
V_{OLC} (Internal Clock)	Ground +0.3 min	V
V_{IHC} (External Clock)	Supply -0.5 min	V
V_{ILC} (External Clock)	Ground +0.5 min	V
Power Supplies		
+5V OSC/CLOCK Supply		
Voltage Tolerances	±10	%
Current Drain	8 typ; 13 max	mA
+5V Logic Supply		
Voltage Tolerances	±10	%
Current Drain	250 max	mA
+15V (or +12V) Supply		
Voltage Tolerances	±5	%
Current Drain	65 max	mA
-15V Supply		
Voltage Tolerances	±5	%
Current Drain		
Idle	65 max	mA
25% Transmit	105 max	mA
100% Transmit	250 max	mA
-12V Supply		
Voltage Tolerances	±5	%
Current Drain		
Idle	65 max	mA
25% Transmit	105 max	mA
100% Transmit	250 max	mA
Temperature Range		
Operating (Case)	–55 to +125	°C
Storage	–65 to +150	°C
Physical Characteristics		
Size		
68 pin DDIP	1.6 x 1.9 x 0.18	in

TABLE 1 – CT1775N SPECIFICATIONS

GENERAL

As shown in the block diagram of Figure 1, the CT1775N provides all functions required to implement a Dumb Remote Terminal Unit (RTU). It is designed for the greatest flexibility and ease of use. CT1775N can be operated with either an internal or external clock. Simple control lines are provided to interface with either single channel or dual redundant configurations.

Control lines are available to implement either on line or off line wraparound built-in test. CT1775N can be configured to perform a parity check on its hard-wired terminal address. It provides numerous output flags to simplify the use interface. These flags indicate various decoded messages, as well as the results of error checks. Sync selection, along with the flexible controls, allows the CT1775N to operate as a Bus Controller as well as a Remote Terminal.

INTERNAL OR EXTERNAL CLOCK

CT1775N may be operated with either its internal clock or an external clock. Internal clock operation requires that a 12 MHz parallel-resonant fundamental-mode crystal, such as MIL-C-3098/42 TYPE CR64/U, be connected between pin 18 (XTAL) and ground. In addition, +5 volt power must be connected to pin 2 (OSC/CLOCK POWER), and CLOCK OUT (pin 19) must be connected to CLOCK in (pin 24).

For external clock operation, no connection is made to pin 2 (OSC/CLOCK POWER, and the external clock is applied to pin 24 (CLOCK IN). Pin 19 (CLOCK OUT) is not connected. The external clock must be capable of driving a load of 20 picofarads to within 0.5 volts of the + 5 volt power supply and to within 0.5 volts of ground. Standard TTL voltage levels will not work properly. It must have a rise time and fall time of less than 10 nanoseconds. For compliance with MILSTD-1553, the external clock frequency must be 12 MHz.

8 BIT OR 16 BIT INTERFACE

The CT1775N may be configured to interface with either 8 bit or 16 bit parallel data highways. For 16 bit operation, the 16 data lines (D 15 through DO) are used directly. LATCH DATA 1 and LATCH DATA 2 are tied together, as are $\overline{\text{DATA SELECT 1}}$ and $\overline{\text{DATA SELECT 2}}$. This allows data transfer in 16 bit bytes.

For 8 bit parallel data highways, the 16 data lines must be tied together in eight pairs (1315 to D7, D8 to 130, etc.) The two LATCH DATA and $\overline{\text{DATA SELECT}}$ are used independently. This allows transfer in two 8 bit bytes.

ADDRESS WITH PARITY

The CT1775N provides five lines for hard-wired terminal address. Internal pull-up resistors are provided on these lines, so logic "1" lines may be left open-circuited. Logic "0" lines must be grounded. The CT1775N maybe configured to check the parity of these five address lines. This function can be selected by using the ENA PAR CHECK line. The address parity line (TMADDP) is hard-wired for odd address parity if the function is sued. the ODD PARITY output flag indicates a valid check for odd parity of the six address lines.

DUAL REDUNDANT OPERATION

The CT1775N may be used in a dual redundant configuration with a minimum of additional circuitry. A $\overline{\text{CHAN SELECT}}$ signal is provided which simultaneously disables the LATCH DATA, $\overline{\text{DATA SELECT}}$, and $\overline{\text{ENC ENABLE}}$ lines of the CT1775N. Therefore, $\overline{\text{CHAN SELECT}}$ can be used to multiplex a single set of LATCH DATA, $\overline{\text{DATA SELECT}}$ and $\overline{\text{ENC ENABLE}}$ control signals between two CT1775N units, which have these signals tied together in parallel.

WRAPAROUND BUILT-IN TEST

The CT1775N may be configured to implement either on line or off line wrap around built-in test. By enabling the receiver with $\overline{\text{RX STROBE}}$ during a normal transmission, the encoded word will be fed back into the decoder by the receiver. In this on line wrap around mode of operation, the CT1775N compares each decoded word that is fed back with the original word that was encoded. The $\overline{\text{BIT STATUS}}$ output flag indicates when the two words are not the same.

Care must be taken when using this on line wrap around test technique because an outgoing status word will be interpreted by the decoder as a new command word. Since the status word has the correct address and the same sync as a command word, the CT1775N will set RT ENABLE and $\overline{\text{VAL CMD WD}}$. For on line wrap around operation, it is therefore necessary to reset RT ENABLE after transmission of a status word. This can be accomplished by inverting SEND DATA and applying it to $\overline{\text{DEC RST}}$ during status word transmission. If it is required that the status word be fed back, RT ENABLE should be reset immediately after it goes HIGH by applying a LOW to $\overline{\text{DEC RST}}$ for 1 microsecond (minimum). The status word will be available at the receive register.

The CT1775N can be placed in an off line wrap around test mode by use of the S/T SELECT signal. In this mode, the transceiver is disabled and the encoder output is fed directly to the decoder input. All other functions remain the same, and the CT1775N compares each word that is decoded with the original word that was encoded. The $\overline{\text{BIT STATUS}}$ line also indicates the result of this comparison for the off line wrap around test.

FAIL SAFE TIME-OUT

The CT1775N contains a timer which continuously monitors the length of each transmitted message. This timer detects a transmitted message which exceeds 768 microseconds and causes the transmission to terminate. At the same time, The FAIL-SAFE flag is set to indicate a Terminal Fail-Safe Time-out. Further transmissions are inhibited until the FAIL-SAFE flag is reset by $\overline{\text{MRST}}$ or a valid command word with the correct address is received.

OUTPUT FLAGS

The CT1775NCT1775N provides numerous output flags to offer the greatest user flexibility. VALID WORD indicates receipt of a word with valid sync, Manchester coding and parity. RT ENABLE indicates a valid word and correct address. VAL CMD WD indicates a valid word and a Command Sync. BROADCAST indicates a valid command word and an address of 11111. The BROADCAST flag may be inhibited by using the BDCST INHIBIT line. MODE CODE indicates a valid command word and a subaddress of 11111 or 00000.

INITIALIZATION

To ensure error-free operation, it is desirable to reset the CT1775N to its initialized state upon power turn-on. The MRST (master reset) signal is provided for this purpose. Both the flecoder and encoder, as well as all flags, are reset by a LOW on MRST. This function interrupts and overrides all other control signals. The MRST function can also be sued during fault recovery routines.

TRANSCEIVER OPERATION

The CT1775N contains a transceiver similar to Aeroflex model CT3232. When connected to a serial MUX data bus via transformer and isolation resistors, as shown in Figure 6, the CT1775N transceiver will fully comply with MIL-STD-1553. The correct Technitrol part numbers for transformers used in direct-coupled and transformercoupled operation are shown in Figure 6.

Transceiver TX INHIBIT and RX STROBE signals are provided to afford flexible operation. These signals may be used to disable the transmitter and receiver, respectively.

ENCODER OPERATION

Figure 2 illustrates the transmit mode timing. Encoder detail timing is shown in Figure 4. The transmit cycle is initiated by a LOW on ENC ENABLE. The first HIGH to LOW (falling edge) transition of ESC OUT, when ENC ENABLE is LOW, starts the cycle which lasts for 20 clock periods of the 1 MHz ESC OUT. The next LOW to HIGH transition of ESC OUT strobes the SYNC SELECT line. A HIGH on SYNC SELECT produces a data sync and a LOW produces a command/status sync.

A LOW to HIGH transition of SEND DATA occurs at the fourth falling edge of ESC OUT. This indicates the completion of the sync interval and the start of the serial data interval. Parallel data must be stable at the second rank transmit register prior to the rising edge of SEND DATA, which occurs 3 microseconds (minimum) after the HIGH to LOW transition of ENC ENABLE. LATCH DATA is used to transfer parallel data to the first rank transmit register. LATCH DATA must be brought LOW and DATA SELECT brought HIGH prior to the rising edge of SEND DATA. If SEND DATA is connected directly to LOAD DATA, it will lock out the second rank transmit register and serial data shifting into the encoder will proceed properly.

For multiple word transmissions, the next word may be transferred to the transmit register any time after SEND DATA goes HIGH, but no later than the next LOW to HIGH transition of SEND DATA. SEND DATA remains HIGH for 16 periods of ESC OUT, during which time the data word is serially shifted to the Manchester encoder. The encoder adds the parity bit during the next ESC OUT period after SEND DATA goes LOW. To terminate transmission after any word, ENC ENABLE must go to HIGH no later than the first rising edge of ESC OUT after SEND DATA goes LOW.

The entire transmit cycle may be interrupted and initialized by applying a 1 microsecond (minimum) negative pulse to MRST. It is possible to input data to the encoder in serial form by forcing both transmit registers to be transparent. With LATCH DATA 1 held HIGH and LOAD DATA 1 held LOW, serial data input on D15 will be applied directly to the encoder serial input. ESC OUT must be used to shift in the serial data, MSB first, starting at the LOW to HIGH transition of SEND DATA.

DECODER OPERATION

Figure 3 illustrates the receive mode timing. Decoder detail timing is shown in Figure 5. A receive cycle, which lasts for 20 clock periods of the 1 MHz DSC OUT, is initiated when the decoder recognizes a valid sync and two valid Manchester data bits. TAKE DATA goes LOW at the first HIGH to LOW (falling edge) transition of DSC OUT, following the second valid dat bit. COMM/DATA SYNC is updated at the next rising edge of DSC OUT after TAKE DATA goes LOW. COM/DATA SYNC remains in its new state until the next valid word or until DEC RST or MRST goes LOW.

TAKE DATA remains LOW for 16 periods of DSC OUT, during which time the 16 serial data bits are shifted into the first rank receive register. The serial data is simultaneously available at SERIAL DATA OUT as it is being shifted. At the completion of decoded data shifting, TAKE DATA goes HIGH, which transfers the data to the second rank receive register. This data may be enabled onto the parallel data highway by LOW on DATA SELECT at any time until the next rising edge of TAKE DATA.

At the first rising edge of DSC OUT after TAKE DATA goes HIGH, VALID WORD is updated. It will go LOW if the decoded word was valid. VALID WORD will go HIGH at the start of the next receive cycle, or after 20 microseconds if no additional words ar received. All output flags are enabled by VALID WORD, and therefore they are valid only as long as VALID WORD is LOW.

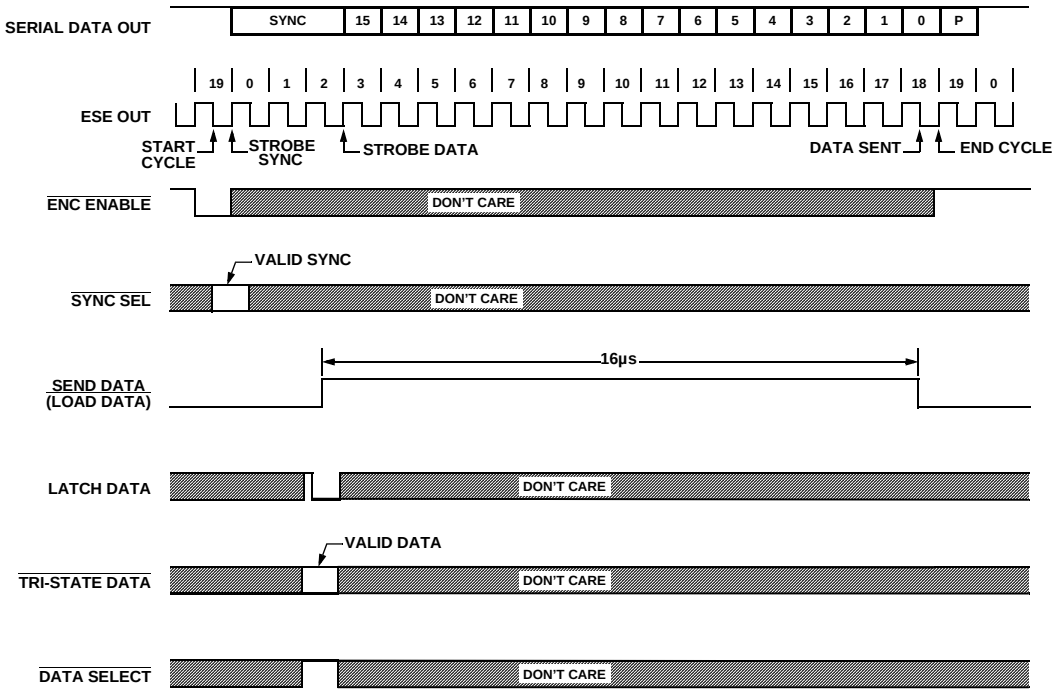
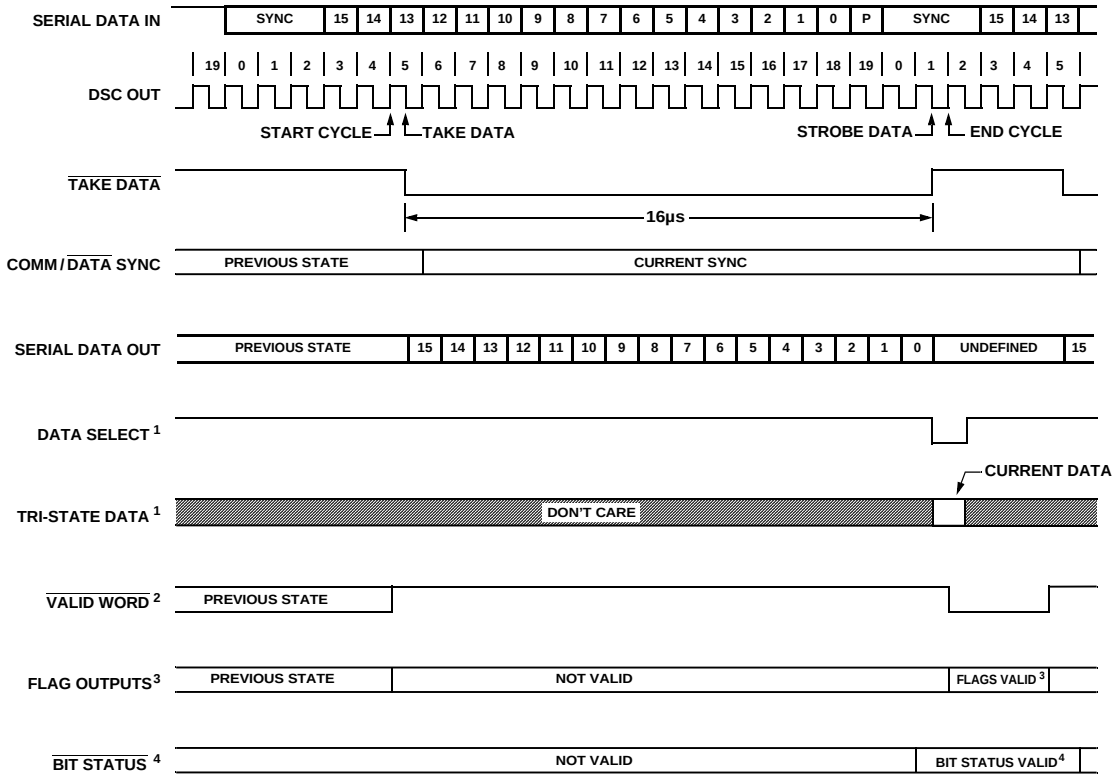


FIGURE 2 – TRANSMIT MODE TIMING



NOTES:

1. Parallel data is held continuously in second rank receiver register, and may be enabled onto the tri-state output at any time with a LOW on $\overline{\text{DATA SELECT}}$.
2. $\overline{\text{VALID WORD}}$ will remainLOW for 20µsec then go HIGH, if a valid sync is not received.
3. FLAG OUTPUTS are valid only when $\overline{\text{VALID WORD}}$ is LOW. Flags are $\overline{\text{MODE CODE}}$, RT Enable, BROADCAST and $\overline{\text{VAL CMD WD}}$.
4. $\overline{\text{BIT STATUS}}$ is valid only if wraparound transmit plus receive cycle has been performed. LATCH DATA must be HIGH, and either S/T SELECT or $\overline{\text{RX STROBE}}$ must be HIGH for the full wraparound cycle duration.

FIGURE 3 – RECEIVE MODE TIMING

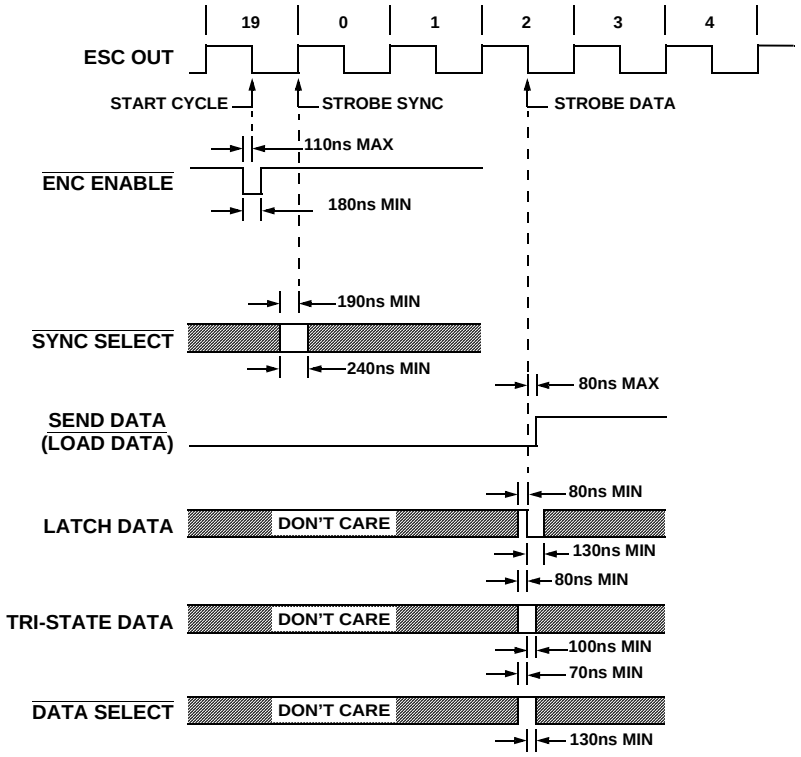


FIGURE 4 – ENCODER DETAIL TIMING

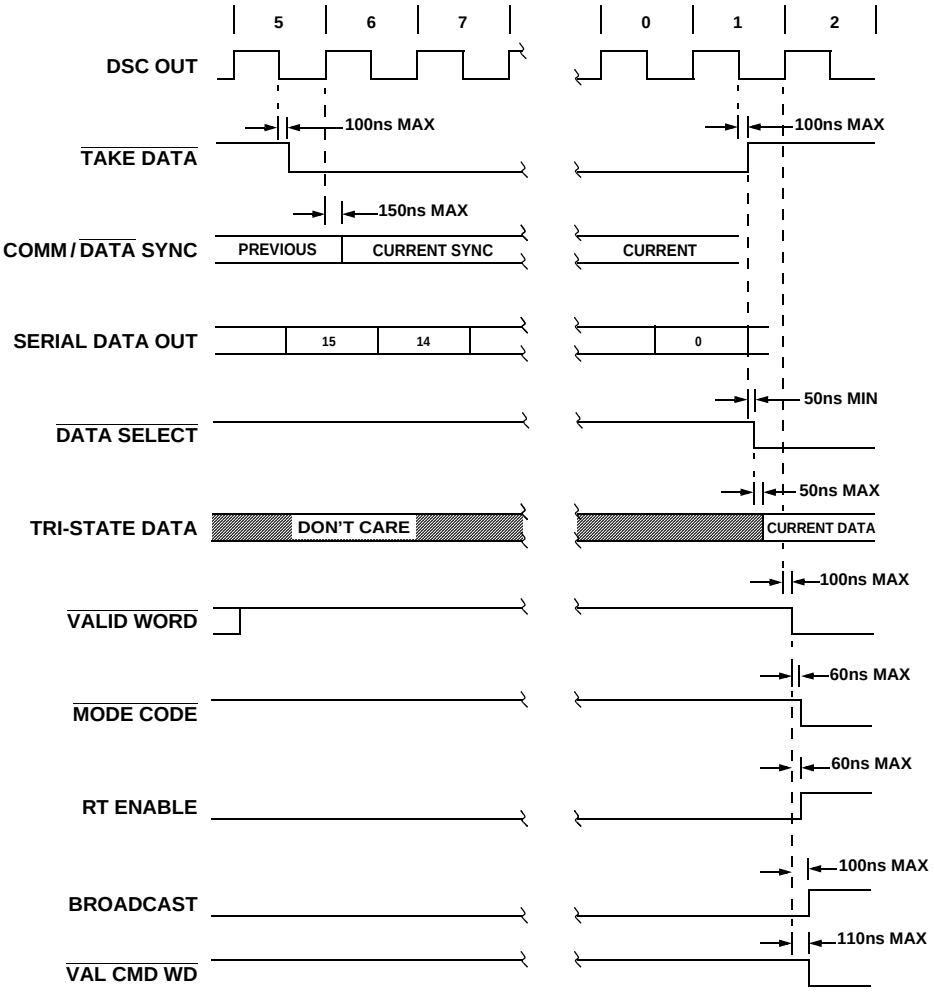


FIGURE 5 – DECODER DETAIL TIMING

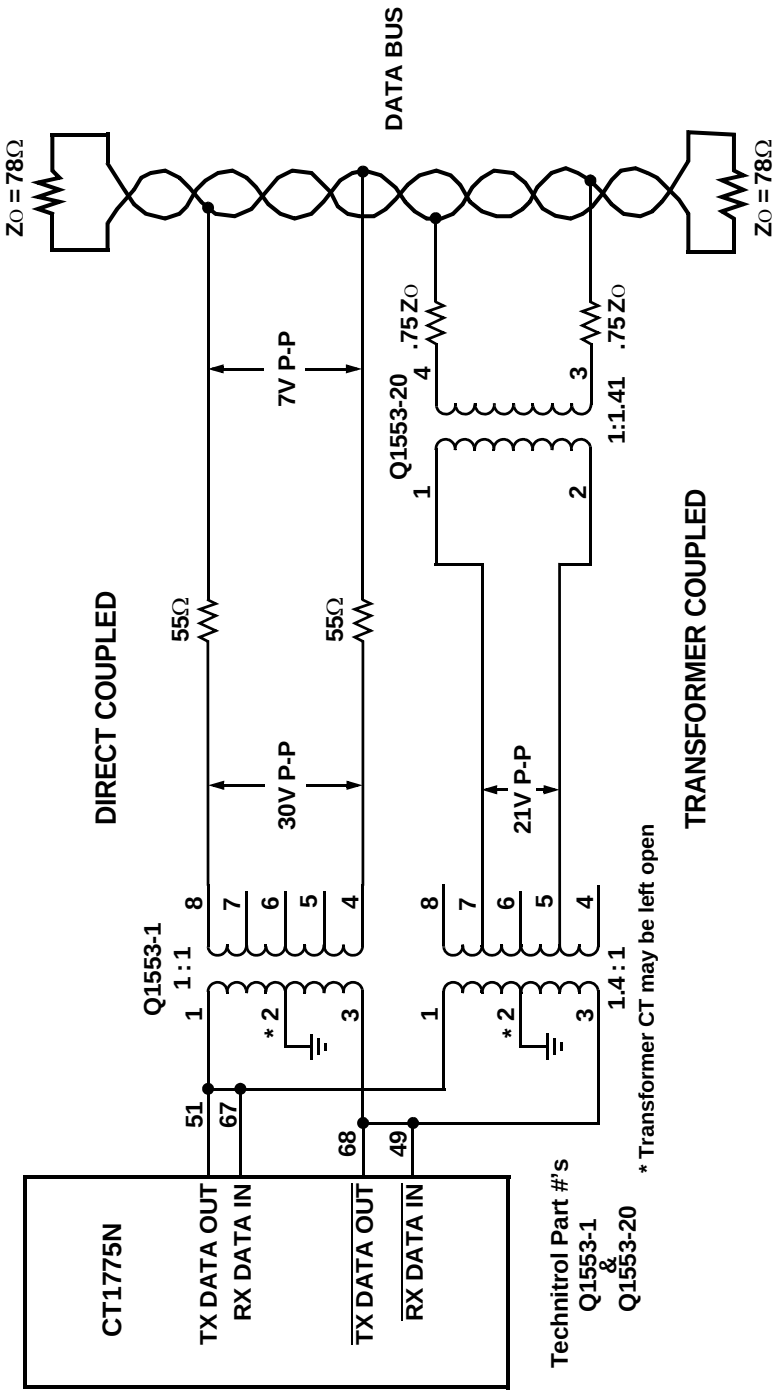


FIGURE 6 – TYPICAL TRANSFORMER CONNECTIONS

PIN FUNCTION AND LOADING TABLE

PIN #	NAME	I_{IH} (µA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	GND					Power supply and logic return.
2	+5V OSC/ CLOCK POWER					+5V Power for oscillator and clock driver.
3	NC					No connection.
4	$\overline{\text{TX INHIBIT}}$	20	-0.4			A LOW on this input inhibits the transmitter.
5	$\overline{\text{SYNC SELECT}}$	20	-0.4			A LOW on this input results in a transmitted DATA sync. A HIGH on this input results in a transmitted COMMAND (or STATUS) sync.
6	SERIAL DATA OUT			-0.4	4.0	Received serial data in NRZ format is available at this output when $\overline{\text{TAKE DATA}}$ is LOW.
7	ESC OUT			-0.4	4.0	LOW to HIGH transitions on this output when SEND DATA is HIGH causes the transmit cycle data shifting to occur.
8	NC					No connection.
9	COMM / $\overline{\text{DATA}}$ SYNC			-.36	3.6	A LOW on this output indicates receipt of a DATA word. A HIGH indicates receipt of a COMMAND (or STATUS) word.
10	$\overline{\text{MRST}}$	40	-0.8			A LOW on this input (1 µsec minimum) resets the decoderto its initialized condition (same function as $\overline{\text{DEC RST}}$), resets FAIL-SAFE, and stops and clears the transmit cycle. This function interrupts and overridesall othercontrols.
11	$\overline{\text{VALID WORD}}$			-0.4	4.0	A LOW on this output indicates receipt of a valid word.
12	$\overline{\text{BIT STATUS}}$			-0.4	4.0	A LOW on this output, during wrap around self test only, indicates that the last word decoded was identical to the last word encoded.
13	LATCH DATA 1	20	-0.4			A HIGH on this input causes parallel tri-state I/O data on D8 through D15 to appear at the output of the first rank transmit register. A LOW locks out the register inputs.
14	$\overline{\text{VAL CMD WD}}$			-0.4	4.0	A LOW on this output indicates the receipt of a valid command word.
15	$\overline{\text{BDCST INH}}$	20	-0.4			A LOW on this input inhibits the indication of the BROADCAST output flag.
16	TMADD1*	20	-0.4			Part of 5 bit hard-wired terminal address input.
17	TMADD3*	20	-0.4			Part of 5 bit herd-wired terminal address input.
18	XTAL					A 12 MHz parallel resonant crystal is connected between this input and ground.
19	CLOCK OUT			-1.0	1.0	Output of oscillator and clock driver (see text).
20	$\overline{\text{TAKE DATA}}$			-0.4	4.0	A LOW on this output indicates that received data is being shifted into the first rank register and is available at SERIAL DATA OUT. A LOW to HIGH transition transfers the contents of the first rank receiver register to the second rank register.

PIN FUNCTION AND LOADING TABLE (con't)

PIN #	NAME	I_{IH} (µA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
21	$\overline{\text{DEC RST}}$	20	-0.4			A LOW on this input (1 µsec minimum) resets the decoderto its initialized state, resets COMM/$\overline{\text{DATA}}$ SYNC to a LOW, and resets $\overline{\text{VALID WORD}}$ to a HIGH.
22	DSC OUT			-0.4	4.0	$\overline{\text{LOW}}$ to HIGH transitions on this output when $\overline{\text{TAKE DATA}}$ is LOW causes causes receive cycle data shifting to occur.
23	SEND DATA			-0.4	4.0	A HIGH on this output indicates that transmit cycle data shifting is occuring.
24	CLOCK IN	±1	±.001			12 MHz clock input (20pF load) (see text).
25	S/T SELECT	20	-0.4			A HIGH on this input enables offline wraparound selftest.The transceiver is disabled and the encoder output is connected to the decoder input (see text).
26	FAIL-SAFE			-0.4	4.0	A HIGH on this output indicates that a transmitted message has exceeded 768 µsec, and that transmission has been terminated. FAIL-SAFE is reset by either FIT ENABLE or $\overline{\text{MRST}}$.
27	RT ENABLE			-0.4	4.0	A HIGH on this output indicates receipt of a valid COMMAND word containing the correct 5 bit terminal address plus address parity. FAIL-SAFE is reset when FIT ENABLE goes HIGH.
28	$\overline{\text{MODE CODE}}$			-0.4	4.0	A LOW on this output indicates the reception of a valid COMMAND word whose sub-address field contains all ONES or all ZEROES.
29	LATCH DATA 2	20	-0.4			A HIGH on this input causes parallel tri-state I/O data on D0 through D7 to appear at the output of the first rank transmit register. A LOW locks out the register inputs.
30	$\overline{\text{ENCENABLE}}$	20	-0.4			A LOW on this input causes the transmit cycle to start at the next HIGH to LOW transition of ESC OUT
31	BROADCAST			-0.4	4.0	A HIGH on this output indicates reception of a valid COMMAND word whose address field contains all ONES, if $\overline{\text{BDCST INH}}$ is HIGH.
32	TMADD0*	20	-0.4			LSB of 5-bit hard-wired terminal address input.
33	TMADD2*	20	-0.4			Part of 5-bit hard-wired terminal address input.
34	TMADD4*	20	-0.4			MSB of 5-bit hard-wired terminal address input.
35	TMADDP	20	-0.4			Parity bit of hard-wired terminal address. Hard-wired for odd parity.
36	$\overline{\text{CHAN SELECT}}$	100	-2.0			A LOW on this input enables $\overline{\text{DATA SELECT 1}}$, $\overline{\text{DATA SELECT 2}}$, LATCH DATA 1, LATCH DATA 2, and $\overline{\text{ENC ENABLE}}$ inputs.
37	ODD PARITY			-0.36	3.6	A HIGH on this output indicates a valid check for odd parity of terminal address plus parity bits, if $\overline{\text{ENA PAR CHECK}}$ is a LOW.
38	D15	20	-0.2	-12	12	MSB of 16 bit parallel tri-state I/O.

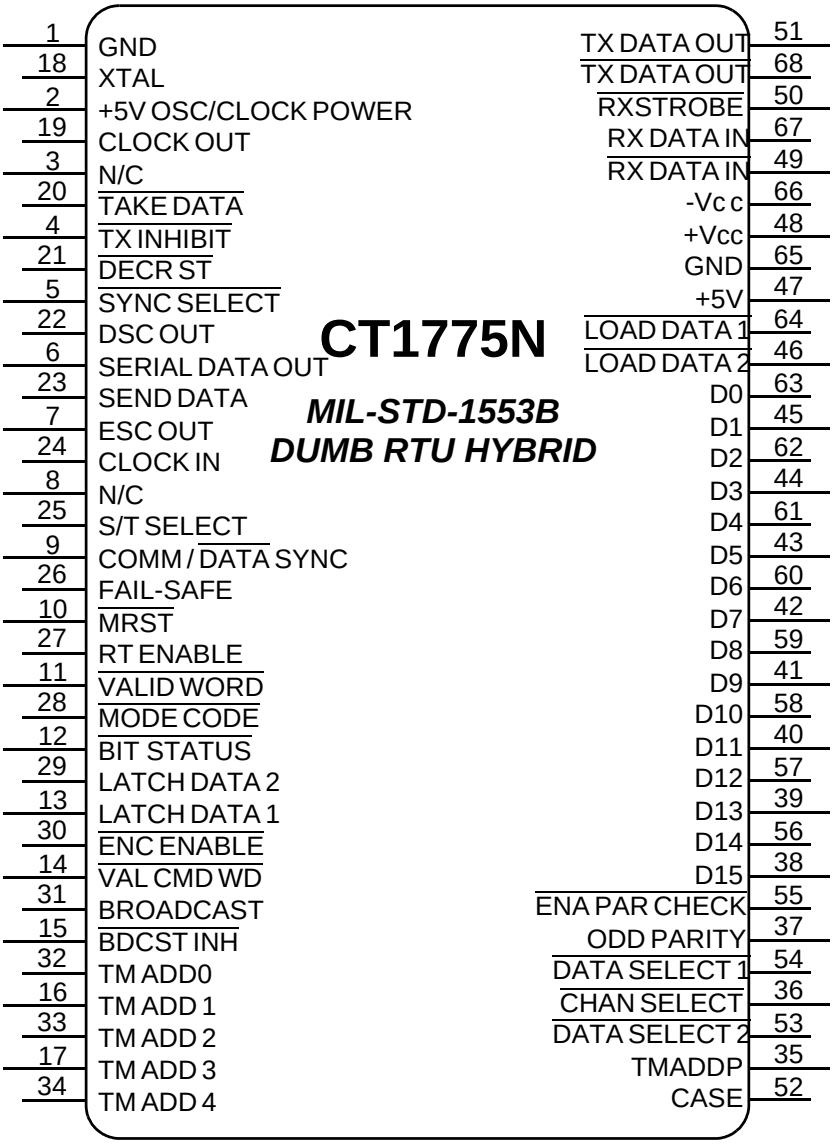
PIN FUNCTION AND LOADING TABLE (con't)

PIN #	NAME	I_{IH} (µA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
39	D13	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
40	D11	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
41	D9	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
42	D7	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
43	D5	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
44	D3	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
45	D1	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
46	$\overline{\text{LOAD DATA 2}}$	20	-0.4			LOW on this input causes the data of the D0 through D7 outputs of the first rank transmit register to be loaded into the second rank transmit register. A HIGH locks out the second rank register inputs.
47	+5V					+5V power supply input.
48	+12V					+12Vpower supply input.
49	$\overline{\text{RX DATA IN}}$					Inverted receiver input.
50	$\overline{\text{RX STROBE}}$	40	-1.6			A LOW on this input disables the receiver output.
51	TX DATA OUT					Transmitter output.
52	CASE					Case connection.
53	$\overline{\text{DATA SELECT 2}}$	20	-0.4			A LOW on this input causes the output of the second rank receiver register to appear on D0 through D7 of the parallel tri-state I/O.
54	$\overline{\text{DATA SELECT 1}}$	20	-0.4			A LOW on this input causes the output of the second rank receiver register to appear on D8 through D15 of the parallel tri-state I/O.
55	$\overline{\text{ENA PAR CHECK}}$	20	-0.4			A LOW on this input enables the function of ODD PARITY.
56	D14	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
57	D12	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
58	D10	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
59	D8	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
60	D6	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
61	D4	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
62	D2	20	-0.2	-12	12	Part of 16 bit parallel tri-state I/O.
63	D0	20	-0.2	-12	12	LSB of 16 bit parallel tri-state I/O.
64	$\overline{\text{LOAD DATA 1}}$	20	-0.4			A LOW on this input causes the data of the D8 through D15 outputs of the first rank transmit register to be loaded into the second rank transmit register. A HIGH locks out the second rank register inputs.
65	GND					Power supply and logic retum

PIN FUNCTION AND LOADING TABLE (con't)

PIN #	NAME	I_{IH} (µA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
66	-12V					-12V power supply input.
67	RX DATA IN					Receiver input.
68	TX DATA OUT					Inverted transmitter output.

NOTES: In the above table, the symbols are defined as follows: *Indicates use of an internal pull-up resistor.
I_{IH} = maximum input HIGH current with V_{IN} = 2.5 volts.
I_{IL} = maximum input LOW current with V_{IN} = 0.4 volts.
I_{OH} = maximum output HIGH current for V_{OUT} = 2.5 volts minimum.
I_{OL} = maximum output LOW current for V_{OUT} = 0.4 volts maximum.



CT1775N PIN OUT DESCRIPTION

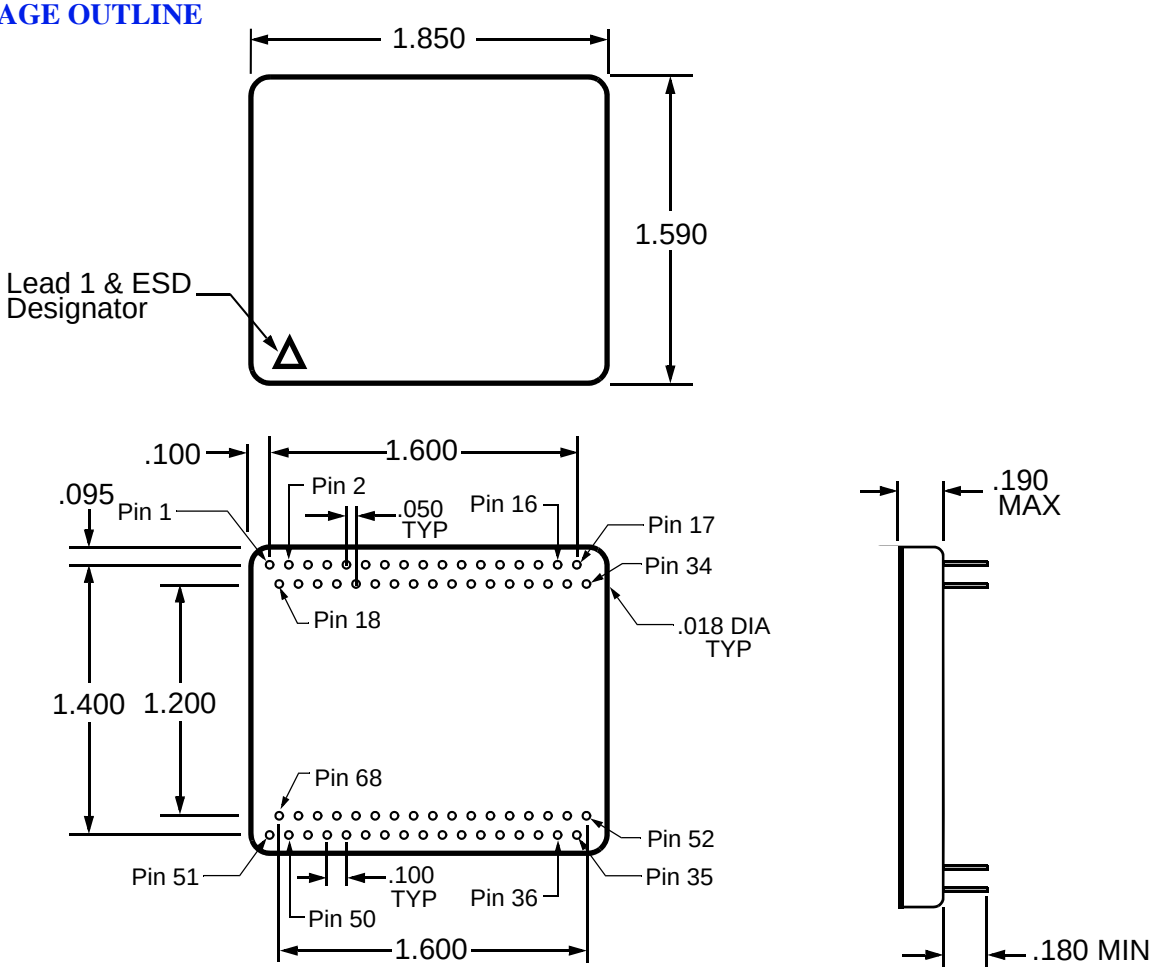
PIN #	FUNCTION	PIN #	FUNCTION
1	GND	35	TMADDP
2	+5V OSC/ CLOCK PWR	36	$\overline{\text{CHAN SELECT}}$
3	N/C	37	ODD PARITY
4	$\overline{\text{TX INHIBIT}}$	38	D15
5	$\overline{\text{SYNC SELECT}}$	39	D13
6	SERIAL DATA OUT	40	D11
7	ESC OUT	41	D9
8	N/C	42	D7
9	COMM / $\overline{\text{DATA}}$ SYNC	43	D5
10	$\overline{\text{MRST}}$	44	D3
11	$\overline{\text{VALID WORD}}$	45	D1
12	$\overline{\text{BIT STATUS}}$	46	$\overline{\text{LOAD DATA 2}}$
13	LATCH DATA 1	47	+5V
14	$\overline{\text{VAL CMD WD}}$	48	+Vcc
15	$\overline{\text{BDCST INH}}$	49	$\overline{\text{RX DATA IN}}$
16	TM ADD 1	50	$\overline{\text{RXSTROBE}}$
17	TM ADD 3	51	TX DATA OUT
18	XTAL	52	CASE
19	CLOCK OUT	53	$\overline{\text{DATA SELECT 2}}$
20	$\overline{\text{TAKE DATA}}$	54	$\overline{\text{DATA SELECT 1}}$
21	$\overline{\text{DECR ST}}$	55	$\overline{\text{ENA PAR CHECK}}$
22	DSC OUT	56	D14
23	SEND DATA	57	D12
24	CLOCK IN	58	D10
25	S/T SELECT	59	D8
26	FAIL-SAFE	60	D6
27	RT ENABLE	61	D4
28	$\overline{\text{MODE CODE}}$	62	D2
29	LATCH DATA 2	63	D0
30	$\overline{\text{ENC ENABLE}}$	64	$\overline{\text{LOAD DATA 1}}$
31	BROADCAST	65	GND
32	TM ADD 0	66	-Vc c
33	TM ADD 2	67	RX DATA IN
34	TM ADD 4	68	$\overline{\text{TX DATA OUT}}$

FIGURE 3 – PIN CONNECTION DIAGRAM, CT1775N AND PINOUT TABLE

ORDERING INFORMATION

MODEL NUMBER	SCREENING	POWER SUPPLY	PACKAGE
CT1775N	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883	+5V, ±12V to ±15V	Plug in

PLUG IN PACKAGE OUTLINE



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