

3.3V, SMD, LV-PECL Oscillator



Model: FCPAXT Series

RoHS Compliant / Pb Free

Rev. 3/9/2007 Preliminary

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http://www.foxonline.com/need_a_sample.htm



FEATURES

- 3.3V Operation
- LV-PECL
- Enable/Disable
- Tape and Reel (2,000 pcs. STD)

• PART NUMBER SELECTION [Learn More](#) - Internet Required

Part Number	Model Number	Frequency Stability ¹	Operating Temperature	Frequency Range (MHz)
728-Frequency-xxxxx	FCP90AXT	±100PPM	-10 ~ +70 (°C)	12.000 ~ 600.000
745-Frequency-xxxxx	FCP95AXT	±50PPM	-10 ~ +70 (°C)	12.000 ~ 600.000

• ELECTRICAL CHARACTERISTICS

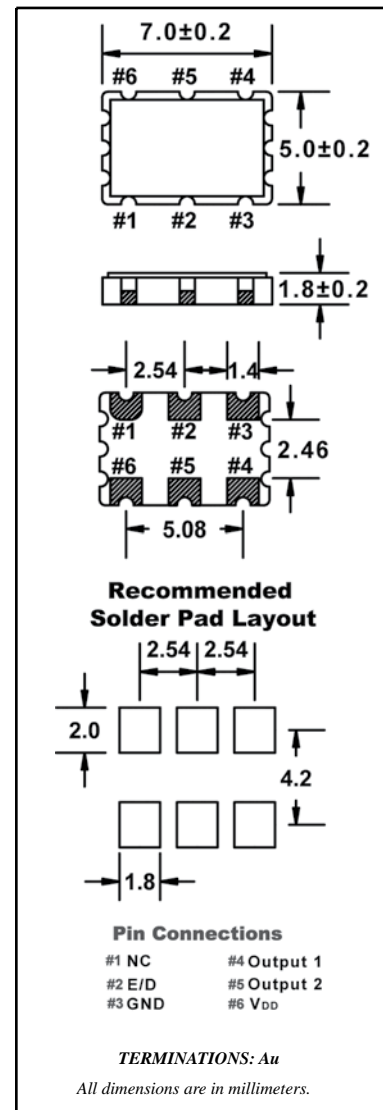
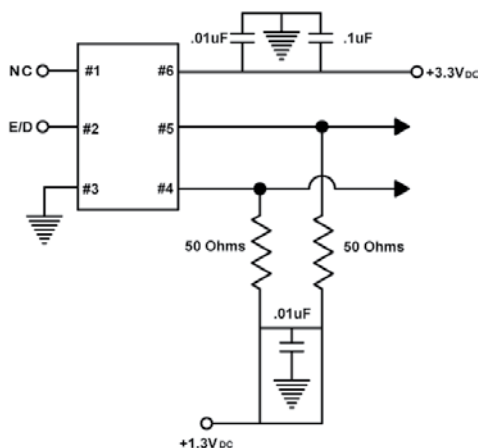
PARAMETERS	MAX (unless otherwise noted)
Frequency Range (Fo)	12.000 ~ 600.000 MHz
Storage Temperature Range (T _{STG})	-55°C ~ +125°C
Supply Voltage (V _{DD})	3.3V ± 5%
Input Current (I _{DD})	120mA
Output Symmetry (50% V _{p-p})	40% ~ 60%
Rise Time (20% ~ 80% V _{p-p}) (T _r)	0.5nS
Fall Time (80% ~ 20% V _{p-p}) (T _f)	0.5nS
Output Voltage (V _{OL})	1.7V
(V _{OH})	2.2V Min
Output Load	See Recommended Circuit
Start-up Time (T _s)	10mS
Output Disable Time	100nS
Output Enable Time	10mS
Phase Noise (@ 10kHz)	-120dBc/Hz
Phase Jitter (12kHz ~ 20MHz)	5pS RMS
Maximum Soldering Temp / Time	260°C / 10 Seconds
Moisture Sensitivity Level (MSL)	1

¹ Inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock, vibration.

² An internal pulldown resistor from pin 2 to pin 3 allows active output if pin 2 is left open. Note: A 0.01μF bypass capacitor should be placed between V_{DD} (Pin 6) and GND (Pin 3) to minimize power supply line noise.

All specifications subject to change without notice.

FCPAXT Series Recommended Circuit



• ENABLE / DISABLE FUNCTION²

(Pin 2)	OUTPUT (Pin 4, Pin 5)
OPEN	ACTIVE
'1' Level V _{IH} ≥ V _{DD} -1.1V	High Z
'0' Level V _{IL} ≤ V _{DD} -1.6V	ACTIVE