RFG60P03, RFP60P03, RF1S60P03, RF1S60P03SM

60A, 30V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 60A, 30V
- $r_{DS(ON)}$ = 0.027Ω
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG60P03, RFP60P03, RF1S60P03 and RF1S60P03SM P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

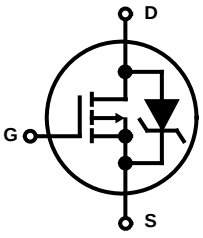
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG60P03	TO-247	RFG60P03
RFP60P03	TO-220AB	RFP60P03
RF1S60P03	TO-262AA	F1S60P03
RF1S60P03SM	TO-263AB	F1S60P03

NOTE: When ordering use the entire part number.

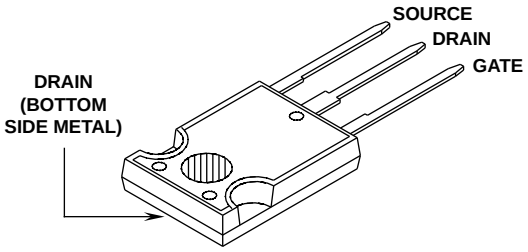
Formerly developmental type TA49045.

Symbol

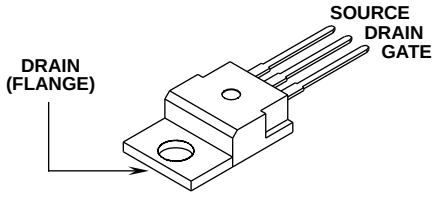


Packages

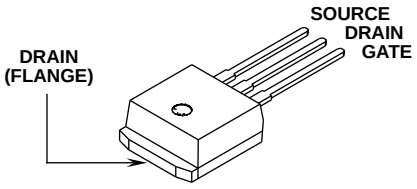
JEDEC STYLE TO-247



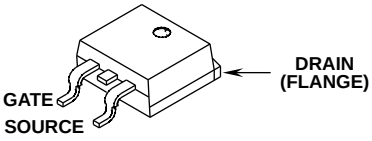
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings T_C = +25°C

		RFG60P03, RFP60P03, RF1S60P03, RFS60P03SM	UNITS
Drain Source Voltage	V_{DSS}	-30	V
Drain Gate Voltage	V_{DGR}	-30	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	60	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
T_C = +25°C	P_D	176	W
Derate above +25°C	P_T	1.17	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **3951.1**

Electrical Specifications

T_C = +25°C, Unless Otherwise Specified.

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		-30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA		-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	T_C = +25°C	-	-	-1	µA
			T_C = +150°C	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 60A, V_{GS} = -10V		-	-	0.027	Ω
Turn-On Time	t_{ON}	V_{DD} = -15V, I_D = 60A R_L = 0.25Ω, V_{GS} = -10V R_{GS} = 2.5Ω		-	-	140	ns
Turn-On Delay Time	$t_{D(ON)}$			-	20	-	ns
Rise Time	t_R			-	75	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	35	-	ns
Fall Time	t_F			-	40	-	ns
Turn-Off Time	t_{OFF}			-	-	115	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to -20V	V_{DD} = -24V, I_D = 60A, R_L = 0.4Ω	-	190	230	nC
Gate Charge at 10V	$Q_{G(-10)}$	V_{GS} = 0 to -10V		-	100	120	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to -2V		-	7.5	9	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V f = 1MHz		-	3000	-	pF
Output Capacitance	C_{OSS}			-	1500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	525	-	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	-	0.85	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = -60A	-	-	-1.75	V
Reverse Recovery Time	t_{RR}	I_{SD} = -60A, dI_{SD}/dt = -100A/µs	-	-	200	ns

Typical Performance Curves

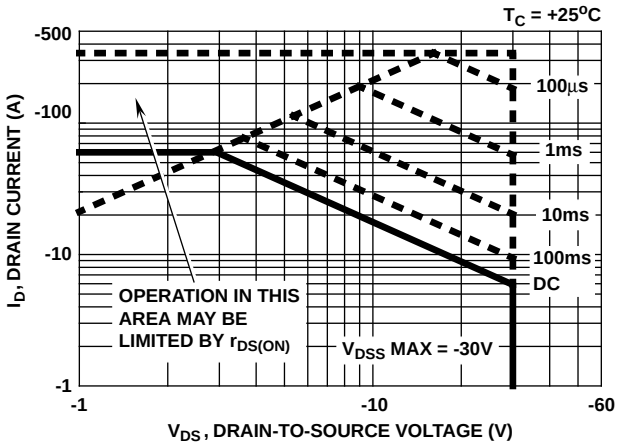


FIGURE 1. SAFE OPERATING AREA CURVE

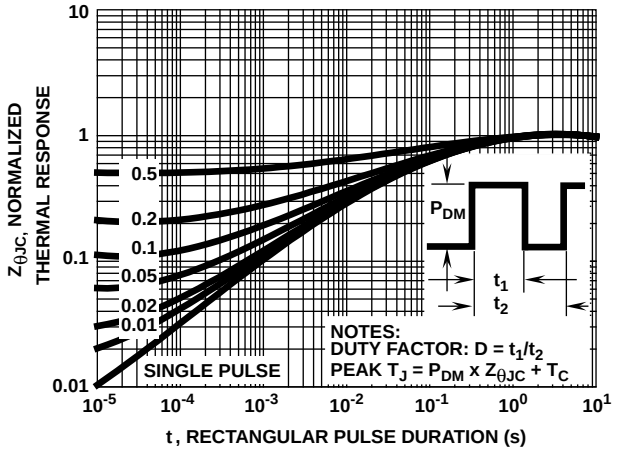


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

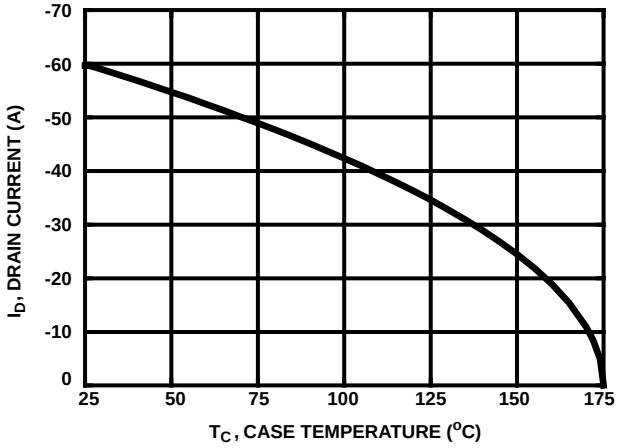


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

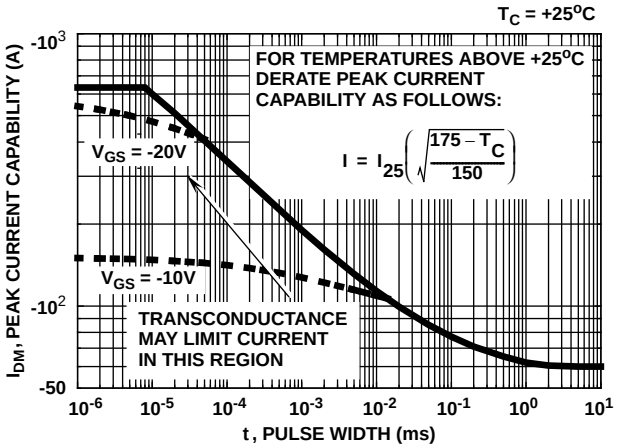


FIGURE 4. PEAK CURRENT CAPABILITY

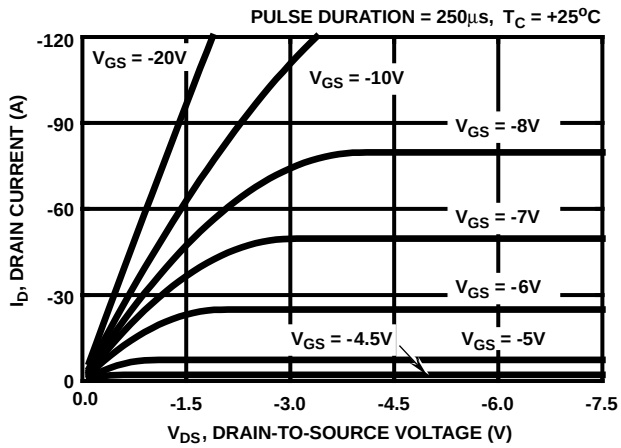


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

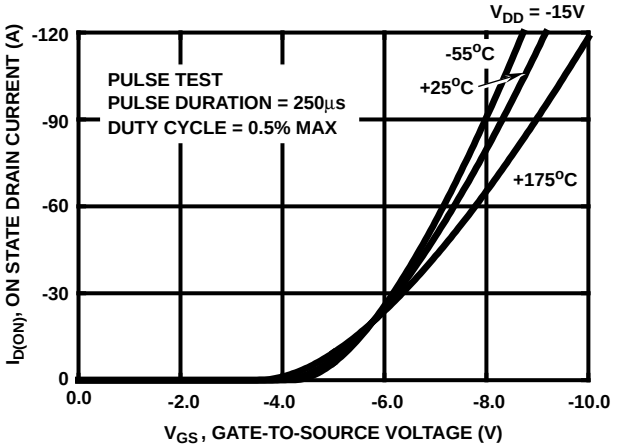


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

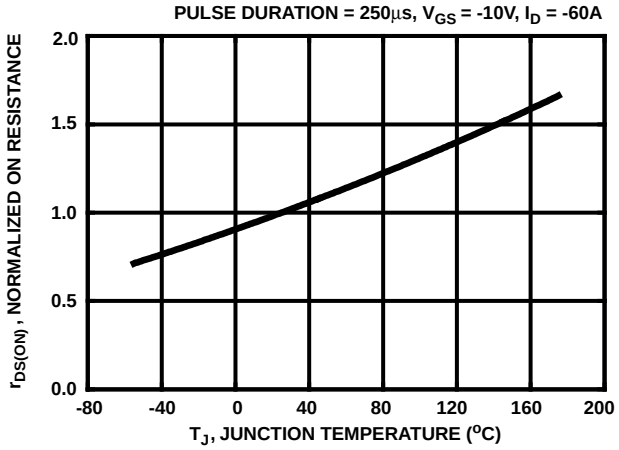


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

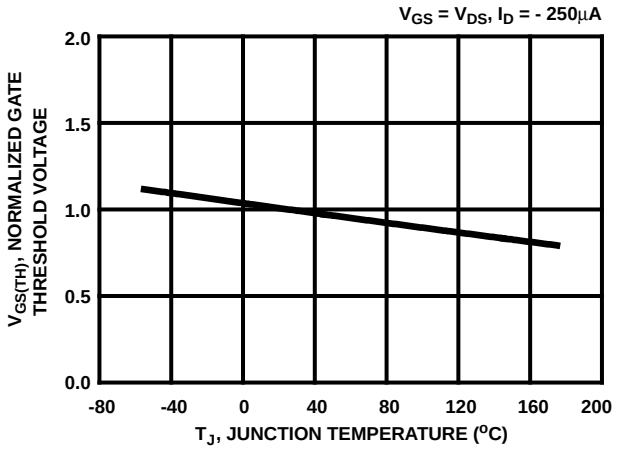


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

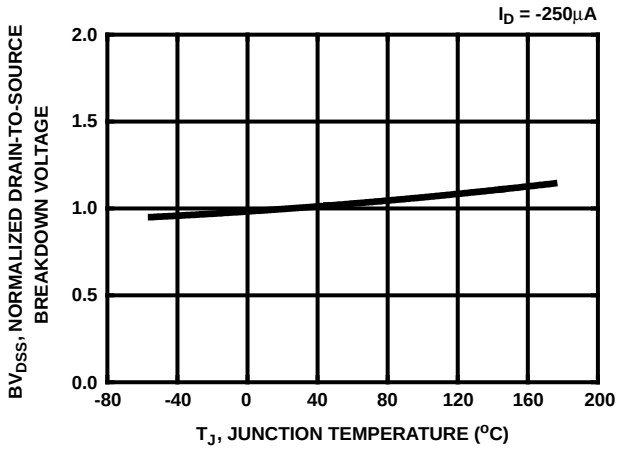


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

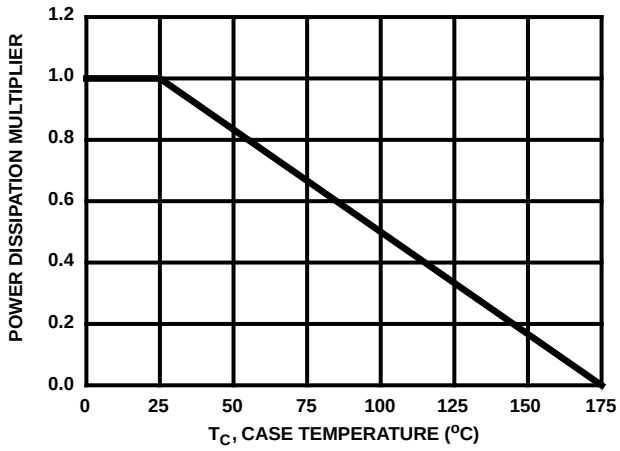


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS

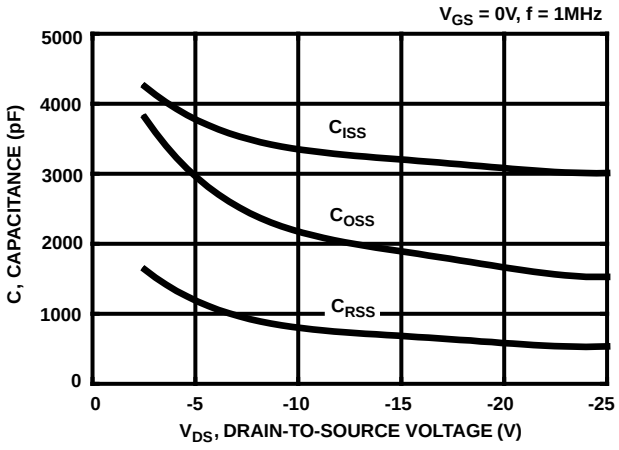


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

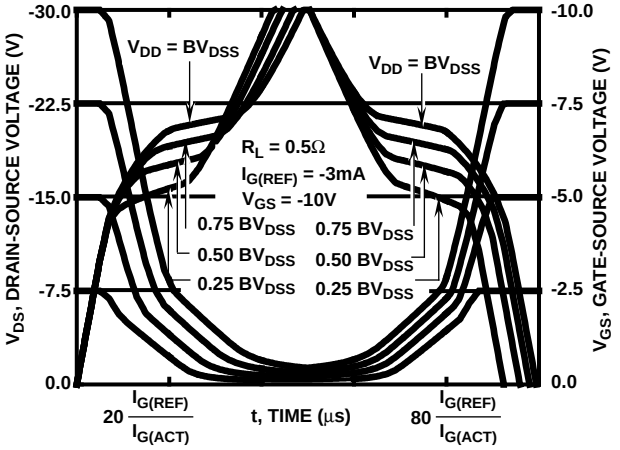


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

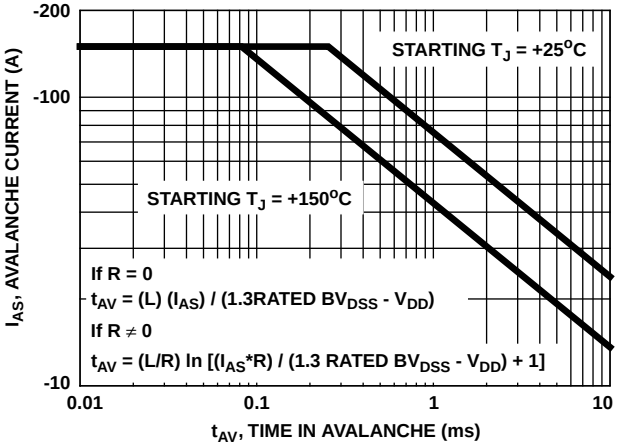


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

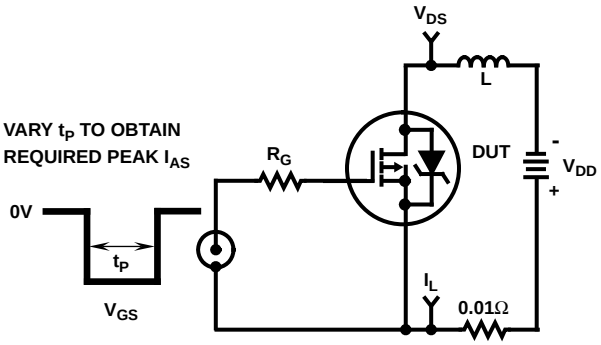


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

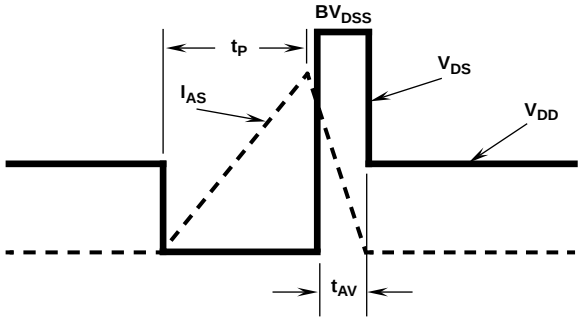


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

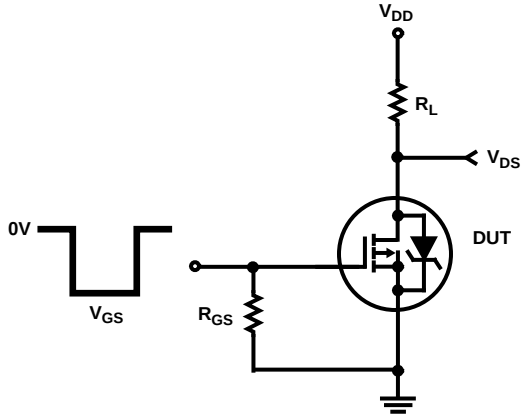


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

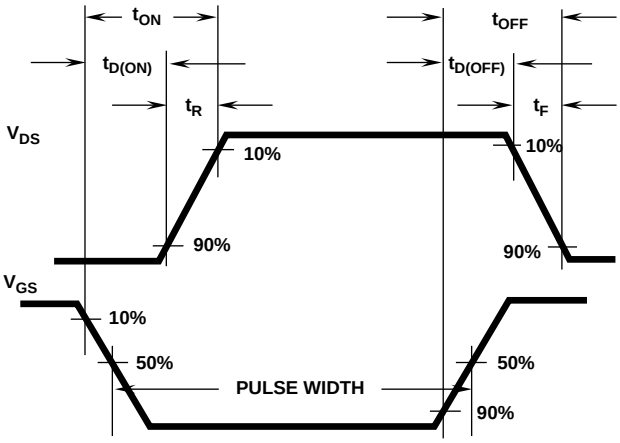


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG60P03, RFP60P03, RF1S60P03, RF1S60P03SM

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.SUBCKT RFP60P03  2  1  3                    REV 6/21/94

CA 12 8 5.01e-9
CB 15 14 3.9e-9
CIN 6 8 3.09e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -36.59
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

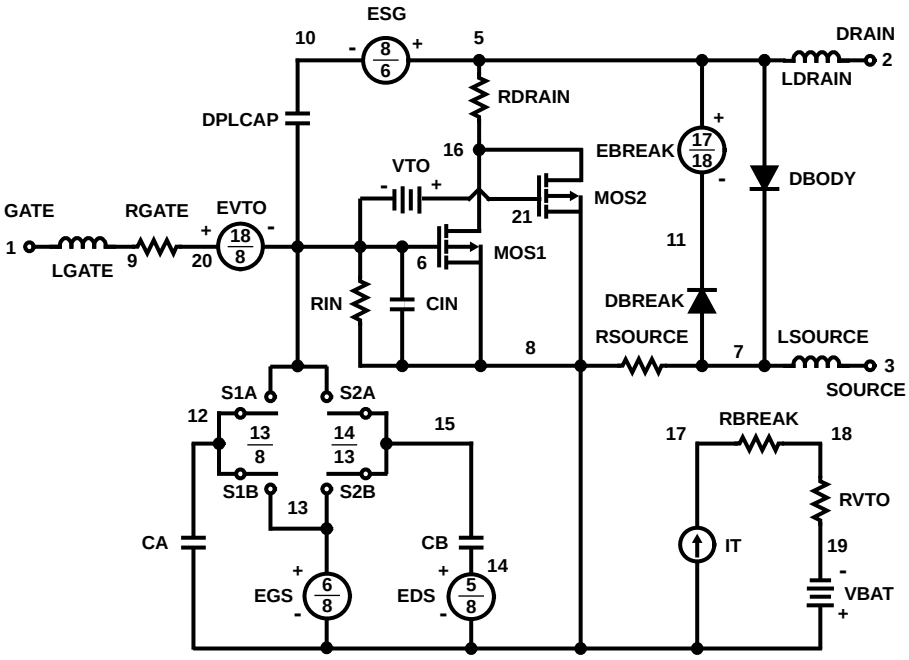
LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 2.36e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1e-4
RGATE 9 20 3.25
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 11.28e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.92
```



.MODEL DBDMOD D (IS=4.21e-13 RS=1e-2 TRS1=-2.69e-4 TRS2=-1.33e-6 CJO=5.05e-9 TT=5.33e-8)
.MODEL DBKMOD D (RS=3.80e-2 TRS1=-4.76e-4 TRS2=-4.17e-12)
.MODEL DPLCAPMOD D (CJO=4.05e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.98 KP=16.27 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=8.05e-4 TC2=1.48e-6)
.MODEL RDSMOD RES (TC1=2.80e-3 TC2=2.62e-6)
.MODEL RVTOMOD RES (TC1=-3.34e-3 TC2=1.46e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=7.5 VOFF=4.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.5 VOFF=7.5)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.43 VOFF=-3.57)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.57 VOFF=1.43)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.