



CYPRESS

CY28339

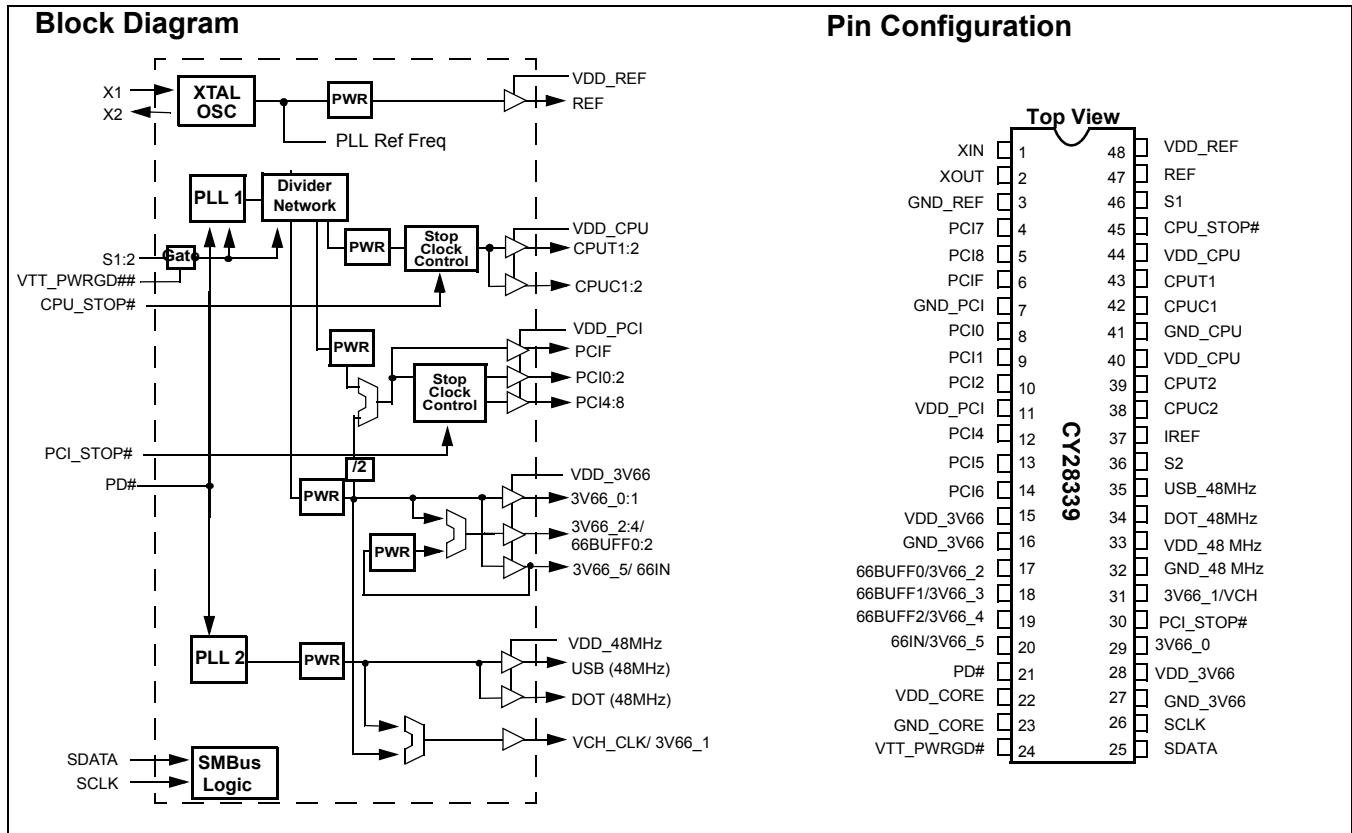
# Intel® CK408 Mobile Clock Synthesizer

## Features

- Compliant with Intel® CK 408 rev 1.1 Mobile Clock Synthesizer specifications
- 3.3V power supply
- Two differential CPU clocks
- Nine copies of PCI clocks
- Three copies configurable PCI free-running clocks
- Two 48 MHz clocks (USB, DOT)
- Five/six copies of 3V66 clocks
- One VCH clock
- One reference clock at 14.318 MHz
- SMBus support with read-back capabilities
- Ideal Lexmark profile Spread Spectrum electromagnetic interference (EMI) reduction
- Dial-a-Frequency™ features
- Dial-a-dB™ features
- 48-pin TSSOP package

Table 1. Frequency Table<sup>[1]</sup>

| S2 | S1 | CPU (1:2) | 3V66   | 66BUFF(0:2)/3V66(0:4) | 66IN/3V66-5        | PCIF, PCI | REF     | USB/ DOT |
|----|----|-----------|--------|-----------------------|--------------------|-----------|---------|----------|
| 1  | 0  | 100M      | 66M    | 66IN                  | 66-MHz clock input | 66IN/2    | 14.318M | 48M      |
| 1  | 1  | 133M      | 66M    | 66IN                  | 66-MHz clock input | 66IN/2    | 14.318M | 48M      |
| 0  | 0  | 100M      | 66M    | 66M                   | 66M                | 33 M      | 14.318M | 48M      |
| 0  | 1  | 133M      | 66M    | 66M                   | 66M                | 33 M      | 14.318M | 48M      |
| M  | 0  | TCLK/2    | TCLK/4 | TCLK/4                | TCLK/4             | TCLK/8    | TCLK    | TCLK/2   |



**Note:**

1. TCLK is a test clock driven on the XTAL\_IN input during test mode. M = driven to a level between 1.0V and 1.8V. If the S2 pin is at a M level during power-up, a 0 state will be latched into the device's internal state register.

**Pin Definitions**

| Pin Number                    | Name  | I/O | Description  |
|-------------------------------|---|-----|--|
| 47                            | REF0  |     | <b>3.3V 14.318-MHz clock output.</b>   |
| 1                             | XIN   |     | <b>14.318-MHz crystal input.</b>   |
| 2                             | XOUT  |     | <b>14.318-MHz crystal input.</b>   |
| 43, 42,<br>39, 38             | CPUT1, CPUC1<br>CPUT2, CPUC2                              |     | <b>Differential CPU clock outputs.</b>   |
| 29                            | 3V66_0  |     | <b>3.3V 66-MHz clock output.</b>   |
| 31                            | 3V66_1/VCH  |     | <b>3.3V selectable through SMBus to be 66 MHz or 48 MHz.</b>   |
| 20                            | 66IN/3V66_5   |     | <b>66-MHz input to buffered 66BUFF and PCI or 66-MHz clock from internal VCO.</b>  |
| 17, 18, 19                    | 66BUFF [2:0]<br>/3V66 [4:2]                               |     | <b>66-MHz buffered outputs from 66Input or 66-MHz clocks from internal VCO.</b>  |
| 6                             | PCIF  |     | <b>33 MHz clocks divided down from 66Input or divided down from 3V66; PCIF default is free-running.</b>  |
| 8, 9, 10, 12, 13,<br>14, 4, 5 | PCI [0:2]<br>PCI [4:6]<br>PCI [7:8]                       |     | <b>PCI clock outputs divided down from 66Input or divided down from 3V66; PCI [7:8] are configurable as free-running PCI through SMBus.<sup>[2]</sup></b>  |
| 35                            | USB_48M   |     | <b>Fixed 48-MHz clock output.</b>  |
| 34                            | DOT_48M   |     | <b>Fixed 48-MHz clock output.</b>  |
| 36                            | S2  |     | <b>Special 3.3V three-level input for Mode selection.</b>  |
| 46                            | S1  |     | <b>3.3V LVTTTL inputs for CPU frequency selection.</b>   |
| 37                            | IREF  |     | <b>A precision resistor is attached to this pin which is connected to the internal current reference.</b>  |
| 21                            | PD#   |     | <b>3.3V LVTTTL input for Power_Down# (active LOW).</b>   |
| 30                            | PCI_STOP#   |     | <b>3.3V LVTTTL input for PCI_STOP# (active LOW).</b>   |
| 45                            | CPU_STOP#   |     | <b>3.3V LVTTTL input for CPU_STOP# (active LOW).</b>   |
| 24                            | VTT_PWRGD#  |     | <b>3.3V LVTTTL input is a level-sensitive strobe used to determine when S[2:1] inputs are valid and OK to be sampled (Active LOW). Once VTT_PWRGD# is sampled LOW, the status of this input will be ignored.</b> |
| 25                            | SDATA   |     | <b>SMBus-compatible SDATA.</b>   |
| 26                            | SCLK  |     | <b>SMBus-compatible SCLK.</b>  |
| 11, 15, 28, 40, 44,<br>48     | VDD_PCI,<br>VDD_3V66,<br>VDD_CPU, VDD_RE<br>F             |     | <b>3.3V power supply for outputs.</b>  |
| 33                            | VDD_48 MHz  |     | <b>3.3V power supply for 48 MHz.</b>   |
| 22                            | VDD_CORE  |     | <b>3.3V power supply for phase-locked loop (PLL).</b>  |
| 3, 7, 16, 27, 32,<br>41       | GND_REF,<br>GND_PCI,<br>GND_3V66,<br>GND_IREF,<br>GND_CPU |     | <b>Ground for outputs.</b>   |
| 23                            | GND_CORE  |     | <b>Ground for PLL.</b>   |

**Note:**

2. PCI3 is internally disabled and is not accessible.

## Two-Wire SMBus Control Interface

The two-wire control interface implements a Read/Write slave only interface according to SMBus specification.

The device will accept data written to the D2 address and data may read back from address D3. It will not respond to any other addresses, and previously set control registers are retained as long as power is maintained on the device.

## Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:

1. "Command code" byte
2. "Byte count" byte.

Although the data (bits) in the command is considered "don't care," it must be sent and will be acknowledged. After the Command Code and the Byte Count have been acknowledged, the sequence (Byte 0, Byte 1, and Byte 2) described below will be valid and acknowledged.

### Byte 0: CPU Clock Register<sup>[3,4]</sup>

| Bit | @Pu<br>p | Name           | Description  |
|-----|----------|----------------|--|
| 7   | 0        |                | Spread Spectrum Enable.<br>0 = Spread Off, 1 = Spread On. This is a Read and Write control bit.  |
| 6   | 0        |                | CPU Clock Power-down Mode Select.<br>0 = Drive CPUT to 2x IREF and drive CPUC LOW<br>1 = Tri-state all CPU outputs.<br>This is only applicable when PD# is LOW. It is not applicable to CPU_STOP#. |
| 5   | 0        | 3V66_1/VC<br>H | 3V66_1/VCH Frequency Select<br>0 = 66M selected, 1 = 48M selected. This is a Read and Write control bit.   |
| 4   |          |                | Reserved   |
| 3   | HW       | PCI_STOP#      | Reflects the current value of the internal PCI_STOP# function when read. Internally PCI_STOP# is a logical AND function of the internal SMBus register bit and the external PCI_STOP# pin.         |
| 2   | HW       | S2             | Frequency Select Bit 2. Reflects the value of S2. This bit is Read-only.   |
| 1   | HW       | S1             | Frequency Select Bit 1. Reflects the value of S1. This bit is Read-only.   |
| 0   | 1        |                | Reserved   |

### Byte 1: CPU Clock Register

| Bit | @Pu<br>p | Name                         | Description  |
|-----|----------|------------------------------|--|
| 7   | 1        |                              | Reserved   |
| 6   | 0        | CPUT1, CPUC1<br>CPUT2, CPUC2 | CPUT/C Output Functionality Control when CPU_STOP# is asserted.<br>0 = Drive CPUT to 6x IREF and drive CPUC LOW<br>1 = three-state all CPU outputs.<br>This bit will override Byte0, Bit6 such that even if it is 0, when PD# goes LOW the CPU outputs will be three-stated. |
| 5   | 0        | CPUT2, CPUC2                 | CPUT/C2 Functionality Control when CPU_STOP# is asserted.<br>0 = Stopped LOW, 1 = Free Running. This is a Read and Write control bit.  |
| 4   | 0        | CPUT1, CPUC1                 | CPUT/C1 Functionality Control When CPU_STOP# is asserted.<br>0 = Stopped LOW, 1 = Free Running. This is a Read and Write control bit.  |
| 3   | 0        |                              | Reserved   |
| 2   | 1        | CPUT2, CPUC2                 | CPUT/C2 Output Control.<br>0 = disable, 1 = enabled. This is a Read and Write control bit.   |
| 1   | 1        | CPUT1, CPUC1                 | CPUT/C1 Output Control.<br>0 = disable, 1 = enabled. This is a Read and Write control bit.   |
| 0   | 1        |                              | Reserved   |

#### Notes:

3. PU = internal pull-up. PD = internal pull-down. T = tri-level logic input with valid logic voltages of LOW = < 0.8V, T = 1.0 – 1.8V and HIGH = > 2.0V.
4. The "Pin#" column lists the relevant pin number where applicable. The "@Pup" column gives the default state at power-up.

**Byte 2: PCI Clock Control Register** (all bits are Read and Write functional)

| Bit | @Pup | Name | Description  |
|-----|------|------|--|
| 7   | 0    | REF  | REF Output Control. 0 = high strength, 1 = low strength. |
| 6   | 1    | PCI6 | PCI6 Output Control. 0 = forced LOW, 1 = enabled         |
| 5   | 1    | PCI5 | PCI5 Output Control. 0 = forced LOW, 1 = enabled         |
| 4   | 1    | PCI4 | PCI4 Output Control. 0 = forced LOW, 1 = enabled         |
| 3   | 1    |      | Reserved   |
| 2   | 1    | PCI2 | PCI2 Output Control. 0 = forced LOW, 1 = enabled         |
| 1   | 1    | PCI1 | PCI1 Output Control. 0 = forced LOW, 1 = enabled         |
| 0   | 1    | PCI0 | PCI0 Output Control. 0 = forced LOW, 1 = enabled         |

**Byte 3: PCIF Clock and 48M Control Register** (all bits are Read and Write functional)

| Bit | @Pup | Name    | Description  |
|-----|------|---------|--|
| 7   | 1    | DOT_48M | DOT_48M Output Control. 0 = forced LOW, 1 = enabled                                  |
| 6   | 1    | USB_48M | USB_48M Output Control. 0 = forced LOW, 1 = enabled                                  |
| 5   | 0    | PCIF    | PCI_STOP# Control of PCIF. 0 = Free Running, 1 = Stopped when PCI_STOP# is asserted. |
| 4   | 1    | PCI8    | PCI_STOP# Control of PCI8. 0 = Free Running, 1 = Stopped when PCI_STOP# is asserted. |
| 3   | 1    | PCI7    | PCI_STOP# Control of PCI7. 0 = Free Running, 1 = Stopped when PCI_STOP# is asserted. |
| 2   | 1    | PCIF    | PCIF Output Control. 0 = forced LOW, 1 = running                                     |
| 1   | 1    | PCI_8   | PCI_8 Output Control. 0 = forced LOW, 1 = running                                    |
| 0   | 1    | PCI_7   | PCI_7 Output Control. 0 = forced LOW, 1 = running                                    |

**Byte 4: Control Register** (all bits are Read and Write functional)

| Bit | @Pup | Name           | Description   |
|-----|------|----------------|---|
| 7   | 0    |                | SS2 Spread Spectrum Control Bit. 0 = down spread, 1 = center spread). |
| 6   | 0    |                | Reserved. Set = 0.  |
| 5   | 1    | 3V66_0         | 3V66_0 Output Enable. 0 = disable, 1 = enabled                        |
| 4   | 1    | 3V66_1/VCH     | 3V66_1/VCH Output Enable. 0 = disable, 1 = enabled                    |
| 3   | 1    | 3V66_5         | 3V66_5 Output Enable. 0 = disable, 1 = enabled                        |
| 2   | 1    | 19             | 66BUFF2/3V66_4 Output Enable. 0 = disable, 1 = enabled                |
| 1   | 1    | 18             | 66BUFF1/3V66_3 Output Enable. 0 = disable, 1 = enabled                |
| 0   | 1    | 66BUFF0/3V66_2 | 66BUFF0/3V66_2 Output Enable. 0 = disable, 1 = enabled                |

**Byte 5: Clock Control Register** (all bits are Read and Write functional)

| Bit | @Pup | Name    | Description  |
|-----|------|---------|--|
| 7   | 0    |         | SS1 Spread Spectrum Control Bit.                                     |
| 6   | 1    |         | SS0 Spread Spectrum Control Bit.                                     |
| 5   | 0    |         | 66IN to 66M delay Control MSB.                                       |
| 4   | 0    |         | 66IN to 66M delay Control LSB.                                       |
| 3   | 0    |         | Reserved. Set = 0.   |
| 2   | 0    | DOT_48M | DOT_48M Edge Rate Control. When set to 1, the edge is slowed by 15%. |
| 1   | 0    |         | Reserved. Set = 0.   |
| 0   | 0    | USB_48M | USB_48M edge rate control. When set to 1, the edge is slowed by 15%. |

**Byte 6: Silicon Signature Register<sup>[5]</sup>** (all bits are Read-only)

| Bit | @Pup | Name | Description        |
|-----|------|------|--------------------|
| 7   | 0    |      | Revision = 0001    |
| 6   | 0    |      |                    |
| 5   | 0    |      |                    |
| 4   | 1    |      |                    |
| 3   | 0    |      | Vendor Code = 0011 |
| 2   | 0    |      |                    |
| 1   | 1    |      |                    |
| 0   | 1    |      |                    |

**Byte 7: Reserved Register**

| Bit | @Pup | Name | Description        |
|-----|------|------|--------------------|
| 7   | 0    |      | Reserved. Set = 0. |
| 6   | 0    |      | Reserved. Set = 0. |
| 5   | 0    |      | Reserved. Set = 0. |
| 4   | 0    |      | Reserved. Set = 0. |
| 3   | 0    |      | Reserved. Set = 0. |
| 2   | 0    |      | Reserved. Set = 0. |
| 1   | 0    |      | Reserved. Set = 0. |
| 0   | 0    |      | Reserved. Set = 0. |

**Byte 8: Dial-a-Frequency Control Register N**

| Bit | @Pup | Name    | Description  |
|-----|------|---------|--|
| 7   | 0    |         | Reserved. Set = 0.   |
| 6   | 0    | N6, MSB | These bits are for programming the PLL's internal N register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock. |
| 5   | 0    | N5      |  |
| 4   | 0    | N4      |  |
| 3   | 0    | N3      |  |
| 2   | 0    | N2      |  |
| 1   | 0    | N1      |  |
| 0   | 0    | N0, LSB |  |

**Byte 9: Dial-a-Frequency Control Register R**

| Bit | @Pup | Name    | Description  |
|-----|------|---------|--|
| 7   | 0    |         | Reserved. Set = 0.   |
| 6   | 0    | R5, MSB | These bits are for programming the PLL's internal R register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock. |
| 5   | 0    | R4      |  |
| 4   | 0    | R3      |  |
| 3   | 0    | R2      |  |
| 2   | 0    | R1      |  |
| 1   | 0    | R0      |  |
| 0   | 0    | DAF_ENB | R and N register mux selection. 0 = R and N values come from the ROM. 1 = data is loaded from DAF (SMBus) registers.   |

**Note:**

- When writing to this register, the device will acknowledge the Write operation, but the data itself will be ignored.

## Dial-a-Frequency Features

SMBus Dial-a-Frequency feature is available in this device via Byte8 and Byte9.

P is a large-value PLL constant that depends on the frequency selection achieved through the hardware selectors (S1, S0). P value may be determined from *Table 2*.

**Table 2. P Value**

| S(1:0) | P        |
|--------|----------|
| 0 0    | 32005333 |
| 0 1    | 48008000 |
| 1 0    | 96016000 |
| 1 1    | 64010667 |

## Dial-a-dB Features

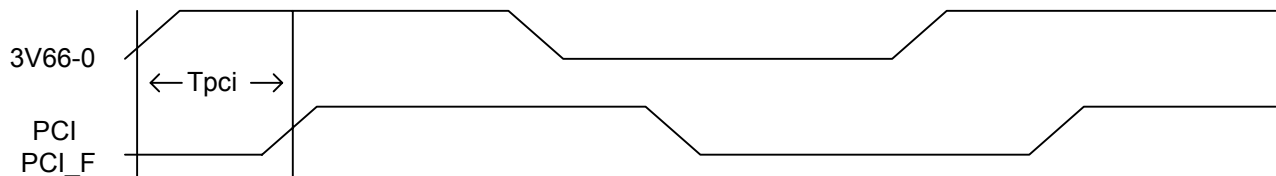
SMBus Dial-a-dB feature is available in this device via Byte8 and Byte9.

## Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique used to minimizing EMI radiation generated by repetitive digital signals. A clock presents the greatest EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any one point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting specific register bits in the SMBus control bytes. *Table 3* is a listing of the modes and percentages of Spread Spectrum modulation that this device incorporates.

**Table 3. Spread Spectrum**

| SS2 | SS1 | SS0 | Spread Mode | Spread%      |
|-----|-----|-----|-------------|--------------|
| 0   | 0   | 0   | Down        | +0.00, -0.25 |
| 0   | 0   | 1   | Down        | +0.00, -0.50 |
| 0   | 1   | 0   | Down        | +0.00, -0.75 |
| 0   | 1   | 1   | Down        | +0.00, -1.00 |
| 1   | 0   | 0   | Center      | +0.13, -0.13 |
| 1   | 0   | 1   | Center      | +0.25, -0.25 |
| 1   | 1   | 0   | Center      | +0.37, -0.37 |
| 1   | 1   | 1   | Center      | +0.50, -1.50 |



**Figure 1. Unbuffered Mode – 3V66\_0 to PCI and PCIF Phase Relationship**

## Special Functions

### PCIF and IOAPIC Clock Outputs

The PCIF clock outputs are intended to be used, if required, for systems IOAPIC clock functionality. Any two of the PCIF clock outputs can be used as IOAPIC 33-Mhz clock outputs. They are 3.3V outputs will be divided down via a simple resistive voltage divider to meet specific system IOAPIC clock voltage requirements. In the event that these clocks are not required, they can be used as general PCI clocks or disabled via the assertion of the PCI\_STOP# pin.

### 3V66\_1/VCH Clock Output

The 3V66\_1/VCH pin has a dual functionality that is selectable via SMBus.

#### Configured as DRCG (66M), SMBus Byte0, Bit 5 = “0”

The default condition for this pin is to power-up in a 66M operation. In 66M operation this output is SSCG-capable and when spreading is turned on, this clock will be modulated.

#### Configured as VCH (48M), SMBus Byte0, Bit 5 = “1”

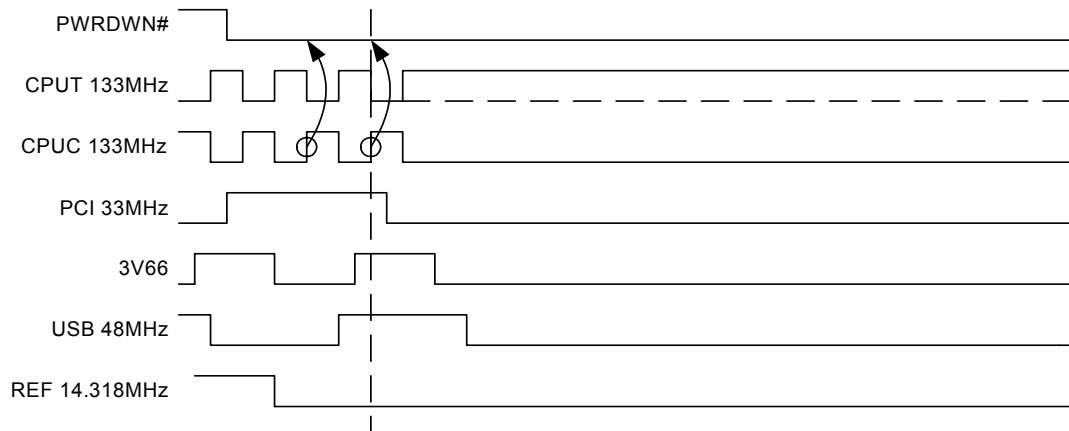
In this mode, output is configured as a 48-Mhz non-spread spectrum output that is phase-aligned with other 48M outputs (USB and DOT) to within 1-ns pin-to-pin skew. The switching of 3V66\_1/VCH into VCH mode occurs at system power-on. When the SMBus Bit 5 of Byte 0 is programmed from a “0” to a “1,” the 3V66\_1/VCH output may glitch while transitioning to 48M output mode.

### PD# (Power-down) Clarification

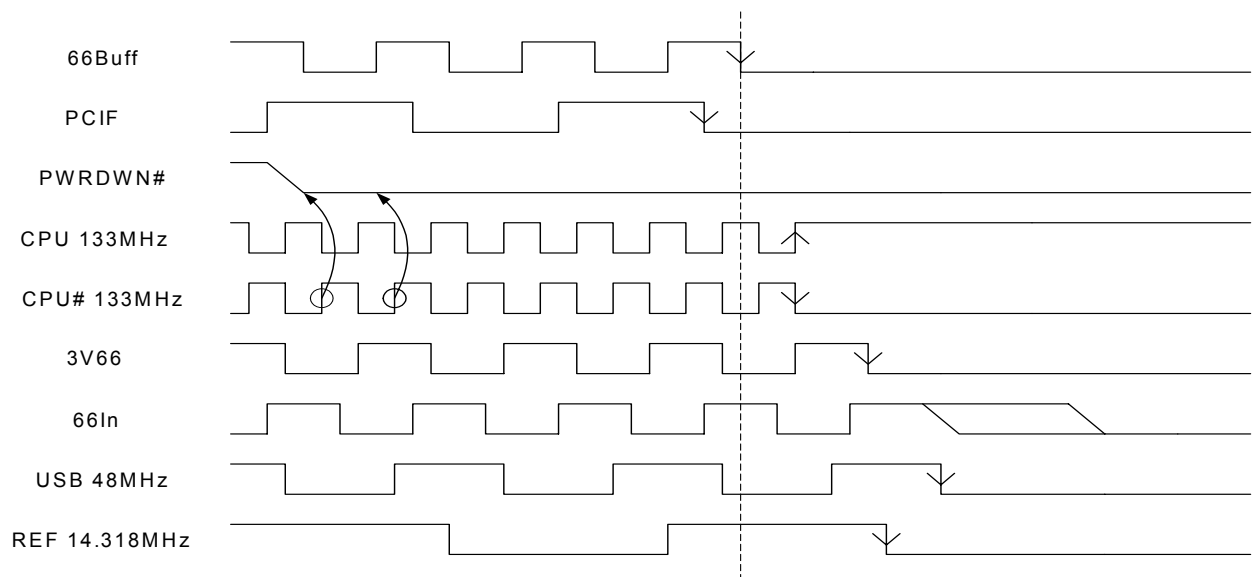
The PD# (power-down) pin is used to shut off all clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is LOW, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the LOW “stopped” state.

### PD# Assertion

When PD# is sampled LOW by two consecutive rising edges of the CPUC clock, then on the next HIGH-to-LOW transition of PCIF, the PCIF clock is stopped LOW. On the next HIGH-to-LOW transition of 66BUFF, the 66BUFF clock is stopped LOW. From this time, each clock will stop LOW on its next HIGH-to-LOW transition, except the CPUC clock. The CPU clocks are held with the CPUC clock pin driven HIGH with a value of  $2 \times I_{ref}$ , and CPUC undriven. After the last clock has stopped, the rest of the generator will be shut down.



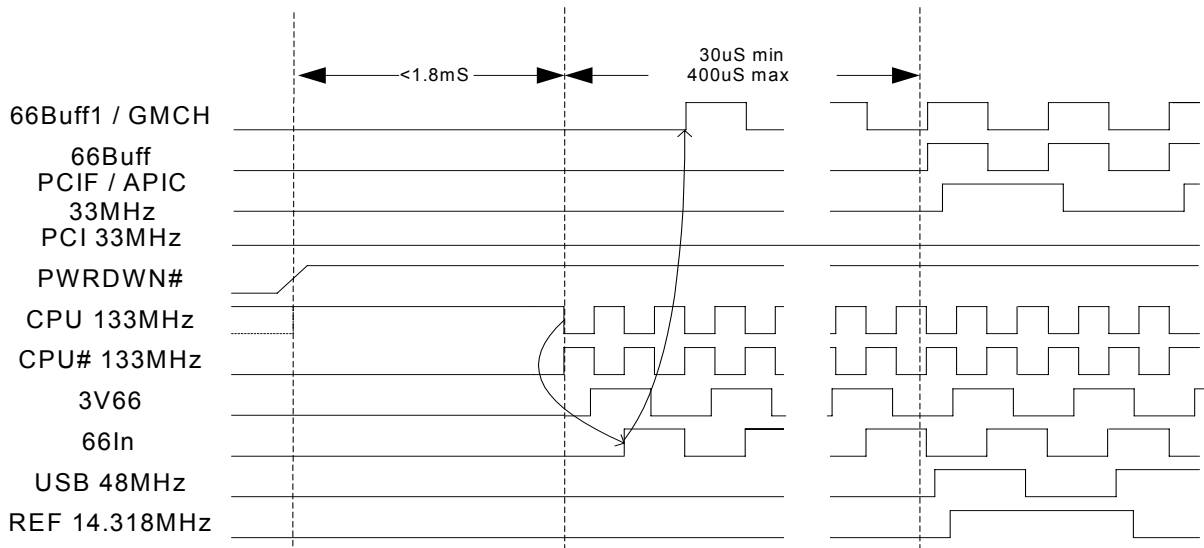
**Figure 2. Power-down Assertion Timing Waveforms – Unbuffered Mode**



**Figure 3. Power-down Assertion Timing Waveforms Figure – Buffered Mode**

**PD# Deassertion**

The power-up latency between PD# rising to a valid logic '1' level and the starting of all clocks is less than 3.0 ms.



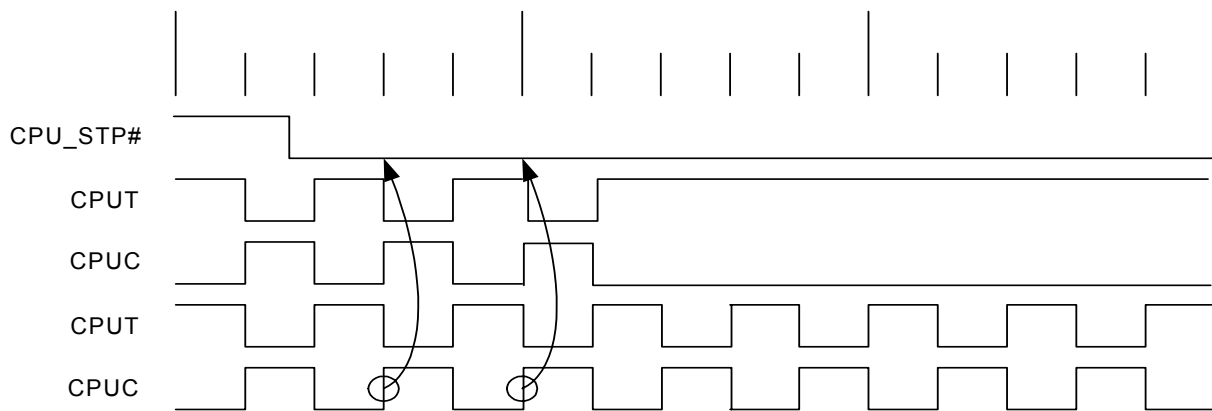
**Figure 4. Power-down Deassertion Timing Waveforms – Buffered Mode**

**CPU\_STOP# Clarification**

The CPU\_STOP# signal is an active LOW input used to synchronously stop and start the CPU output clocks while the rest of the clock generator continues to function.

**CPU\_STOP# Assertion**

When CPU\_STOP# pin is asserted, all CPUT/C outputs that are set with the SMBus configuration to be stoppable via assertion of CPU\_STOP# will be stopped after being sampled by two falling CPUT/C clock edges. The final state of the stopped CPU signals is CPUT = HIGH and CPU0C = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to (Mult 0 "select") × (Iref), and the CPUC signal will not be driven. Due to external pull-down circuitry CPUC will be LOW during this stopped state.

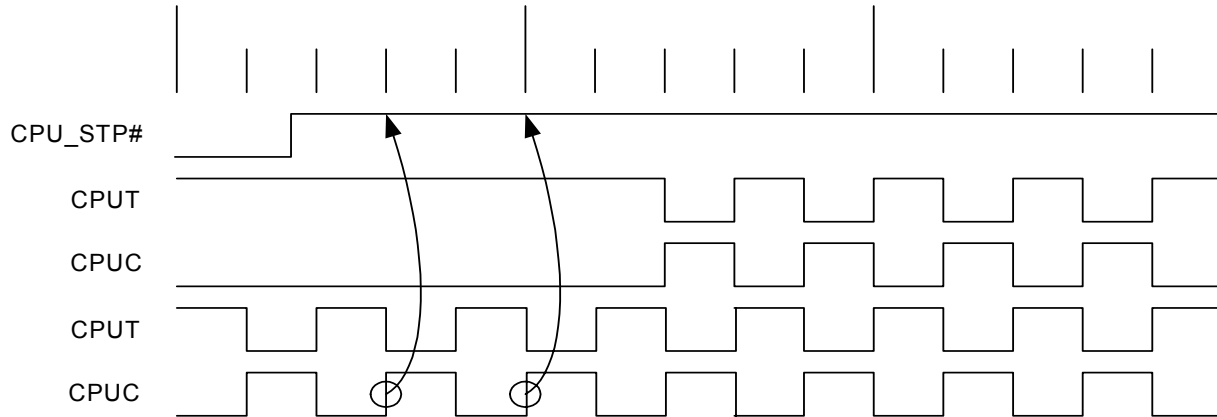


**Figure 5. CPU\_STOP# Assertion Waveform**



### CPU\_STOP# Deassertion

The deassertion of the CPU\_STOP# signal will cause all CPUC/C outputs that were stopped to resume normal operation in a synchronous manner (meaning that no short or stretched clock pulses will be produced when the clock resumes). The maximum latency from the deassertion to active outputs is no more than two CPUC clock cycles.



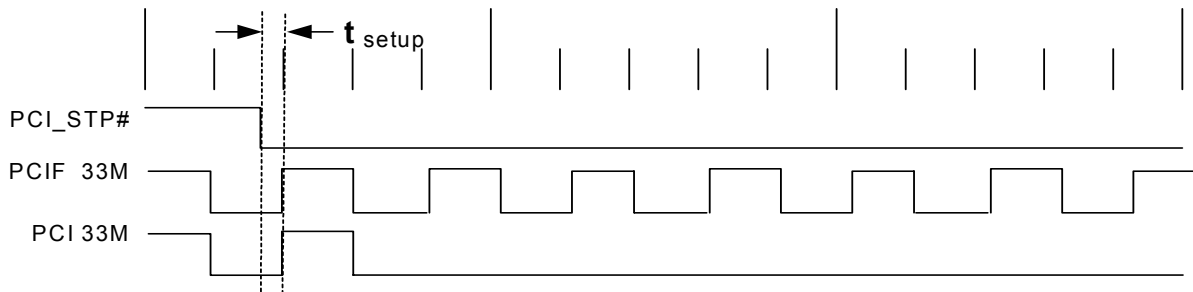
**Figure 6. CPU\_STOP# De-assertion Waveform**

### Three-state Control of CPU Clocks Clarification

During CPU\_STOP# and PD# modes, CPU clock outputs may be set to driven or undriven (tri-state) by setting the corresponding SMBus entry in Bit6 of Byte0 and Bit6 of Byte1.

### PCI\_STOP# Assertion

The PCI\_STOP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI\_STOP# going LOW is 10 ns ( $t_{setup}$ ) (see Figure 2.) The PCIF clocks will not be affected by this pin if their control bits in the SMBus register are set to allow them to be free running.



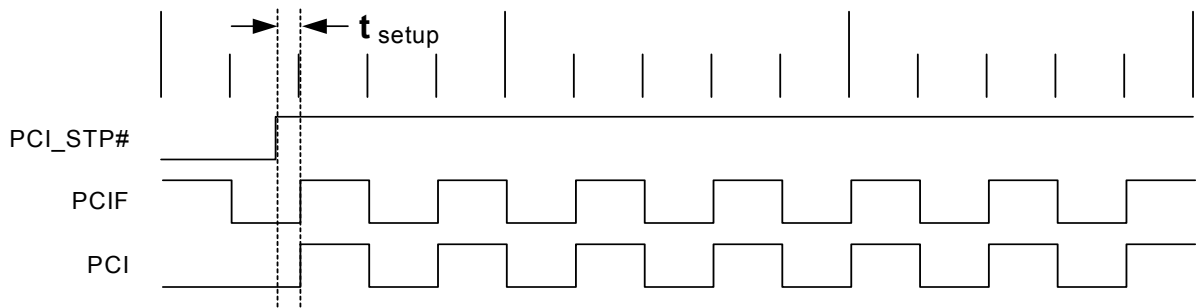
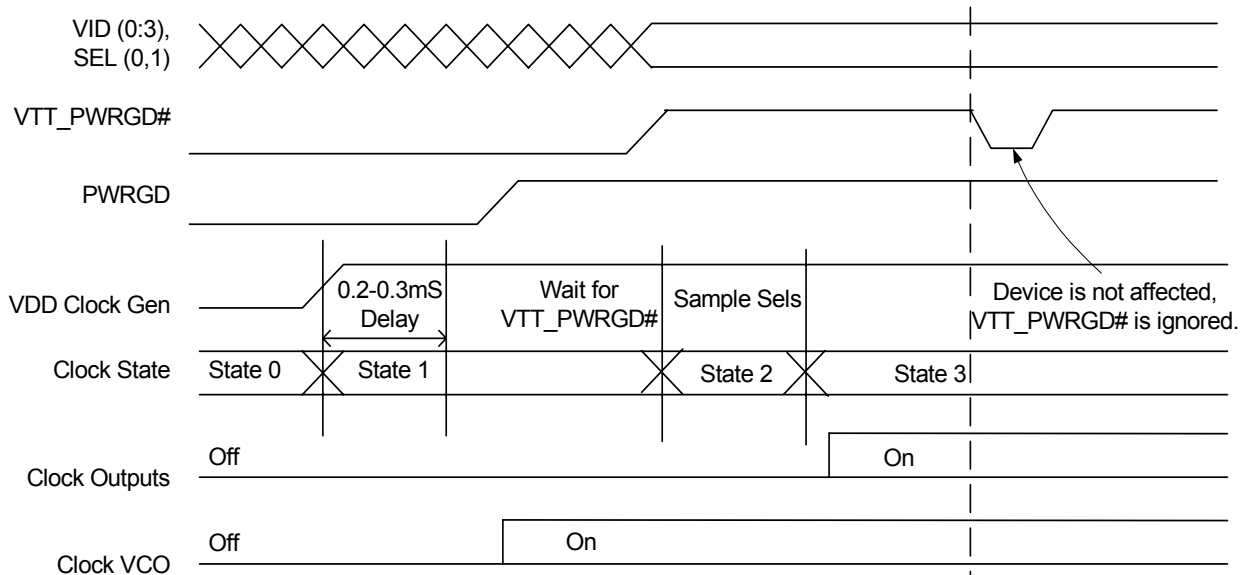
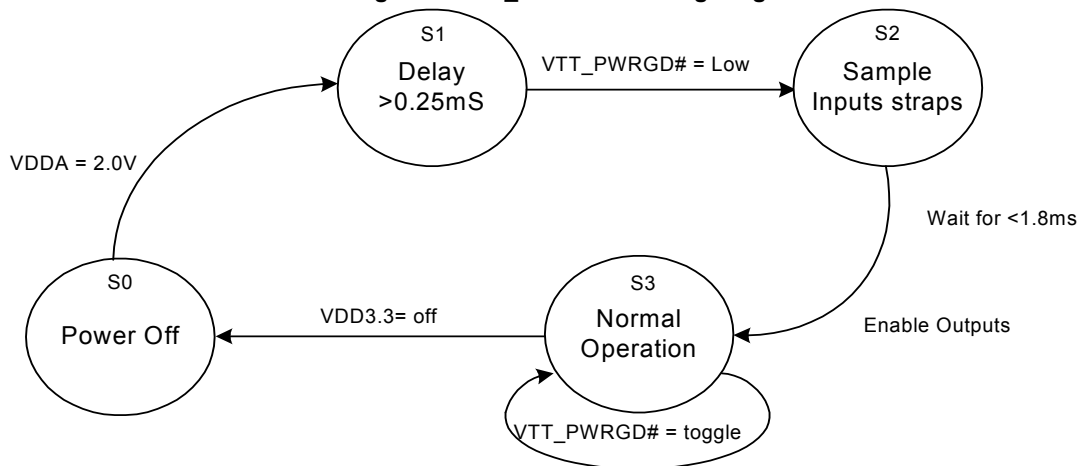
**Figure 7. PCI\_STOP# Assertion Waveform**

### PCI\_STOP# Deassertion

The deassertion of the PCI\_STOP# signal will cause all PCI(0:2, 4:8) and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI\_STOP# transitions to a HIGH level.

The PCI STOP function is controlled by two inputs. One is the device PCI\_STOP# pin number 34 and the other is SMBus

Byte 0, Bit 3. These two inputs to the function are logically AND'ed. If either the external pin or the internal SMBus register bit is set LOW, the stoppable PCI clocks will be stopped in a logic LOW state. Reading SMBus Byte 0, Bit 3 will return a 0 value if either of these control bits are set LOW (which indicates that the devices stoppable PCI clocks are not running).


**Figure 8. PCI\_STOP# Deassertion Waveform**

**Figure 9. VTT\_PWRGD# Timing Diagram**

**Figure 10. Clock Generator Power-up/Run State Program**

Iout is selectable depending on implementation. The parameters above apply to all configurations. Vout is the voltage at the pin of the device.

The various output current configurations are shown in the host swing select functions table. For all configurations, the deviation from the expected output current is  $\pm 7\%$  as shown in the current accuracy table.

**Table 4. CPU Clock Current Select Function**

| Board Target Trace/Term Z | Reference R, Iref – Vdd (3*Rr) | Output Current | Voh @ Z   |
|---------------------------|--------------------------------|----------------|-----------|
| 50Ω                       | Rr = 330 1%, Iref = 3.33mA     | Ioh = 6*Iref   | 1.0V @ 50 |
| 50Ω                       | Rr = 475 1%, Iref = 2.32mA     | Ioh = 6*Iref   | 0.7V @ 50 |

**Table 5. Group Timing Relationship and Tolerances**

| Description               | Offset | Tolerance | Conditions                       |
|---------------------------|--------|-----------|----------------------------------|
| 3V66 to PCI               | 2.5 ns | ±1.0 ns   | 3V66 leads PCI (unbuffered mode) |
| USB_48M to DOT_48M Skew   | 0.0 ns | ±1.0 ns   | 0 degrees phase shift            |
| 66BUFF(0:2) to PCI offset | 2.5 ns | ±1.0 ns   | 66BUFF leads PCI (buffered mode) |

### USB\_48M and DOT\_48M Phase Relationship

The USB\_48M and DOT\_48M clocks are in phase. It is understood that the difference in edge rate will introduce some inherent offset. When 3V66\_1/VCH clock is configured for VCH (48-MHz) operation it is also in phase with the USB and DOT outputs. See *Figure 11*.

### 66IN to 66BUFF(0:2) Buffered Prop Delay

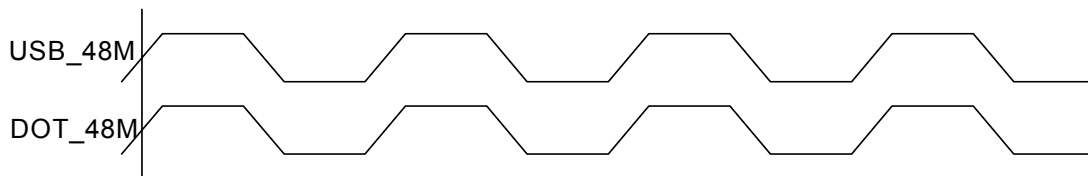
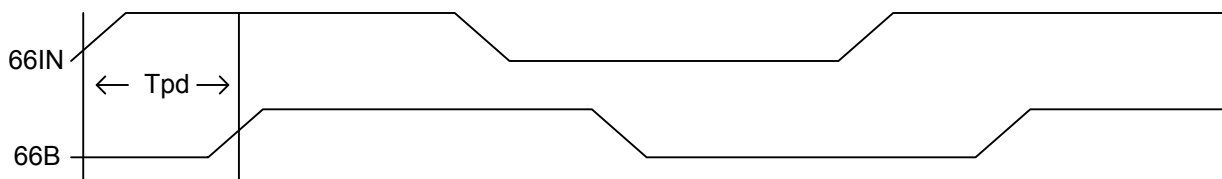
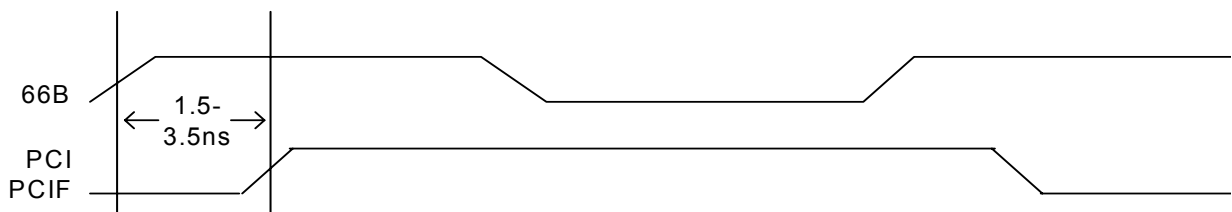
The 66IN to 66BUFF(0:2) output delay is shown in *Figure 12*. The Tpd is the prop delay from the input pin (66IN) to the output pins (66BUFF[0:2]). The outputs' variation of Tpd is described in the AC parameters section of this data sheet. The measurement taken at 1.5V.

### 66BUFF(0:2) to PCI Buffered Clock Skew

*Figure 13* shows the difference (skew) between the 3V33(0:5) outputs when the 66M clocks are connected to 66IN. This offset is described in the Group Timing Relationship and Tolerances section of this data sheet. The measurements were taken at 1.5V.

### 3V66 to PCI Un-Buffered Clock Skew

*Figure 1* shows the timing relationship between 3V66\_0 and PCI(0:2,4:8) and PCIF when configured to run in the unbuffered mode.

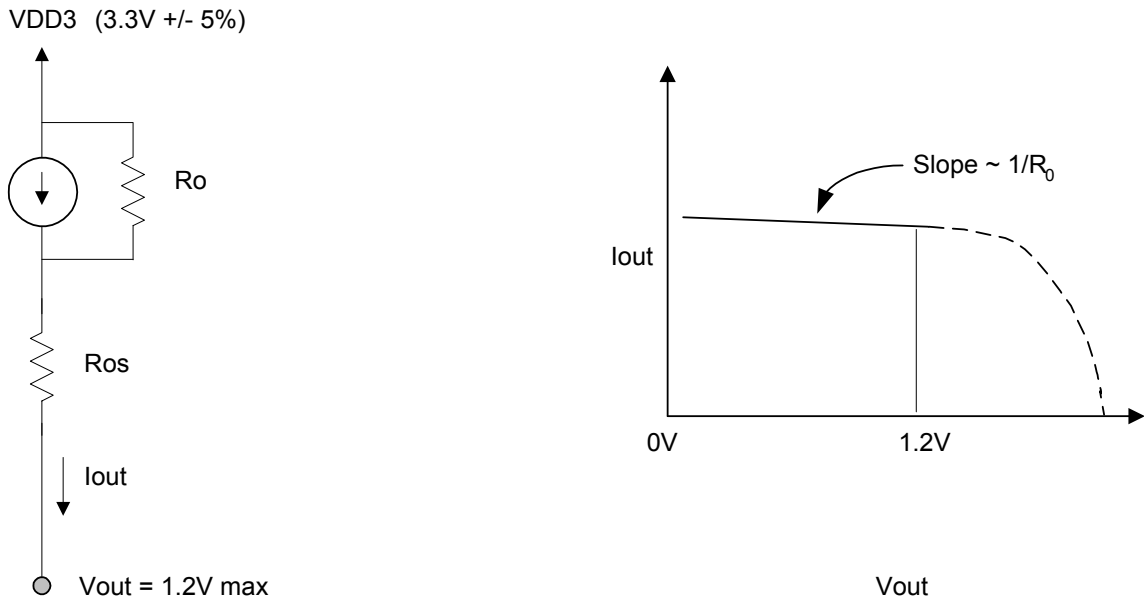

**Figure 11. USB\_48M and DOT\_48M Phase Relationship**

**Figure 12. 66IN to 66BUFF(0:2) Output Delay Figure**

**Figure 13. Buffer Mode – 3V66\_0; 66BUFF(0:2) Phase Relationship**

## Buffer Characteristics

### Current Mode CPU Clock Buffer Characteristics

The current mode output buffer detail and current reference circuit details are contained in the previous table of this data sheet. The following parameters are used to specify output buffer characteristics:

1. Output impedance of the current mode buffer circuit –  $R_o$  (see *Figure 14*).
2. Minimum and maximum required voltage operation range of the circuit –  $V_{op}$  (see *Figure 14*).
3. Series resistance in the buffer circuit –  $R_{os}$  (see *Figure 14*).
4. Current accuracy at given configuration into nominal test load for given configuration.



**Figure 14. Buffer Characteristics**

**Table 6. Host Clock (HCSL) Buffer Characteristics**

| Characteristic | Min.                        | Max. |
|----------------|-----------------------------|------|
| $R_o$          | 3000 $\Omega$ (recommended) | N/A  |
| $R_{os}$       |                             |      |
| $V_{out}$      | N/A                         | 1.2V |

**Table 7. Maximum Lumped Capacitive Output Loads**

| Clock         | Max Load | Units |
|---------------|----------|-------|
| PCI Clocks    | 30       | pF    |
| 3V66          | 30       | pF    |
| 66BUFF        | 30       | pF    |
| USB_48M Clock | 20       | pF    |
| DOT_48M       | 10       | pF    |
| REF Clock     | 50       | pF    |

**Absolute Maximum Conditions**

| Parameter          | Description                       | Condition                   | Min. | Max.                  | Unit  |
|--------------------|-----------------------------------|-----------------------------|------|-----------------------|-------|
| V <sub>DD</sub>    | Core Supply Voltage               |                             | -0.5 | 4.6                   | V     |
| V <sub>DD_A</sub>  | Analog Supply Voltage             |                             | -0.5 | 4.6                   | V     |
| V <sub>IN</sub>    | Input Voltage                     | Relative to V <sub>SS</sub> | -0.5 | V <sub>DD</sub> + 0.5 | VDC   |
| T <sub>S</sub>     | Temperature, Storage              | Non Functional              | -65  | 150                   | °C    |
| T <sub>A</sub>     | Temperature, Operating Ambient    | Functional                  | 0    | 70                    | °C    |
| T <sub>J</sub>     | Temperature, Junction             | Functional                  | -    | 150                   | °C    |
| ESD <sub>HBM</sub> | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015    | 2000 | -                     | Volts |
| ∅ <sub>JC</sub>    | Dissipation, Junction to Case     | Mil-Spec 883E Method 1012.1 | 45   |                       | °C/W  |
| ∅ <sub>JA</sub>    | Dissipation, Junction to Ambient  | JEDEC (JESD 51)             | 15   |                       | °C/W  |
| UL-94              | Flammability Rating               | At 1/8 in.                  | V-0  |                       |       |
| MSL                | Moisture Sensitivity Level        |                             | 1    |                       |       |

**DC Electrical Specifications**

| Parameter  | Description               | Condition                         | Min.  | Max.  | Unit |
|--|---------------------------|-----------------------------------|-------|-------|------|
| V <sub>DD_A</sub> ,<br>V <sub>DD_REF</sub> ,<br>V <sub>DD_PCI</sub> ,<br>V <sub>DD_3V66</sub> ,<br>V <sub>DD_48</sub> ,<br>V <sub>DD_CPU</sub> | 3.3 Operating Voltage     | 3.3 ± 5%                          | 3.135 | 3.465 | V    |
| I <sub>DD3.3V</sub>  | Dynamic Supply Current    | All frequencies at maximum values | -     | 280   | mA   |
| I <sub>PD3.3V</sub>  | Power Down Supply Current | PD# Asserted                      | -     |       | mA   |
| C <sub>IN</sub>  | Input Pin Capacitance     |                                   | -     | 5     | pF   |
| C <sub>OUT</sub>   | Output Pin Capacitance    |                                   | -     | 6     | pF   |
| L <sub>IN</sub>  | Pin Inductance            |                                   | -     | 7     | nH   |
| C <sub>XTAL</sub>  | Crystal Pin Capacitance   | Measured from the XIN             | 30    | 42    | pF   |

**AC Electrical Specifications**

| Parameter                       | Description                     | Condition   | Min.   | Max. | Unit |
|---------------------------------|---------------------------------|---|--------|------|------|
| <b>Crystal</b>                  |                                 |   |        |      |      |
| T <sub>DC</sub>                 | XIN Duty Cycle                  | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5   | 52.5 | %    |
| T <sub>PERIOD</sub>             | XIN period                      | When Xin is driven from an external clock source  | 69.841 | 71.0 | ns   |
| T <sub>R</sub> / T <sub>F</sub> | XIN Rise and Fall Times         | Measured between 0.3V <sub>DD</sub> and 0.7V <sub>DD</sub>  | -      | 10.0 | ns   |
| T <sub>CCJ</sub>                | XIN Cycle to Cycle Jitter       | As an average over 1μs duration   | -      | 500  | ps   |
| <b>CPU at 0.7V</b>              |                                 |   |        |      |      |
| T <sub>DC</sub>                 | CPUT and CPUC Duty Cycle        | Measured at crossing point V <sub>OX</sub>  | 45     | 55   | %    |
| T <sub>PERIOD</sub>             | 66MHz CPUT and CPUC Period      | Measured at crossing point V <sub>OX</sub>  | 14.85  | 15.3 | ns   |
| T <sub>PERIOD</sub>             | 100MHz CPUT and CPUC Period     | Measured at crossing point V <sub>OX</sub>  | 9.85   | 10.2 | ns   |
| T <sub>PERIOD</sub>             | 133MHz CPUT and CPUC Period     | Measured at crossing point V <sub>OX</sub>  | 7.35   | 7.65 | ns   |
| T <sub>PERIOD</sub>             | 200MHz CPUT and CPUC Period     | Measured at crossing point V <sub>OX</sub>  | 4.85   | 5.1  | ns   |
| T <sub>SKEW</sub>               | Any CPUT/C to CPUT/C Clock Skew | Measured at crossing point V <sub>OX</sub>  | -      | 100  | ps   |
| T <sub>CCJ</sub>                | CPUT/C Cycle to Cycle Jitter    | Measured at crossing point V <sub>OX</sub>  | -      | 150  | ps   |

**AC Electrical Specifications** (continued)

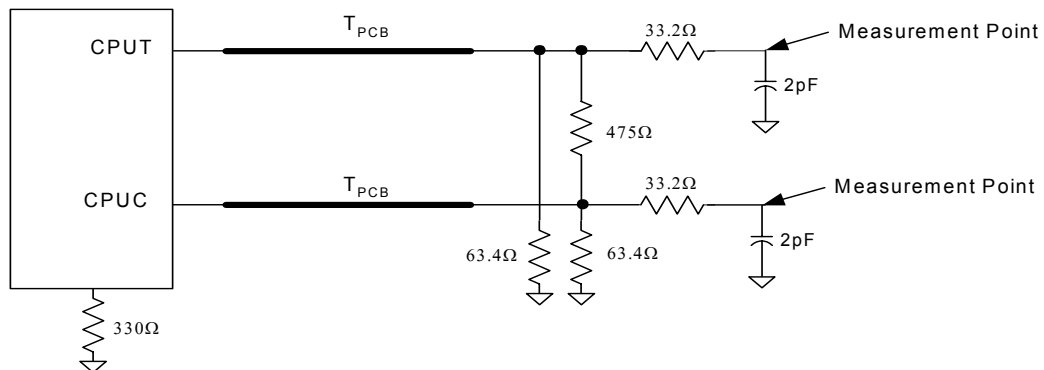
| Parameter                       | Description                                       | Condition   | Min.  | Max. | Unit |
|---------------------------------|---|---|-------|------|------|
| T <sub>R</sub> / T <sub>F</sub> | CPUT and CPUC Rise and Fall Times                 | Measured from Vol= 0.175 to Voh = 0.525V  | 175   | 700  | ps   |
| T <sub>RFM</sub>                | Rise/Fall Matching                                | Determined as a fraction of 2*(T <sub>R</sub> -T <sub>F</sub> )/(T <sub>R</sub> +T <sub>F</sub> ) | –     | 20   | %    |
| ΔT <sub>R</sub>                 | Rise Time Variation                               |   | –     | 125  | ps   |
| ΔT <sub>F</sub>                 | Fall Time Variation                               |   | –     | 125  | ps   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing              |   | 280   | 430  | mv   |
| <b>CPU at 1.0 Volts</b>         |   |   |       |      |      |
| T <sub>DC</sub>                 | CPUT and CPUC Duty Cycle                          | Measured at crossing point V <sub>OX</sub>  | 45    | 55   | %    |
| T <sub>PERIOD</sub>             | 66MHz CPUT and CPUC Period                        | Measured at crossing point V <sub>OX</sub>  | 14.85 | 15.3 | ns   |
| T <sub>PERIOD</sub>             | 100MHz CPUT and CPUC Period                       | Measured at crossing point V <sub>OX</sub>  | 9.85  | 10.2 | ns   |
| T <sub>PERIOD</sub>             | 133MHz CPUT and CPUC Period                       | Measured at crossing point V <sub>OX</sub>  | 7.35  | 7.65 | ns   |
| T <sub>PERIOD</sub>             | 200MHz CPUT and CPUC Period                       | Measured at crossing point V <sub>OX</sub>  | 4.85  | 5.1  | ns   |
| T <sub>SKEW</sub>               | Any CPUT/C to CPUT/C Clock Skew                   | Measured at crossing point V <sub>OX</sub>  | –     | 100  | ps   |
| T <sub>CCJ</sub>                | CPUT/C Cycle to Cycle Jitter                      | Measured at crossing point V <sub>OX</sub>  | –     | 150  | ps   |
| T <sub>R</sub> / T <sub>F</sub> | CPUT and CPUC Rise and Fall Times                 | Measured from Vol= 0.175 to Voh = 0.525V  | 175   | 467  | ps   |
| V <sub>OX</sub>                 | Crossing Point Voltage at 0.7V Swing              |   | 510   | 760  | mv   |
| SE_ ΔSlew                       | Absolute Single-ended Rise/Fall Waveform Symmetry |   | –     | 325  | ps   |
| <b>3V66</b>                     |   |   |       |      |      |
| T <sub>DC</sub>                 | 3V66 Duty Cycle                                   | Measurement at 1.5V   | 45    | 55   | %    |
| T <sub>PERIOD</sub>             | 3V66 Period                                       | Measured at crossing point V <sub>OX</sub>  | 15.0  | 15.3 | ns   |
| T <sub>HIGH</sub>               | 3V66 High Time                                    | Measurement at 2.4V   | 4.95  | –    | ns   |
| T <sub>LOW</sub>                | 3V66 Low Time                                     | Measurement at 0.4V   | 4.55  | –    | ns   |
| T <sub>R</sub> / T <sub>F</sub> | 3V66 Rise and Fall Times                          | Measured between 0.4V and 2.4V  | 0.5   | 2.0  | ns   |
| T <sub>SKEWUN-BUFFERED</sub>    | Any 3V66 to Any 3V66 Clock Skew                   | Measurement at 1.5V   | –     | 500  | ps   |
| T <sub>SKEW-BUFFERED</sub>      | Any 3V66 to Any 3V66 Clock Skew                   | Measurement at 1.5V   | –     | 250  | ps   |
| T <sub>CCJ</sub>                | 3V66 Cycle to Cycle Jitter                        | Measurement at 1.5V   | –     | 250  | ps   |
| <b>66BUFF</b>                   |   |   |       |      |      |
| T <sub>DC</sub>                 | 66BUFF Duty Cycle                                 | Measurement at 1.5V   | 45    | 55   | %    |
| T <sub>R</sub> / T <sub>F</sub> | 66BUFF Rise and Fall Times                        | Measured between 0.4V and 2.4V  | 0.5   | 2.0  | ns   |
| T <sub>SKEW</sub>               | Any 66BUFF to Any 66BUFF Skew                     | Measurement at 1.5V   | –     | 175  | ps   |
| T <sub>CCJ</sub>                | 66BUFF Cycle to Cycle Jitter                      | Measurement at 1.5V   | –     | 100  | ps   |
| T <sub>PD</sub>                 | 66IN to 66BUFF(Propagation Delay)                 | Measurement at 1.5V   | 2.5   | 4.5  | ns   |
| <b>PCI /PCIF</b>                |   |   |       |      |      |
| T <sub>DC</sub>                 | PCI /PCIF Duty Cycle                              | Measurement at 1.5V   | 45    | 55   | %    |
| T <sub>PERIOD</sub>             | PCI /PCIF Period                                  | Measured at crossing point V <sub>OX</sub>  | 30    | –    | ns   |
| T <sub>HIGH</sub>               | PCI and PCIF high time                            | Measurement at 2.4V   | 12.0  | –    | nS   |
| T <sub>LOW</sub>                | PCI and PCIF low time                             | Measurement at 0.4V   | 12.0  | –    | nS   |
| T <sub>R</sub> / T <sub>F</sub> | PCI and PCIF rise and fall times                  | Measured between 0.4V and 2.4V  | 0.5   | 2.0  | nS   |
| T <sub>SKEW</sub>               | Any PCI clock to Any PCI clock Skew               | Measurement at 1.5V   | –     | 500  | pS   |

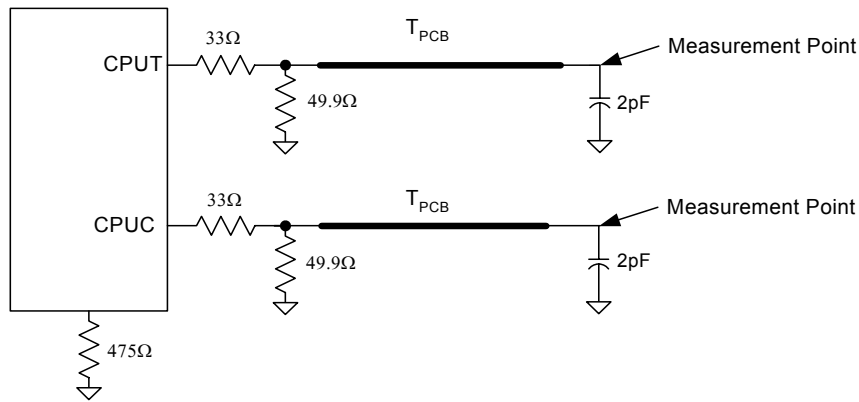
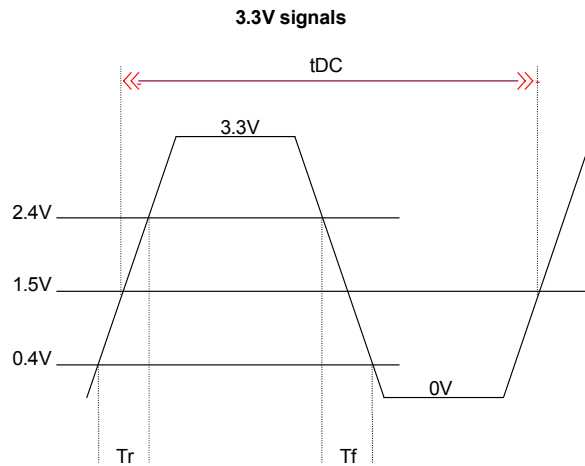
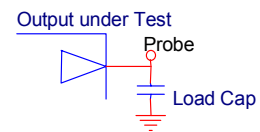
**AC Electrical Specifications** (continued)

| Parameter                       | Description                        | Condition  | Min.   | Max.   | Unit |
|---------------------------------|------------------------------------|--|--------|--------|------|
| $T_{CCJ}$                       | PCIF and PCI Cycle to Cycle Jitter | Measurement at 1.5V  | –      | 250    | ps   |
| <b>DOT_48M</b>                  |                                    |  |        |        |      |
| $T_{DC}$                        | DOT_48M Duty Cycle                 | Measurement at 1.5V  | 45     | 55     | %    |
| $T_{PERIOD}$                    | DOT_48M Period                     | Measurement at 1.5V  | 20.83  | 20.83  | ns   |
| $T_R / T_F$                     | DOT_48M Rise and Fall Times        | Measured between 0.4V and 2.4V   | 0.5    | 1.0    | ns   |
| $T_{CCJ}$                       | DOT_48M Cycle to Cycle Jitter      | Measurement at 1.5V  | –      | 350    | ps   |
| <b>USB_48M</b>                  |                                    |  |        |        |      |
| $T_{DC}$                        | USB_48M Duty Cycle                 | Measurement at 1.5V  | 45     | 55     | %    |
| $T_{PERIOD}$                    | USB_48M Period                     | Measurement at 1.5V  | 20.82  | 20.83  | ns   |
| $T_R / T_F$                     | USB_48M Rise and Fall Times        | Measured between 0.4V and 2.4V   | 1.0    | 2.0    | ns   |
| $T_{CCJ}$                       | DOT_48M Cycle to Cycle Jitter      | Measurement at 1.5V  | –      | 350    | ps   |
| <b>REF</b>                      |                                    |  |        |        |      |
| $T_{DC}$                        | REF Duty Cycle                     | Measurement at 1.5V  | 45     | 55     | %    |
| $T_{PERIOD}$                    | REF Period                         | Measurement at 1.5V  | 69.827 | 69.855 | ns   |
| $T_R / T_F$                     | REF Rise and Fall Times            | Measured between 0.4V and 2.4V   | 1.0    | 4.0    | V/ns |
| $T_{CCJ}$                       | REF Cycle to Cycle Jitter          | Measurement at 1.5V  | –      | 1000   | ps   |
| <b>ENABLE/DISABLE and SETUP</b> |                                    |  |        |        |      |
| $T_{PZL}/T_{PZH}$               | Output Enable Delay (All Outputs)  | When XIN is driven from external clock source  | 1.0    | 10.0   | ns   |
| $T_{PZL}/T_{PZH}$               | Output Disable Delay (All Outputs) |  | 1.0    | 10.0   | ns   |
| $T_{STABLE}$                    | Clock Stabilization from Power-up  |  | –      | 3.0    | ms   |
| $T_{SS}$                        | Stopclock Set Up Time              | CPU_STOP# and PIC_STOP# set up time with respect to PCIF clock to guarantee that the effected clock will stop or start at the next PCIF clock's rising edge. | 10.0   | –      | ns   |
| $T_{SH}$                        | Stopclock Hold Time                |  | 0      | –      | ns   |
| $T_{SU}$                        | Oscillator Start-up time           | When crystal meets min. 40Ω device series resistance specification   |        |        |      |

**Test and Measurement Set-up**
**For Differential CPU Output Signals**

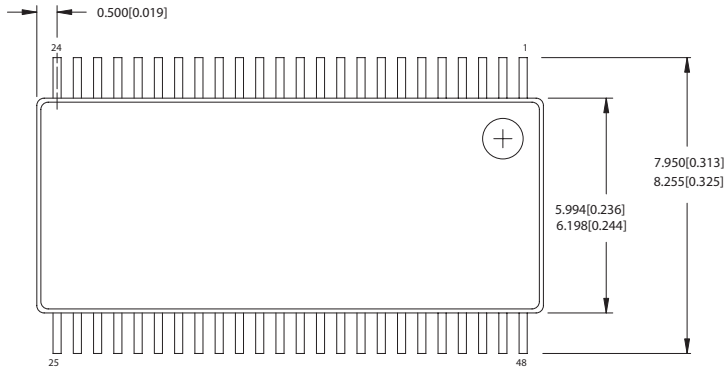
The following diagram shows lumped test load configurations for the differential Host Clock Outputs.


**Figure 15. 1.0V Test Load Termination**


**Figure 16. 0.7V Test Load Termination**

**Figure 17. For Single-ended Output Signals**
**Ordering Information**

| Part Number | Package Type                 | Product Flow           |
|-------------|------------------------------|------------------------|
| CY28339ZC   | 48-pin TSSOP                 | Commercial, 0° to 70°C |
| CY28339ZCT  | 48-pin TSSOP – Tape and Reel | Commercial, 0° to 70°C |
| Lead Free   |                              |                        |
| CY28339ZXC  | 48-pin TSSOP                 | Commercial, 0° to 70°C |
| CY28339ZCXT | 48-pin TSSOP – Tape and Reel | Commercial, 0° to 70°C |



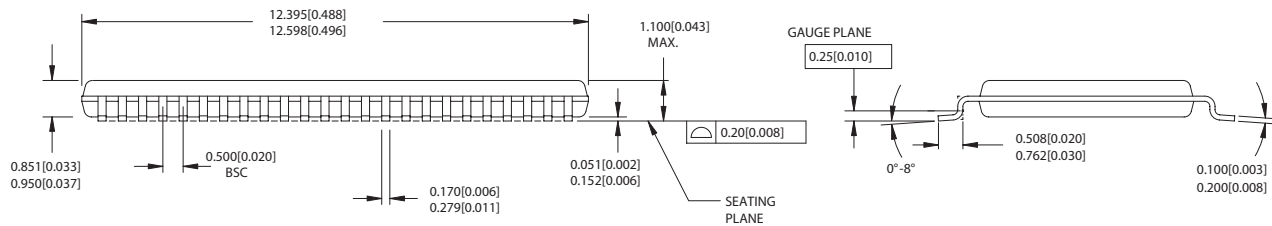
**Package Drawing and Dimensions**
**48-lead (240-mil) TSSOP II Z4824**


DIMENSIONS IN MM [INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.33gms

| PART # |                |
|--------|----------------|
| Z4824  | STANDARD PKG.  |
| ZZ4824 | LEAD FREE PKG. |



51-85059-°C

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**Document History Page**

| <b>Document Title: CY28339 Intel® CK408 Mobile Clock Synthesizer</b><br><b>Document Number: 38-07507</b> |                |                   |                        |                              |
|--|----------------|-------------------|------------------------|------------------------------|
| <b>REV.</b>  | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b> |
| **   | 122362         | 12/13/02          | RGL                    | New Data Sheet               |
| *A   | 237868         | See ECN           | RGL                    | Added Lead Free Devices      |