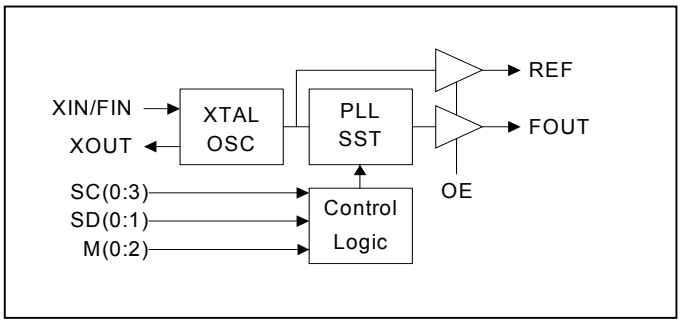
PLL701-50

Low EMI Spread Spectrum Multiplier IC

FEATURES

- Spread Spectrum Clock Generator/Multiplier with output selectable from 1x to 8x.
- 13MHz to 224MHz output with output enable.
- 13MHz to 30 MHz input frequency from crystal or external clock signal.
- Reduced EMI from Spread Spectrum Modulation, with selectable modulation magnitude for Center Spread, Down Spread or Asymmetric Spread.
- TTL/CMOS compatible outputs.
- 3.3V Operating Voltage.
- 150 ps maximum cycle-to-cycle jitter.
- Available in 16-Pin 150mil SSOP.

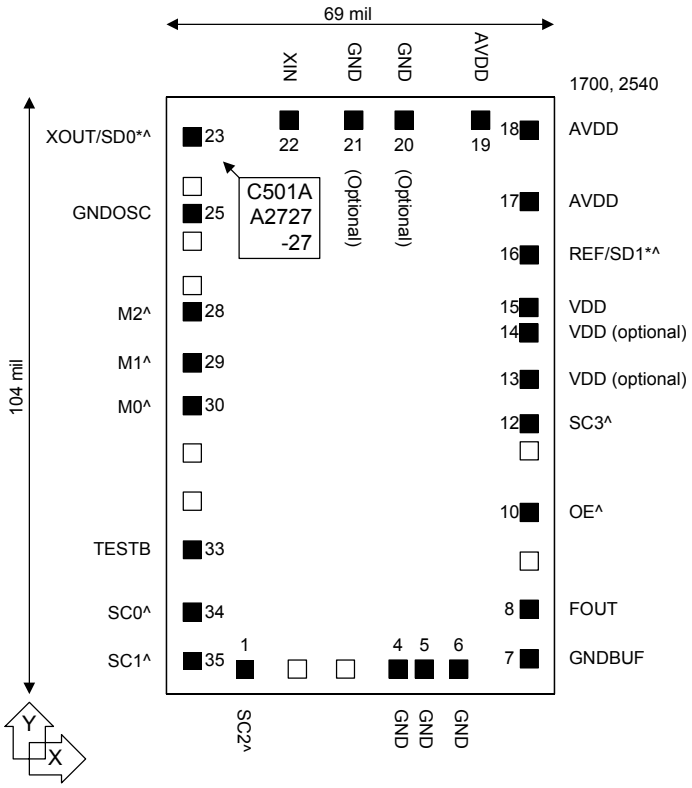
BLOCK DIAGRAM



DESCRIPTION

The PLL701-50 is a low EMI Clock Generator and Multiplier for high-speed digital systems. It uses PhaseLink's unique (Patent Pending) Spread Spectrum Technology (SST) and permits different levels of EMI reduction by selecting the amplitude of the applied SST. The SST feature can be disabled. The chip operates with input frequencies ranging from 13 to 30 MHz and provides 1x to 8x multiplication at its output.

DIE PAD CONFIGURATION



OUTPUT CLOCK (FOUT) SELECTION

M2	M1	M0	FIN/XIN (MHz)	Multiplier	FOUT (MHz)
0	0	0	13 ~ 28	X1	13 ~ 28
0	0	1	13 ~ 28	X2	26 ~ 56
0	1	0	14 ~ 30	X3	42 ~ 90
0	1	1	13 ~ 28	X4	52 ~ 112
1	0	0	20 ~ 30	X5	100 ~ 150
1	0	1	17 ~ 30	X6	102 ~ 180
1	1	0	15 ~ 30	X7	105 ~ 210
1	1	1	13 ~ 28	X8	104 ~ 224

DIE SPECIFICATIONS

Name	Value
Size	104 x 69 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

SPREAD SPECTRUM SELECTION TABLE

SD1	SD0	SC3	SC2	SC1	SC0	Modulation Magnitude	Modulation Frequency	Modulation Type	
1	1	0	0	0	0	0.250%	Fin / 512	C	± 0.125%
1	1	0	0	0	1	0.500%		C	± 0.25%
1	1	0	0	1	0	0.750%		C	± 0.375%
1	1	0	1	0	0	1.250%		C	± 0.625%
1	0	0	1	0	0			A	+0.125 ~ -1.125%
1	1	0	1	0	1	1.500%		C	± 0.75%
1	0	0	1	0	1			A	+0.25 ~ -1.25%
1	1	0	1	1	0	1.750%		C	± 0.875%
1	0	0	1	1	0			A	+0.375 ~ -1.375%
1	1	0	1	1	1	2.000%		C	± 1.00%
1	0	0	1	1	1			A	+0.50 ~ -1.5%
0	1	0	1	1	1			D	-2.00%
1	1	1	0	0	0	2.250%		C	± 1.125%
1	0	1	0	0	0			A	+0.625 ~ -1.625%
0	1	1	0	0	0			A	+0.125 ~ -2.125%
1	1	1	0	0	1	2.500%		C	± 1.25%
0	1	1	0	0	1			A	+0.25 ~ -2.25%
1	0	1	0	0	1			A	+0.75 ~ -1.75%
1	1	1	0	1	0	2.750%		C	± 1.375%
1	0	1	0	1	0			A	+0.875 ~ -1.875%
0	1	1	0	1	0			A	+0.375 ~ -2.375%
1	1	1	0	1	1	3.000%		C	± 1.50%
0	0	1	0	1	1			D	-3.00%
1	0	1	0	1	1			A	+1.00 ~ -2.00%
0	1	1	0	1	1			A	+0.50 ~ -2.50%
1	1	1	1	0	0	3.250%		C	± 1.625%
1	0	1	1	0	0			A	+1.125 ~ -2.125%
0	1	1	1	0	0			A	+0.625 ~ -2.625%
0	0	1	1	0	0			A	+0.125 ~ -3.125%
1	1	1	1	0	1	3.500%		C	± 1.75%
1	0	1	1	0	1			A	+1.25 ~ -2.25%
0	1	1	1	0	1			A	+0.75 ~ -2.75%
0	0	1	1	0	1			A	+0.25 ~ -3.25%
1	1	1	1	1	0	3.750%		C	± 1.875%
1	0	1	1	1	0			A	+1.37 ~ -2.375%
0	1	1	1	1	0			A	+0.875 ~ -2.875%
0	0	1	1	1	0			A	+0.375 ~ -3.375%
1	1	1	1	1	1	0.00 %			SST turned off
1	0	1	1	1	1				SST turned off
0	1	1	1	1	1				SST turned off
0	0	1	1	1	1				SST turned off

Notes: C: Center Spread. A: Asymmetric Spread. D: Down Spread.

FUNCTIONAL DESCRIPTION

Selectable spread spectrum and modulation magnitude

The PLL701-50 provides selectable multiplier factors (1x to 8X), selectable spread spectrum modulation type, as well as selectable modulation magnitude. Selection is made by connecting specific input pins to a logical "zero" or "one". Pins 6 (SC0), 7 (SC1), 8 (SC2) and 12 (SC3) are used as inputs to select the spread spectrum modulation magnitude as shown on the spread spectrum selection table (page 2). Pins 3 (M2), 4 (M1), 5 (M0) are used as inputs to select the multiplication factor as shown on the output clock selection table (page 1). Pin 11 is the output enable pin, which tri-states all outputs when low (logical "zero").

In order to reduce the number of pins on the chip, the PLL701-50 uses pins 2 and 14 (XOUT/SD0 and REF/SD1) as bi-directional pins. The pins serve as modulation type selector inputs (SD0 and SD1) upon power-up (see spread spectrum selection table on page 2), and as XOUT crystal connection (pin 2), and REF output signal (pin 14) as soon as the inputs have been latched.

Connecting a selection pin to a logical "one"

All selection pins have an internal pull-up resistor (30kΩ for pins 3, 4, 5, 6, 7, 8, 11, 12, 14 and 120kΩ for pin 2). This internal pull-up resistor will pull the input value to a logical "one" (pull-up) by default, i.e. when no resistive load is connected between the pin and GND. No external pull-up resistor is therefore required for connecting a logical "one" upon power-up.

Connecting a selection pin to a logical "zero"

For an input only pin, i.e. all input pins except XOUT/SD0 (pin 2) and REF/SD1 (pin 14), the pin simply needs to be grounded to pull the input down to a logical "zero". For the Bidirectional pins (pins 2 and 14) you will need an external resistor. For pin 2 a 27kΩ resistor is recommended and for pin 14 a 4.7kΩ resistor is recommended.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. DC/AC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		2.97		3.63	V
Input High Voltage	V_{IH}		0.7* V_{DD}			V
Input Low Voltage	V_{IL}				0.3* V_{DD}	V
Input High Current	I_{IH}				100	µA
Input Low Current	I_{IL}				100	µA
Output High Voltage	V_{OH}	I_{OH}=5mA, V_{DD} =3.3V	2.4			
Output Low Voltage	V_{OL}	I_{OL}=6mA, V_{DD} =3.3V			0.4	
Input Frequency	F_{XIN}	When using a crystal	See Output Clock Selection table on page 1			MHz
	F_{IN}	When using reference clock	See Output Clock Selection table on page 1			MHz
Maximum interruption of F_{IN}		When using reference clock			100	µs
Load Capacitance	C_L	Between Pin XIN and XOUT*		18		pF
Pull-up Resistor	R_{up}	PIN 2		120		kΩ
Pull-up Resistor	R_{up}	PIN 3,4,5,6,7,8,11,12,14		30		kΩ
Short Circuit Current	I_{sc}			50		mA
3.3V Dynamic Supply Current	I_{CC}	No Load		20		mA

***Note:** Pin XIN and XOUT each has a 36pF capacitance. When used with a XTAL, the two capacitors combined load the crystal with 18pF. If driving XIN with a reference clock signal, the load capacitance will be 36pF (typical).

3. Timing Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Rise Time	T_r	Measured at 0.8V ~ 2.0V @ 3.3V	0.8	0.95	1.1	ns
Fall Time	T_f	Measured at 2.0V ~ 0.8V @ 3.3V	0.78	0.85	0.9	ns
Output Duty Cycle	D_T		45	50	55	%
Cycle to Cycle Jitter	$T_{cyc-cyc}$	X1, X2, X4, X8 FOUT @ 3.3V			100	ps
Cycle to Cycle Jitter	$T_{cyc-cyc}$	X3, X5, X6, X7 FOUT @ 3.3V			150	ps

PAD ASSIGNMENT (LOWER LEFT CORNER: X = 0, Y = 0)

Pad #	Name	X (μm)	Y (μm)	Description
1	SC2	338.9	104.7	Digital control input to select SS modulation magnitude.30kΩ internal pull-up.
2	N/C	569	104.7	
3	N/C	780.5	104.7	
4	GND	1027.6	104.7	Ground.
5	GND	1127.3	104.7	Ground.
6	GND	1284.5	104.7	Ground.
7	GNDBUF	1595.1	139.7	Ground, Buffer Circuitry
8	FOUT	1595.1	381.7	Modulated Clock Frequency Output. The input frequency is multiplied per M(0:2), modulation type is selected per SD(0:1) and modulation rate is selected per SC(0:3).
9	N/C	1595.1	596.3	
10	OE	1595.1	811.9	Output Enable. When low, Tri-states all outputs. 30kΩ internal pull-up.
11	N/C	1595.1	970.3	
12	SC3	1595.1	1069.3	Digital control input to select SS modulation magnitude.30kΩ internal pull-up.
13	VDD (Optional)	1595.1	1312.3	3.3V power supply, Optional
14	VDD (Optional)	1595.1	1555.6	3.3V power supply, Optional
15	VDD	1595.1	1656.8	3.3V power supply.
16	REF/SD1	1595.1	1879.9	At power-up, this pin acts as input pin to select the modulation type and is latched in. After the input sampling, this pin provides a buffered Reference Clock Output of the same frequency as the crystal or clock input. 30kΩ internal pull-up.
17	AVDD	1595.1	2093	3.3V Analog power supply.
18	AVDD	1595.1	2390.6	3.3V Analog power supply.
19	AVDD	1369.2	2435	3.3V Analog power supply.
20	GND (Optional)	1037.3	2435	Ground, Optional
21	GND (Optional)	824.7	2435	Ground, Optional
22	XIN	529.7	2435	Crystal input to be connected to fundamental parallel mode crystal. (C_L=18pF) or clock input.
23	XOUT/SD0	105.6	2343.5	At power-up, this pin is acts as input pin to select the modulation type. After the input sampling, it is used as crystal output connector. 120kΩ internal pull up resistor.
24	N/C	105.6	2136.1	
25	GNDOSC	105.6	2035.6	Ground, Oscillator Circuitry
26	N/C	105.6	1934.9	
27	N/C	105.6	1741.5	
28	M2	105.6	1641.4	Digital control input to select multiplier. 30kΩ internal pull-up.
29	M1	105.6	1396.2	Digital control input to select multiplier. 30kΩ internal pull-up.
30	M0	105.6	1180.3	Digital control input to select multiplier. 30kΩ internal pull-up.
31	N/C	105.6	993.5	
32	N/C	105.6	836.7	
33	TESTB	105.6	680.1	Disables multiplication and SST when pulled low. For crystal fine tuning. Internal pull up.
34	SC0	105.6	354.9	Digital control input to select SS modulation magnitude.30kΩ internal pull-up.
35	SC1	105.6	110.7	Digital control input to select SS modulation magnitude.30kΩ internal pull-up.

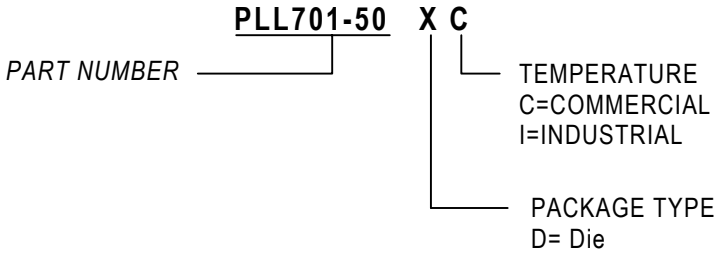
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PLL701-50DC	P701-50DC	Die –Waffle Pack