

PIN CONFIGURATION

FEATURES

Spread Spectrum Clock Generator with selectable multiplier from 1x to 4x outputs.

- Output frequency ranges: 24MHz to 240MHz.
- Selectable Down Spread Modulation.
- TTL/CMOS compatible outputs.
- 3.3V Operating Voltage.
- Low short term jitter.
- Available in 8-Pin 150mil SOIC.

FIN = 24 ~ 120 Mhz

Note: v: $30k\Omega$ Internal Pull down ^: $30k\Omega$ Internal Pull up.

DESCRIPTIONS

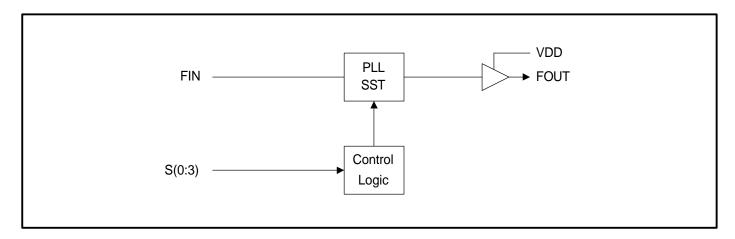
The PLL701-13 is a Spread Spectrum Clock Generator designed for the purpose of reducing EMI in high-speed digital systems. The selectable Down Spread modulation amplitude (see table below) permits EMI reduction without over-clocking the output. Any output frequency can be selected by programming 4 multiplier modes. The device operates over a very wide range of input frequencies and provides 1x to 4x modulated clock outputs.

OUTPUT CLOCK (FOUT) SELECTION

S 3	S2	S2 S1	S0	FIN Range	FOUT	Spread Spectrum Modulation		
33	33 32		30	(MHz)	1001	Frequency	Magnitude	
0	0	0	0	24 - 60	X1		-1.5%	
0	0	0	1	24 - 60	X1		-2.0%	
0	0	1	0	24 - 60	X1		-2.5%	
0	0	1	1	24 - 60	X1		-3.0%	
0	1	0	0	24 - 60	X2		-0.5%	
0	1	0	1	24 - 60	X2	Fin / 256	-1.0%	
0	1	1	0	24 - 60	X2		-1.5%	
0	1	1	1	24 - 60	X2		-2.0%	
1	0	0	0	24 - 60	X2		-2.5%	
1	0	0	1	24 - 60	X2		-3.0%	
1	0	1	0	24 - 60	X4		-0.5%	
1	0	1	1	24 - 60	X4		-1.0%	
1	1	0	0	60 - 120	X1		-0.5%	
1	1	0	1	60 - 120	X1		-1.0%	
1	1	1	0	60 - 120	X1		-1.5%	
1	1	1	1	60 - 120	X1		-2.0%	



BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Туре	Description
FIN	1	I	Input Clock Frequency.
S2	2	I	Digital control input to select output frequency and SST modulation amplitude. Has internal pull-up.
S1	3	I	Digital control input to select output frequency and SST modulation amplitude. Has internal pull-up.
S0	4	I	Digital control input to select output frequency and SST modulation amplitude. Has internal pull-down.
S3	7	I	Digital control input to select output frequency and SST modulation amplitude. Has internal pull-down.
VDD	8	Р	3.3V Power Supply.
FOUT	6	0	SST Modulated Clock Frequency Output. The frequency before modulation is synthesized by multiplying the input frequency by 1X, 2X, or 4X, depending on S(0:3).
GND	5	Р	Ground.



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V _{SS} -0.5	6	V
Input Voltage Range	VI	V _{SS} -0.5	V _{DD} +0.5	V
Output Voltage Range	Vo	Vss-0.5	V _{DD} +0.5	V
Soldering Temperature			260	°C
Storage Temperature	Ts	-65	150	°C
Ambient Operating Temperature*	ТА	-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC/AC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		3.15		3.45	V
Input High Voltage	VIH		0.7*VDD			V
Input Low Voltage	VIL				0.3*VDD	V
Input High Current	Іін				100	μΑ
Input Low Current	lıL				100	μΑ
Output High Voltage	Vон	I _{OH} =5mA, VDD=3.3V	2.4			
Output Low Voltage	Vol	I _{OL} =6mA, VDD=3.3V			0.4	
Input Frequency	Fin		24		120	MHz
Maximum interruption of F _{IN}					none	μs
Input Capacitance	Cin1			4		pF
Pull-up Resistor	Rpu	PIN 2, 3		30		kΩ
Pull-down Resistor	R_{pd}	PIN 4, 7		30		kΩ
Short Circuit Current	I _{sc}			25		mA
3.3V Dynamic Supply Current	Icc	No Load		20		mA

^{*} Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.



3. TIMING CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Rise Time	Tr	Measured at 0.8V ~ 2.0V @ 3.3V	0.8	0.95	1.1	ns
Fall Time	T_f	Measured at 2.0V ~ 0.8V @ 3.3V	0.78	0.85	0.9	ns
Output Duty Cycle	DT		45	50	55	%
Input to Output Delay			2		4	ns
Cycle to Cycle Jitter	Тсус-сус	Over output frequency range @ 3.3V			100	ps

FUNCTIONAL DESCRIPTION

Selectable spread spectrum and modulation rates

The PLL701-13 provides selectable spread spectrum modulation, as well as selectable modulation rate. Selection is made by connecting specific pins to a logical "zero" or "one", according to the output clock selection table and modulation rate selection table on page 1.

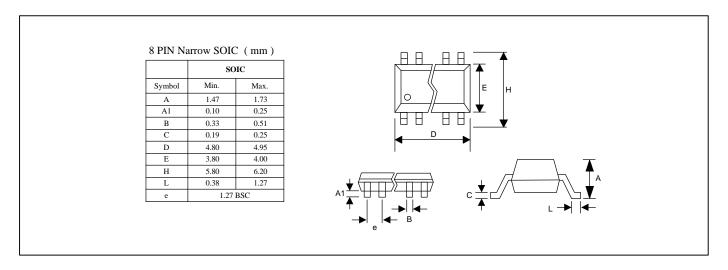
Pins 2 (S2), 3 (S1), 4 (S0), and 7 (S3) are used as inputs to select the spread spectrum modulation as shown on the output clock selection table (page 1).

Default values for S(0:3) through internal pull-up and pull-down resistor

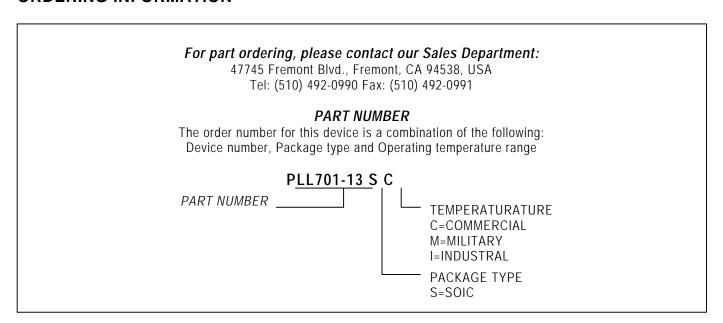
Selection pins S0 and S3 have an internal pull-down resistor of $30k\Omega$, pins 2 and 3 (S1 and S2) have an internal pull-up resistor of $30k\Omega$. This internal pull-up (or pull-down) resistor will pull the input value to a logical "one" (or "zero" respectively) by default, i.e. when no resistive load is connected between the pin and GND (VDD respectively). In order to override the internal pull-up (pull-down), the pin has to be connected to GND (VDD respectively).



PACKAGE INFORMATION



ORDERING INFORMATION



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