



N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package
			Die†
40V	3.0Ω	2.0A	VN1504NW
60V	3.0Ω	2.0A	VN1506NW
90V	3.0Ω	2.0A	VN1509NW

† MIL visual screening available.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Advanced DMOS Technology

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

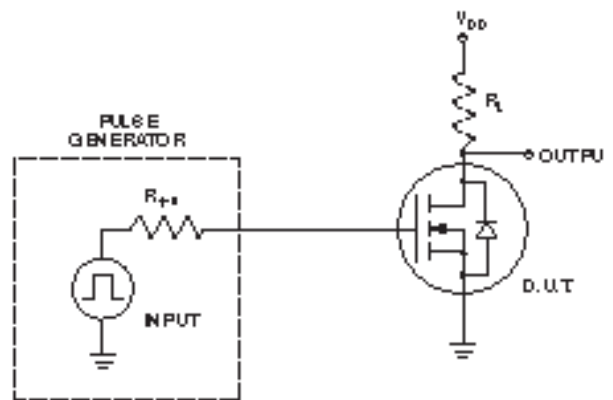
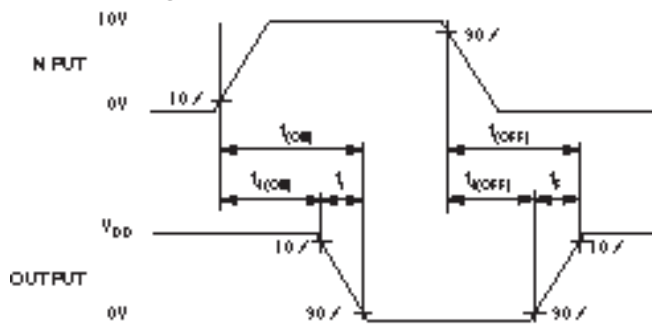
Electrical Characteristics (@25°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1504 VN1506 VN1509	40 60 90			V	$V_{GS} = 0V, I_D = 1mA$
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}, I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}, I_D = 1mA$
I_{GSS}	Gate Body Leakage				100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				1	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
					100		$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ C$
$I_{D(ON)}$	ON-State Drain Current		0.5	1.0		A	$V_{GS} = 5V, V_{DS} = 25V$
			2.0	2.5			$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			3.0	5.0	Ω	$V_{GS} = 5V, I_D = 250mA$
				2.5	3.0		$V_{GS} = 10V, I_D = 1A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.70	1	%/°C	$V_{GS} = 10V, I_D = 1A$
G_{FS}	Forward Transconductance		300	450		mS	$V_{DS} = 25V, I_D = 0.5A$
C_{ISS}	Input Capacitance			55	65	pF	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			20	25		
C_{RSS}	Reverse Transfer Capacitance			5	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD} = 25V$ $I_D = 1A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$V_{GS} = 0V, I_{SD} = 1.0A$
t_{rr}	Reverse Recovery Time			400		ns	$V_{GS} = 0V, I_{SD} = 1.0A$

Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



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