CY25819

Spread Spectrum Clock Generator

Features

- 8- to 32-MHz input frequency range
- CY25819: 16 MHz to 32 MHz
- Separate modulated and unmodulated clocks
- Accepts clock, crystal, and resonator inputs
- Down spread modulation
- Power-down function
- Low-power dissipation
  - CY25819 = 36 mW typ at 16 MHz
  - CY25819 = 63 mW typ at 32 MHz
- Low cycle-to-cycle jitter
  - SSCLK = 250 ps typ
  - REFOUT = 275 ps typ
- Available in 8-pin (150 mil) SOIC package

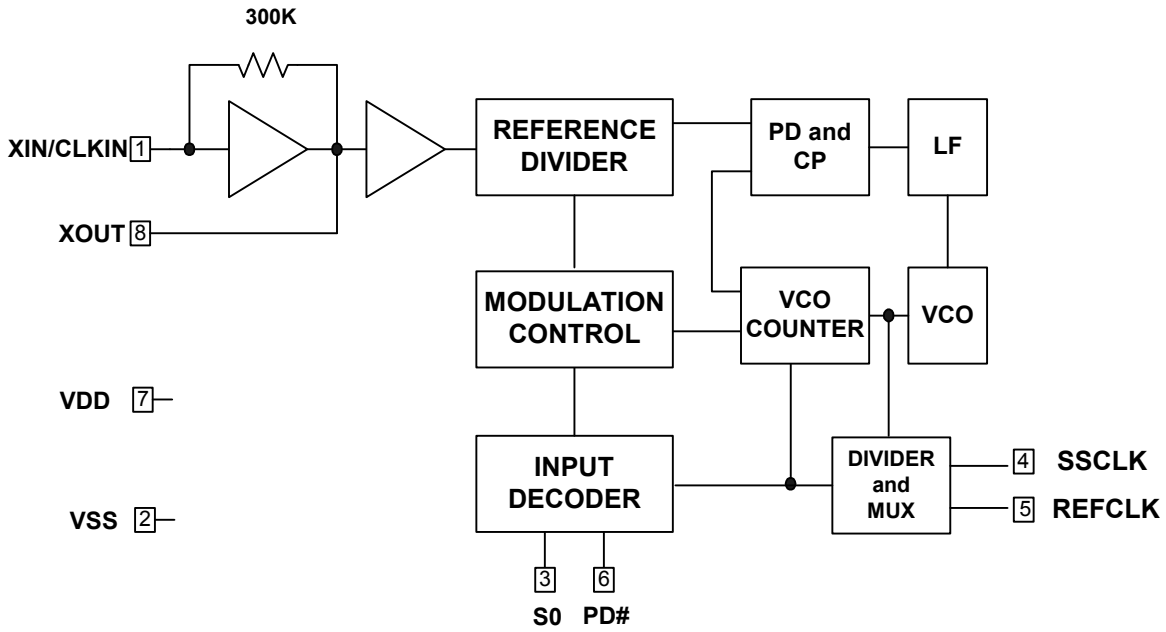
Applications

- Printers and MFPs
- LCD panels and notebook PCs
- Digital copiers
- PDAs
- Automotive
- CD-ROM, VCD, and DVD
- Networking and LAN/WAN
- Scanners
- Modems
- Embedded digital systems

Benefits

- Peak electromagnetic interference (EMI) reduction by 8 dB to 16 dB
- Fast time to market
- Cost reduction

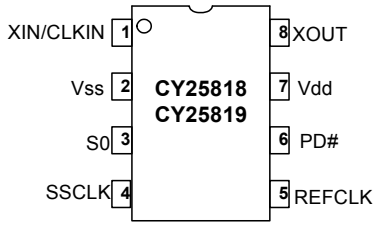
Block Diagram



Contents

Pin Configuration

8-pin SOIC



Pin Description

Pin	Name	Description
1	XIN/CLK	Clock, Crystal, or Ceramic Resonator Input Pin.
2	Vss	Power Supply Ground.
3	S0	**Digital Spread% Control Pin. 3-Level input (H-M-L).** Default = M.
4	SSCLK	**Modulated Spread Spectrum Output Clock.** The output frequency is referenced to input frequency. Refer to Table 2 on page 4 for the amount of modulation (Spread%).
5	REFCLK	**Unmodulated Reference Clock Output.** The unmodulated output frequency is the same as the input frequency.
6	PD#	**Power Down Control Pin.** Default = H (Vdd).
7	Vdd	Positive Power Supply.
8	XOUT	**Clock, Crystal, or Ceramic Resonator Output Pin.** Leave this pin unconnected if an external clock is used at X_{IN} pin.

Overview

The Cypress CY25819 products are Spread Spectrum Clock Generator (SSCG) ICs used for the purpose of reducing EMI found in today's high-speed digital electronic systems. The devices use a Cypress proprietary phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time to market without degrading system performance.

The input frequency range is 8–16 MHz for the CY25818 and 16–32 MHz for the CY25819. Both products accept external clock, crystal, or ceramic resonator inputs.

The CY25819 provide separate modulated (SSCLK) and unmodulated reference (REFCLK) clock outputs which are the same frequency as the input clock frequency. Down spread frequency modulation can be selected by the user, based on three discrete values of Spread%. A separate power down function is also provided.

The CY25819 products are available in an 8-pin SOIC (150-mil) package with a commercial operating temperature range of 0–70 °C. Contact Cypress for availability of –40 to +85 °C industrial temperature range operation or TSSOP package versions.

Input Frequency Range and Selection

CY25819 input frequency range is 8–32 MHz. This range is divided into two segments, as given in Table 1.

Table 1. Input and Output Frequency Selection

Product	Input/Output Frequency Range
CY25819	16–32 MHz

Spread% Selection

CY25818/19 SSCG products provide Down-Spread frequency modulation. The amount of Spread% is selected by using 3-Level S0 digital input. Spread% values are given in Table 2.

Table 2. Spread% Selection

XIN (MHz)	Product	S0 = 1	S0 = 0	S0 = M
		Down (%)	Down (%)	Down (%)
16–20	CY25819	–3.0	–2.2	–0.7
20–24	CY25819	–2.7	–1.9	–0.6
24–28	CY25819	–2.5	–1.8	–0.6
28–32	CY25819	–2.3	–1.7	–0.5

3-Level Digital Inputs

S0 digital input is designed to sense three logic levels designated as HIGH “1”, LOW “0”, and MIDDLE “M”. With this 3-Level digital input logic, the 3-Level logic is able to detect three different logic levels.

The S0 pin includes an on-chip 20K (10K/10K) resistor divider. No external application resistors are needed to implement 3-Level logic, as follows.

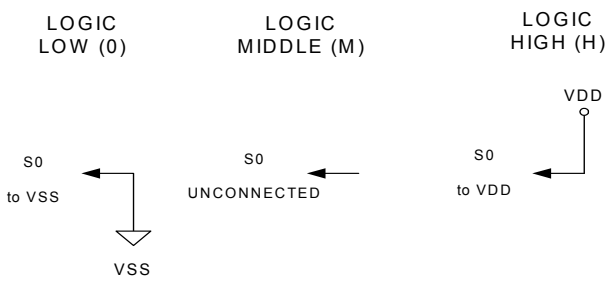
Logic Level “0”: 3-Level logic pin connected to GND.

Logic Level “M”: 3-Level logic pin left floating (no connection).

Logic Level “1”: 3-Level logic pin connected to Vdd.

Figure 1 illustrates how to implement 3-Level Logic.

Figure 1. 3-Level Logic



Modulation Rate

Spread Spectrum Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (fmax) and minimum frequency of the clock (fmin) determine this band of frequencies. The time required to transition from fmin to fmax and back to fmin is the period of the Modulation Rate, Tmod. The Modulation Rates of SSCG clocks are generally referred to in terms of frequency, and fmod = 1/Tmod.

The input clock frequency, fin, and the internal divider determine the Modulation Rate.

In the case of CY25819 devices, the (Spread Spectrum) Modulation Rate, fmod, is given by the following formula:

$fmod = f_{IN}/DR$

where fmod is the Modulation Rate, f_{IN} is the Input Frequency, and DR is the Divider Ratio, as given in Table 3.

Table 3. Modulation Rate Divider Ratios

Product	Input Frequency Range	Divider Ratio (DR)
CY25818	8–16 MHz	256
CY25819	16–32 MHz	512

Maximum Ratings[1, 2]

Supply Voltage (Vdd): ..... +5.5 V
Input Voltage Relative to Vdd: ..... Vdd + 0.3 V
Input Voltage Relative to Vss: ..... Vss + 0.3 V
Operating Temperature: ..... 0 °C to +70 °C
Storage Temperature: ..... –65 °C to +150 °C

DC Electrical Characteristics

Vdd = 3.3 V ± 10%, T_A = 0 °C to +70 °C and C_L = 15 pF (unless otherwise noted)

Parameter	Description	Conditions	Min	Typ	Max	Unit
Vdd	Power Supply Range		2.97	3.3	3.63	V
V_{INH}	Input HIGH Voltage	S0 Input	0.85 Vdd	Vdd	Vdd	V
V_{INM}	Input MIDDLE Voltage	S0 Input	0.40 Vdd	0.50 Vdd	0.60 Vdd	V
V_{INL}	Input LOW Voltage	S0 Input	0.0	0.0	0.15 Vdd	V
V_{OH1}	Output HIGH Voltage	I_{OH} = 4 mA, SSCLK and REFCLK	2.4	–	–	V
V_{OH2}	Output HIGH Voltage	I_{OH} = 6 mA, SSCLK and REFCLK	2.0	–	–	V
V_{OL1}	Output LOW Voltage	I_{OL} = 4 mA, SSCLK Output	–	–	0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 10 mA, SSCLK Output	–	–	1.2	V
C_{IN1}	Input Capacitance	X_{IN} (Pin 1) and X_{OUT} (Pin 8)	6.0	7.5	9.0	pF
C_{IN2}	Input Capacitance	All Digital Inputs	3.5	4.5	6.0	pF
I_{DD1}	Power Supply Current	F_{IN} = 8 MHz, no load	–	10.0	12.5	mA
I_{DD3}	Power Supply Current	F_{IN} = 32 MHz, no load	–	19.0	23.0	mA
I_{DD4}	Power Supply Current	PD# = Vss	–	150	250	mA

Timing Electrical Characteristics

Vdd = 3.3 V ± 10%, T_A = 0 °C to +70 °C and C_L = 15 pF (unless otherwise noted)

Parameter	Description	Conditions	Min	Typ	Max	Unit
ICLKFR1	Input Frequency Range	CY25818	8	–	16	MHz
ICLKFR2	Input Frequency Range	CY25819	16	–	32	MHz
trise1	Clock Rise Time	SSCLK and REFCLK, 0.4V to 2.4V	2.0	3.0	4.0	ns
tfall1	Clock Fall Time	SSCLK and REFCLK, 0.4V to 2.4V	2.0	3.0	4.0	ns
CDCin	Input Clock Duty Cycle	X_{IN}	20	50	80	%
CDCout	Output Clock Duty Cycle	SSCLK and REFCLK @ 1.5V	45	50	55	%
CCJss	Cycle-to-Cycle Jitter	SSCLK; F_{IN} = F_{OUT} = 8–32 MHz	–	250	350	ps
CCJref	Cycle-to-Cycle Jitter	REFCLK; F_{IN} = F_{OUT} = 8–32 MHz	–	275	375	ps

Notes
1. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Operation at any Absolute Maximum Rating is not implied.

Characteristics Curves

The following curves demonstrate the characteristic behavior of the CY25819 when tested over a number of environmental and application specific parameters. These are typical performance curves and are not meant to replace any parameter specified in DC Electrical Characteristics on page 6 and Timing Electrical Characteristics on page 6.

Figure 2. CCJ (ps) vs. Frequency (MHz)

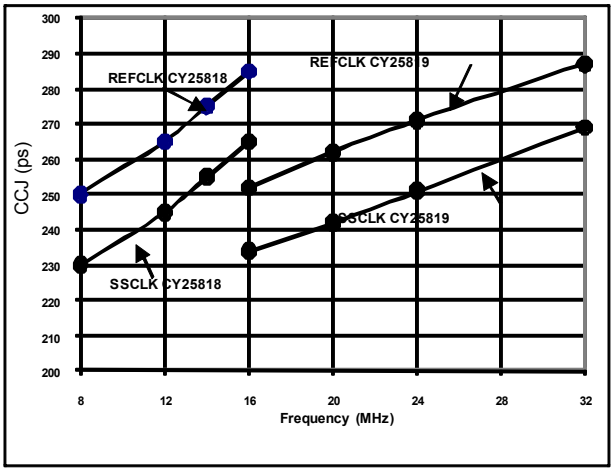


Figure 3. Bandwidth% vs. Temperature

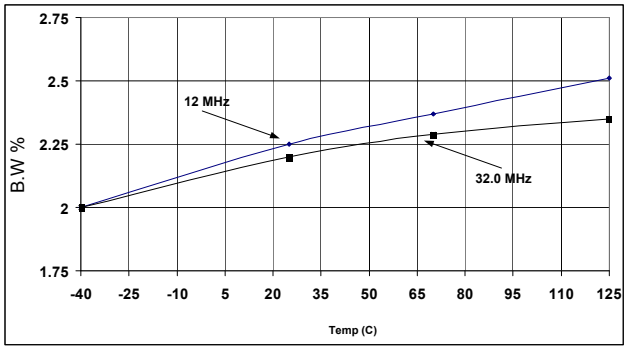


Figure 4. IDD (mA) vs. Frequency (MHz)

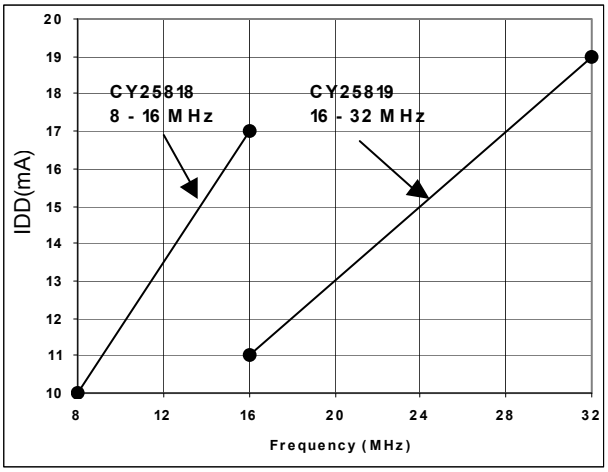
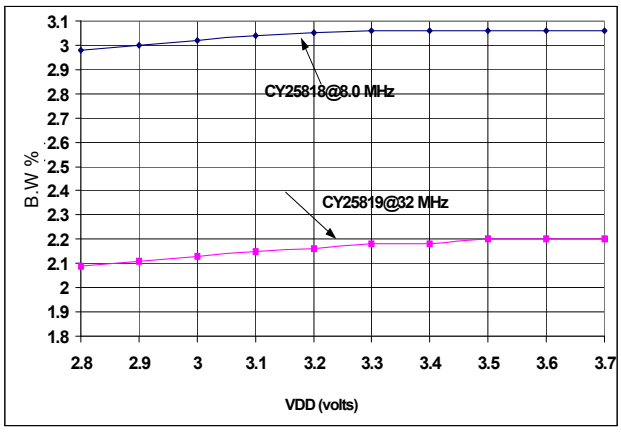


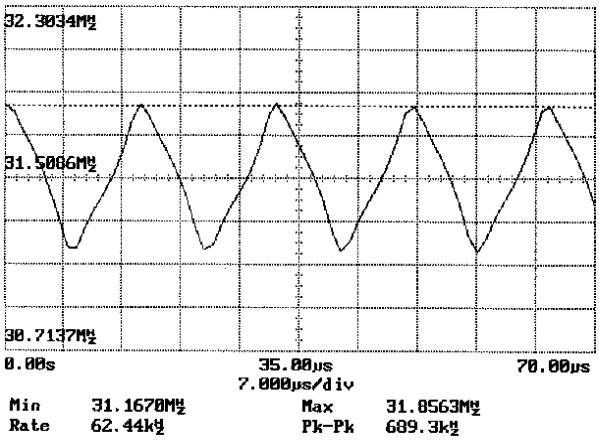
Figure 5. Bandwidth% vs. Vdd



SSCG Profiles

CY25819 SSCG products use a non-linear “optimized” frequency profile as shown in Figure 6. The use of Cypress proprietary “optimized” frequency profile maintains flat energy distribution over the fundamental and higher order harmonics. This results in additional EMI reduction in electronic systems.

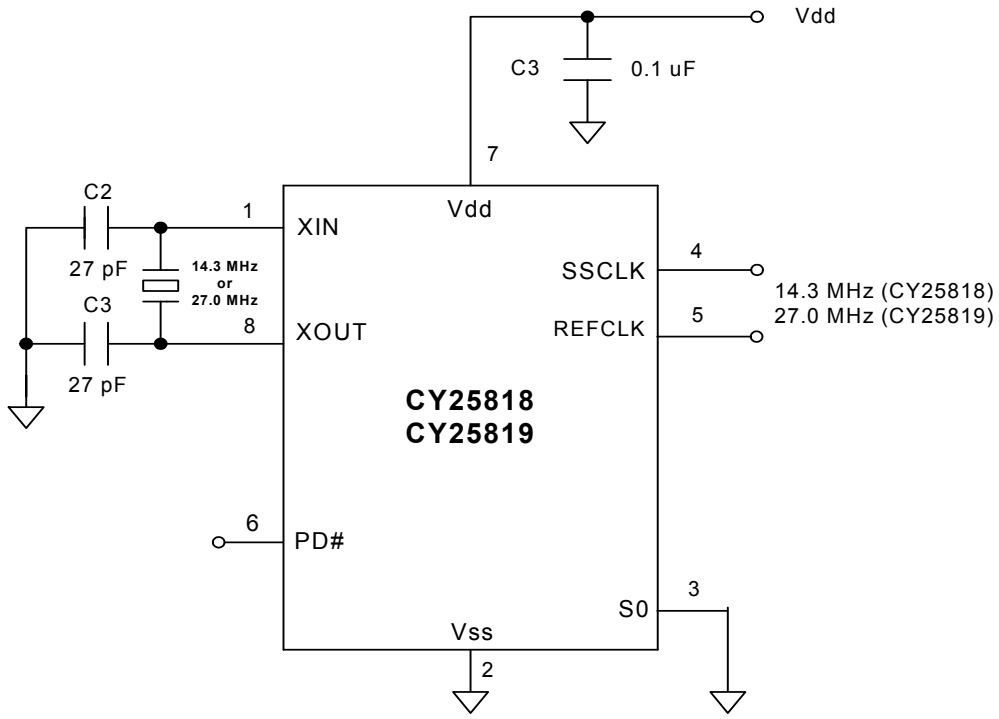
Figure 6. CY25819 Spread Spectrum Profile (Frequency vs. Time)[3]



Note
3. Xin = 32.0 MHz; S0 = 1; SSCLK = 32.0 MHz; BW = –2.15%.

Application Schematic

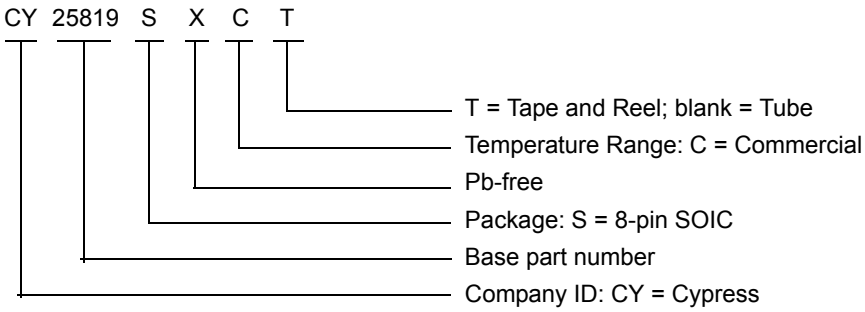
Figure 7. Typical Application Schematic



Ordering Information

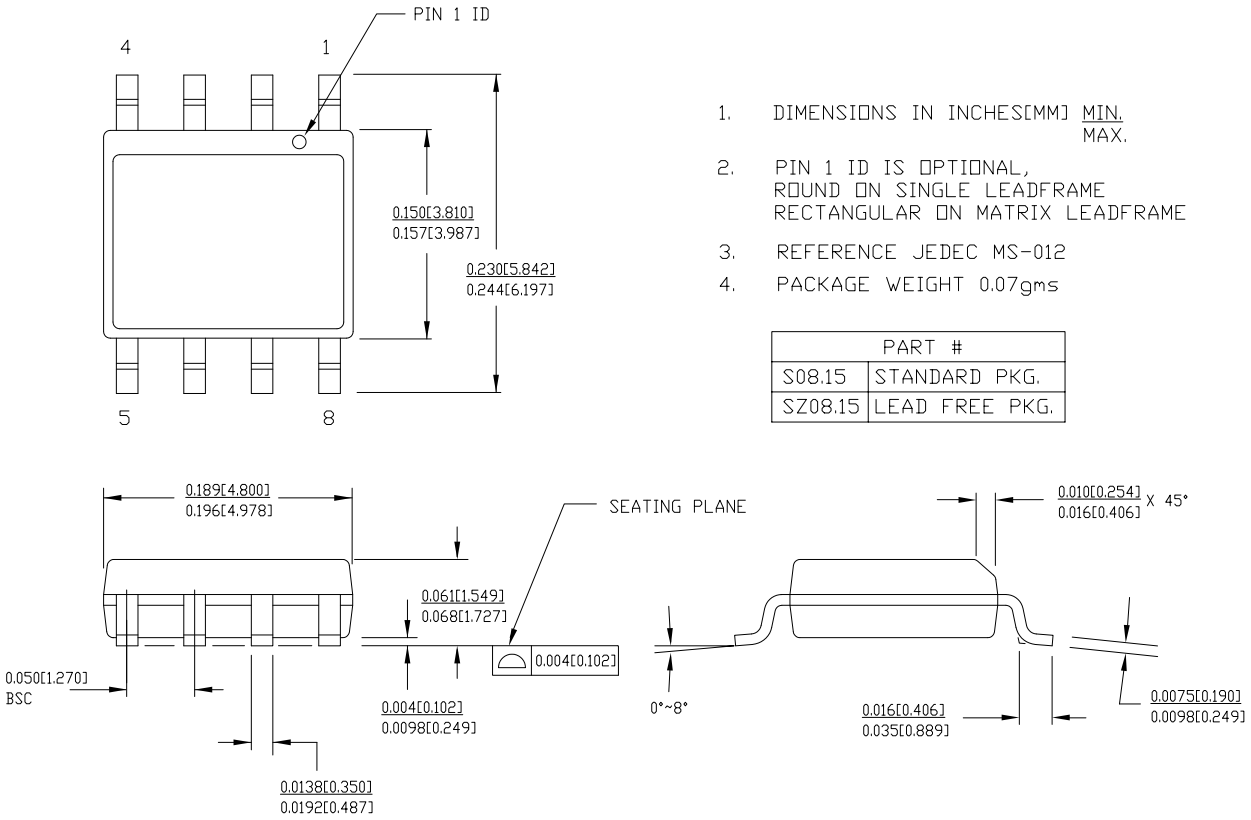
Part Number	Package Type	Product Flow
Pb-Free		
CY25819SXC	8-pin SOIC	Commercial, 0 °C to 70 °C
CY25819SXCT	8-pin SOIC–Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 8. 8-pin SOIC 150 Mils S08.15/SZ08.15



51-85066 *D

Acronyms

Acronym	Description
DVD	digital versatile/video disc
EMI	electromagnetic interference
I/O	input/output
LAN	local area network
LCD	liquid crystal display
PLL	phase locked loop
SOIC	small-outline integrated circuit
SSC	spread spectrum clock
SSCG	spread spectrum clock generator
VCD	video compact disc
WAN	wide area network

Document Conventions

Units of Measure

Symbol	Unit of Measure
dB	decibel
°C	degree Celsius
MHz	Mega Hertz
mA	milli Amperes
mm	milli meter
ms	milli seconds
mW	milli Watts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts
W	Watts

Document History Page

Document Title: CY25819, Spread Spectrum Clock Generator Document Number: 38-07362				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112462	03/21/02	OXC	New Data Sheet
*A	122701	12/28/02	RBI	Added power up requirements to maximum rating information.
*B	448097	See ECN	RGL	Add Lead-free devices
*C	2901658	03/30/10	BASH	Removed inactive parts from the ordering information table. Updated package diagram and contents.
*D	3253540	05/10/2011	CXQ	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5