

750kHz – 800MHz Low Phase Noise Multiplier XO

Universal Low Phase Noise IC's

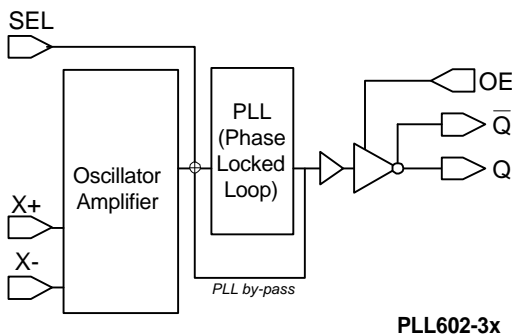
FEATURES

- Selectable 750kHz to 800MHz range.
- Low phase noise output (@ 10kHz frequency offset, -140dBc/Hz for 19.44MHz, -127dBc/Hz for 106.25MHz, -125dBc/Hz for 155.52MHz, -110dBc/Hz for 622.08MHz).
- CMOS (PLL602-37), PECL (PLL602-35 and PLL602-38) or LVDS (PLL602-39) output.
- 12 to 25MHz crystal input.
- No external load capacitor or varicap required.
- Output Enable selector.
- Selectable 1/16 to 32x frequency multiplier.
- 3.3V operation.
- Available in 16-Pin (TSSOP or 3x3mm QFN).

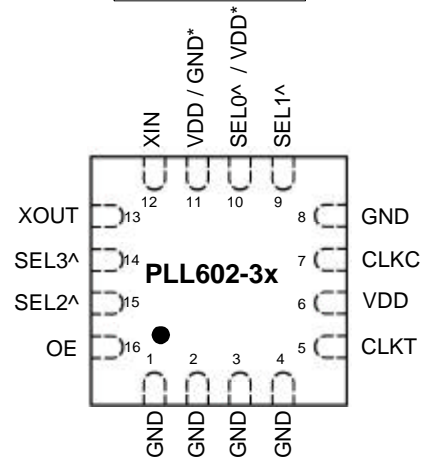
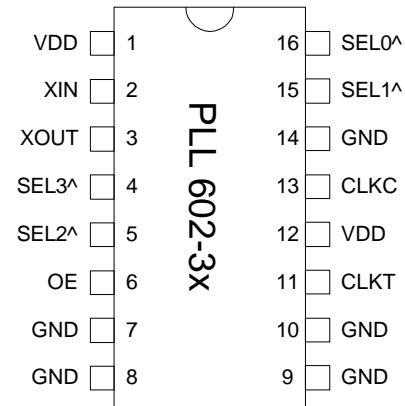
DESCRIPTIONS

The PLL602-35 (PECL with inverted OE), PLL602-37 (CMOS), PLL602-38 (PECL), and PLL602-39 (LVDS) are high performance and low phase noise XO IC chips. They provide phase noise performance as low as -125dBc at 1kHz offset (at 155MHz), by multiplying the input crystal frequency up to 32x. They accept fundamental parallel resonant mode crystals from 12 to 25MHz.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



^: Internal pull-up
*: On 3x3 package, PLL602-35/-38 do not have SEL0 available: Pin 10 is VDD, pin 11 is GND. However, PLL602-37/-39 have SEL0 (pin 10), and pin 11 is VDD. See pin assignment table for details.

OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL602-38	0 (Default)	Output enabled
	1	Tri-state
PLL602-35 PLL602-37 PLL602-39	0	Tri-state
	1 (Default)	Output enabled

OE Input: Logical states defined by PECL levels for PLL602-38
Logical states defined by CMOS levels for PLL602-35/-37/-39

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FREQUENCY SELECTION TABLE

SEL3	SEL2	SEL1	SEL0	Selected Multiplier
0	0	1	1	Fin x 32
0	1	1	0	Fin / 8
0	1	1	1	Fin x 2
1	0	0	1	Fin / 2
1	0	1	0	Fin / 16
1	0	1	1	Fin x 4
1	1	0	0	Fin / 4
1	1	0	1	Fin x 8
1	1	1	0	Fin x 16
1	1	1	1	No multiplication

Note: SEL0 is not available (always "1") for PLL602-35 and PLL602-38 in 3x3mm package

PIN DESCRIPTIONS PLL602-35 and PLL602-38 (see next page of PLL602-37/-39)

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
XIN	2	12	I	Crystal in connector.
XOUT	3	13	I	Crystal out connector.
OE	6	16	I	Output enable pin (see OE logic state table on page 1).
GND	7,8,9,10,14	1,2,3,4,8,11	P	GND.
CLKT	11	5	O	True output PECL
CLKC	13	7	O	Complementary output PECL.
SEL0	16	Not available	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL1	15	9	I	
SEL2	5	15	I	
SEL3	4	14	I	
VDD	1, 12	6,10	P	+3.3V VDD.

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PIN DESCRIPTIONS PLL602-37/-39 (see previous page of PLL602-35/-38)

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
XIN	2	12	I	Crystal in connector.
XOUT	3	13	I	Crystal out connector.
OE	6	16	I	Output enable pin (see OE logic state table on page 1).
GND	7,8,9,10,14	1,2,3,4,8	P	GND.
CLKT	11	5	O	True output LVDS (PLL602-39) (N/C for PLL602-37)
CLKC	13	7	O	Complementary output LVDS (PLL602-39) (CMOS out for PLL602-37).
SEL0	16	10	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL1	15	9	I	
SEL2	5	15	I	
SEL3	4	14	I	
VDD	1, 12	6,11	P	+3.3V VDD.

ELECTRICAL SPECIFICATIONS
1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

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2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	C_L (xtal)			12		pF
Recommended ESR	R_E	AT cut			30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	PECL/LVDS/CMOS	$F_{out} < 24\text{MHz}$			25/25/15	mA
			$24\text{MHz} < F_{out} < 96\text{MHz}$			65/45/30	
			$96\text{MHz} < F_{out} < 800\text{MHz}$			100/80/40	
Operating Voltage	V_{DD}		3.13		3.47	V	
Output Clock Duty Cycle		@ 1.4V (CMOS) @ 1.25V (LVDS) @ $V_{DD} - 1.3\text{V}$ (PECL)	45 45 45	50 50 50	55 55 55	%	
Short Circuit Current				± 50		mA	

4. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			12		25	MHz
Output Clock Rise Time		0.8V ~ 2.0V with 10 pF load			1.5	ns
		0.3V ~ 3.0V with 15 pF load		3.7	5	
Output Clock Fall Time		2.0V ~ 0.8V with 10 pF load			1.5	
		3.0V ~ 0.3V with 15pF load		3.7	5	
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%
Short Circuit Current				± 50		mA

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5. Jitter specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND.	19.44MHz		5		ps
		77.76MHz		8		
		155.52MHz		9		
		622.08MHz		10		
Accumulated jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	155.52MHz		TBM		ps
Integrated jitter RMS	Integrated 12 kHz to 20 MHz	155.52MHz		3	4	ps

6. Phase noise specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	19.44MHz	-60	-90	-112	-140	-150	dBc/Hz
	106.25MHz	-60	-90	-112	-127	-125	
	155.52MHz	-60	-90	-112	-125	-123	
	622.08MHz	-60	-90	-109	-110	-109	

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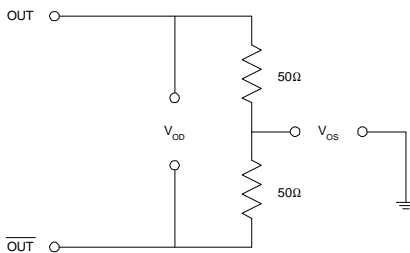
7. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

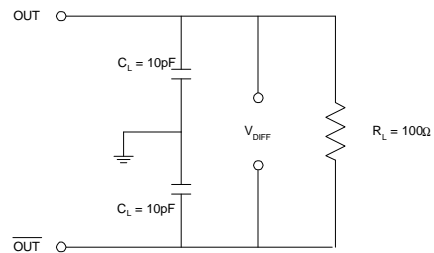
8. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	$R_L = 100 \Omega$ $C_L = 10 pF$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

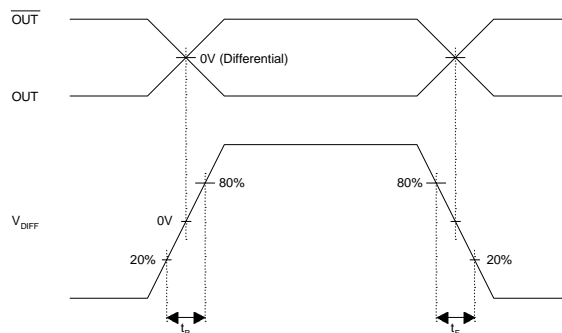
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



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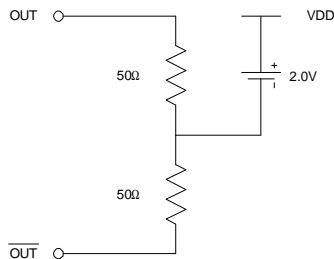
9. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	V_{OL}			$V_{DD} - 1.620$	V

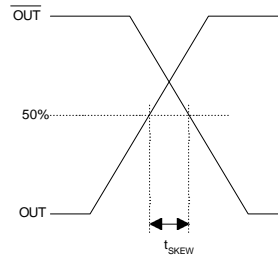
10. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	0.8V ~ 2.0V			1.5	ns
Clock Fall Time	t_f	2.0V ~ 0.8V			1.5	ns
Duty Cycle		Measured @ 1.4V	40	50	60	%

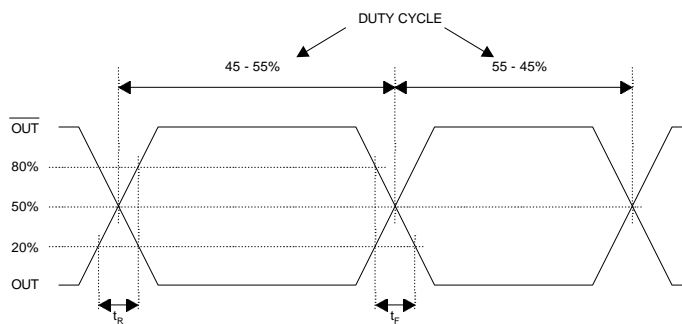
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



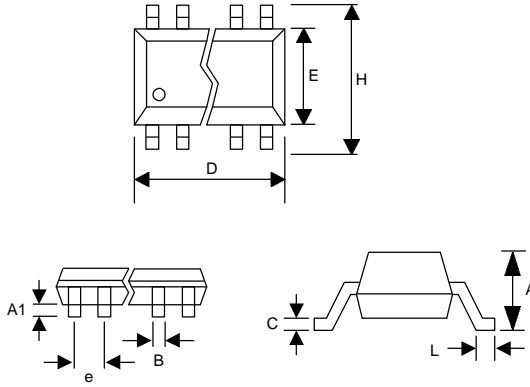
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PACKAGE INFORMATION

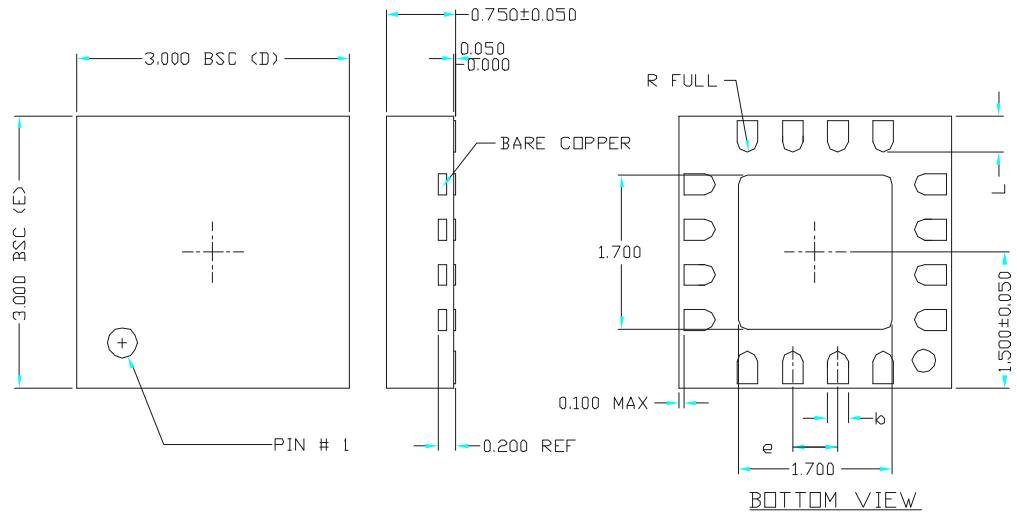
16 PIN Narrow SOIC, TSSOP (mm)

Symbol	SOIC		TSSOP	
	Min.	Max.	Min.	Max.
A	1.35	1.75	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	9.80	10.00	4.90	5.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	



VARIATIONS:

SYMBOL	16 LD		
	MIN	NDM	MAX
e	0.50 BSC		
k	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		



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ORDERING INFORMATION

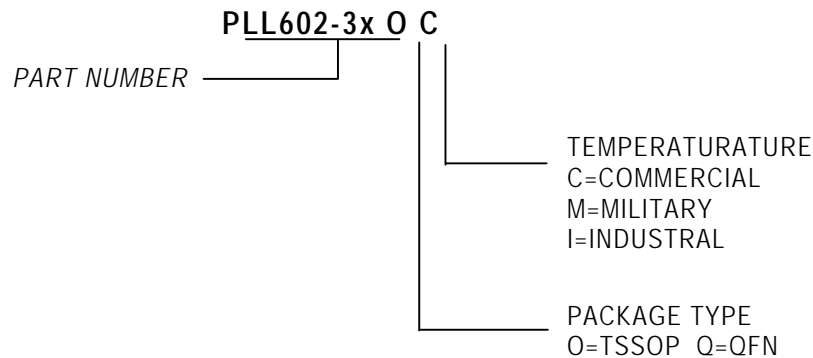
For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



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