

Dual Enhancement Mode MOSFET (N-and P-Channel)

Features

- N-Channel
40V/7.5A,
 $R_{DS(ON)} = 21m\Omega$ (typ.) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 30m\Omega$ (typ.) @ $V_{GS} = 4.5V$
- P-Channel
-40V/-6A,
 $R_{DS(ON)} = 36m\Omega$ (typ.) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 50m\Omega$ (typ.) @ $V_{GS} = -4.5V$
- Super High Dense Cell Design
- Reliable and Rugged
- Lead Free Available (RoHS Compliant)

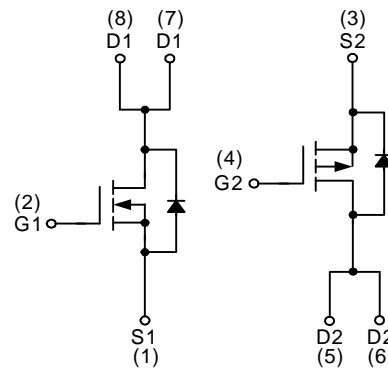
Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems

Pin Description



Top View of PDIP – 8



N-Channel MOSFET P-Channel MOSFET

Ordering and Marking Information

<p>APM4568 □□-□□□</p> <div style="margin-left: 20px;"> <p>└─ Lead Free Code</p> <p>└─ Handling Code</p> <p>└─ Temp. Range</p> <p>└─ Package Code</p> </div>	<p>Package Code J : PDIP-8</p> <p>Operating Junction Temp. Range C : -55 to 150 °C</p> <p>Handling Code TU : Tube</p> <p>Lead Free Code L : Lead Free Device Blank : Original Device</p>
<p>APM4568 J : APM4568 XXXXX</p>	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N Channel	P Channel	Unit	
V_{DSS}	Drain-Source Voltage	40	-40	V	
V_{GSS}	Gate-Source Voltage	± 20	± 20		
I_D^*	Continuous Drain Current	$V_{GS}=10\text{V (N)}$	7.5	-6	A
I_{DM}^*	Pulsed Drain Current	$V_{GS}=-10\text{V (P)}$	30	-20	
I_S^*	Diode Continuous Forward Current	2.8	-2.8	A	
T_J	Maximum Junction Temperature	150		$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55 to 150			
P_D^*	Power Dissipation	$T_A=25^\circ\text{C}$	2.5		W
		$T_A=100^\circ\text{C}$	1		
$R_{\theta JA}^*$	Thermal Resistance-Junction to Ambient	50		$^\circ\text{C/W}$	

Note:

*Surface Mounted on 1in^2 pad area, $t \leq 10\text{sec}$.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	APM4568J			Unit		
			Min.	Typ.	Max.			
Static Characteristics								
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_{DS}=250\mu\text{A}$	N-Ch	40			V	
		$V_{GS}=0\text{V}, I_{DS}=-250\mu\text{A}$	P-Ch	-40				
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$	N-Ch			1	μA	
						30		
		$V_{DS}=-32\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$	P-Ch					-1
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu\text{A}$	N-Ch	1.3	2	2.5	V	
		$V_{DS}=V_{GS}, I_{DS}=-250\mu\text{A}$	P-Ch	-1.3	-1.9	-2.5		
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	N-Ch			± 100	nA	
		$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	P-Ch			± 100		
$R_{DS(ON)}^a$	Drain-Source On-State Resistance	$V_{GS}=10\text{V}, I_{DS}=7.5\text{A}$	N-Ch		21	29	$\text{m}\Omega$	
		$V_{GS}=-10\text{V}, I_{DS}=-6\text{A}$	P-Ch		36	50		
		$V_{GS}=4.5\text{V}, I_{DS}=5\text{A}$	N-Ch		30	44		
		$V_{GS}=-4.5\text{V}, I_{DS}=-4\text{A}$	P-Ch		50	70		

Electrical Characteristics (Cont.) ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	APM4568J			Unit	
			Min.	Typ.	Max.		
Diode Characteristics							
V_{SD}^a	Diode Forward Voltage	$I_{SD}=2A, V_{GS}=0V$	N-Ch		0.8	1.1	V
		$I_{SD}=-2A, V_{GS}=0V$	P-Ch		-0.8	-1.1	
Dynamic Characteristics^b							
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	N-Ch		2		Ω
			P-Ch		8		
C_{iss}	Input Capacitance	N-Channel $V_{GS}=0V,$ $V_{DS}=20V,$ Frequency=1.0MHz	N-Ch		980		pF
			P-Ch		1095		
C_{oss}	Output Capacitance	P-Channel $V_{GS}=0V,$ $V_{DS}=-20V,$	N-Ch		110		
			P-Ch		125		
C_{rss}	Reverse Transfer Capacitance	N-Channel $V_{GS}=0V,$ $V_{DS}=-20V,$	N-Ch		75		
			P-Ch		70		
$t_{d(ON)}$	Turn-on Delay Time	N-Channel $V_{DD}=20V, R_L=20\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	N-Ch		16	30	ns
			P-Ch		12	23	
t_r	Turn-on Rise Time	P-Channel $V_{DD}=-20V, R_L=20\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	N-Ch		19	35	
			P-Ch		21	39	
$t_{d(OFF)}$	Turn-off Delay Time	N-Channel $V_{DD}=20V, R_L=20\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	N-Ch		30	55	
			P-Ch		43	78	
t_f	Turn-off Fall Time	P-Channel $V_{DD}=-20V, R_L=20\Omega,$ $I_{DS}=-1A, V_{GEN}=-10V,$ $R_G=6\Omega$	N-Ch		6	12	
			P-Ch		11	21	
Q_{rr}	Reverse Recovery Charge	N-Channel $I_{SD}=7.5A, dI_{SD}/dt = 100A/\mu s$ P-Channel $I_{SD}=-6A, dI_{SD}/dt = 100A/\mu s$	N-Ch		22		nC
			P-Ch		20		
			N-Ch		15		
			P-Ch		13		
Gate Charge Characteristics^b							
Q_g	Total Gate Charge	N-Channel $V_{DS}=20V, V_{GS}=10V,$ $I_{DS}=7.5A$	N-Ch		20	28	nC
			P-Ch		20	28	
Q_{gs}	Gate-Source Charge	P-Channel $V_{DS}=-20V, V_{GS}=-10V,$ $I_{DS}=-6A$	N-Ch		3		
			P-Ch		3.5		
Q_{gd}	Gate-Drain Charge	N-Channel $V_{DS}=20V, V_{GS}=10V,$ $I_{DS}=7.5A$	N-Ch		6		
			P-Ch		3.5		

Notes:

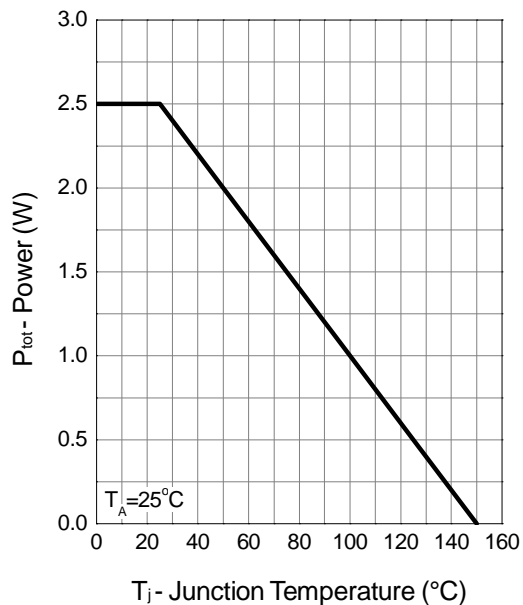
a : Pulse test ; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

b : Guaranteed by design, not subject to production testing.

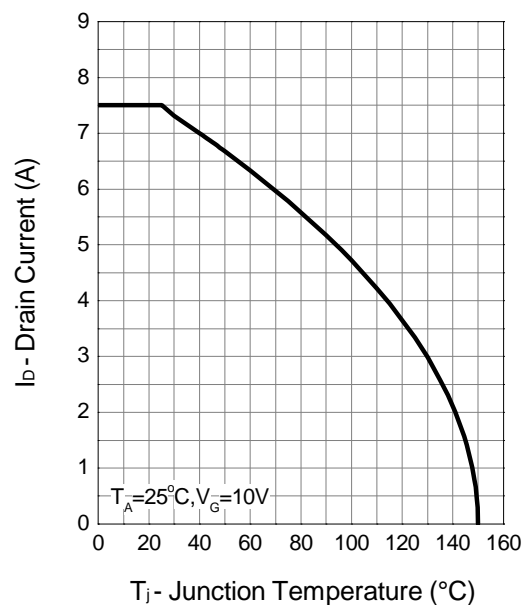
Typical Characteristics

N-Channel

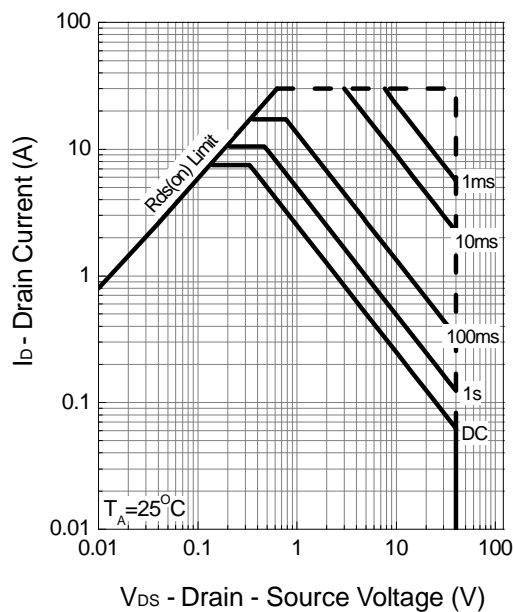
Power Dissipation



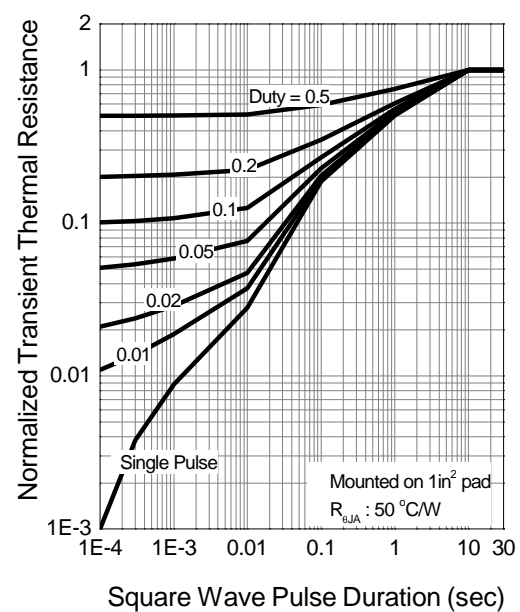
Drain Current



Safe Operation Area



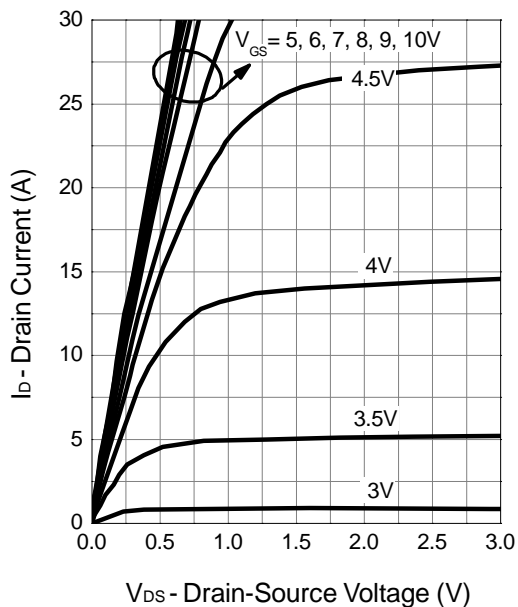
Thermal Transient Impedance



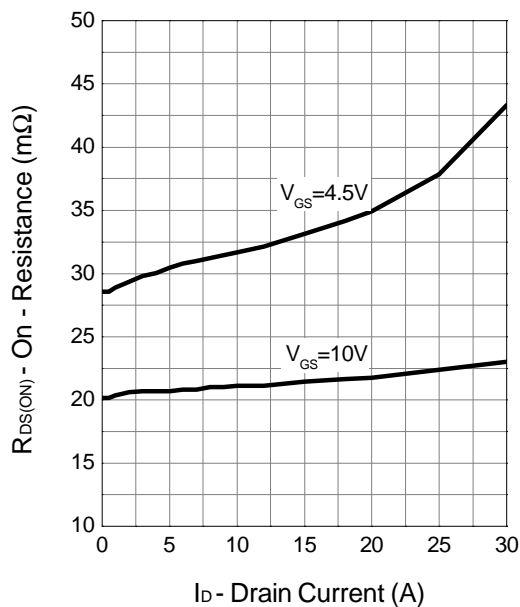
Typical Characteristics (Cont.)

N-Channel

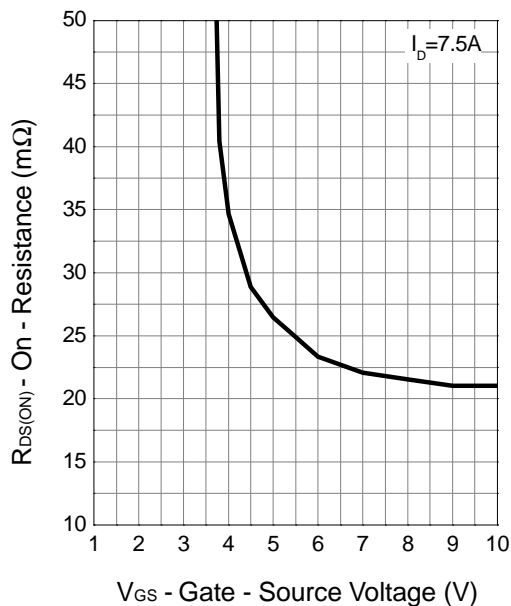
Output Characteristics



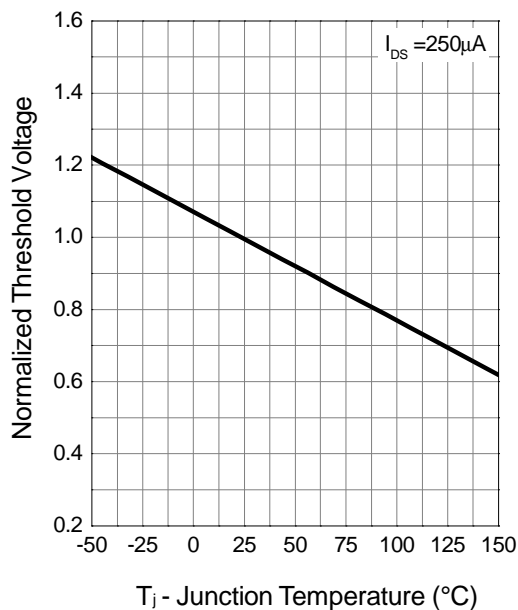
Drain-Source On Resistance



Drain-Source On Resistance



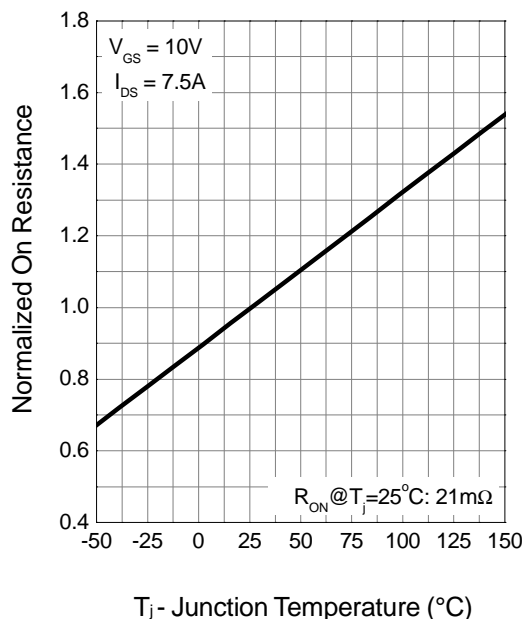
Gate Threshold Voltage



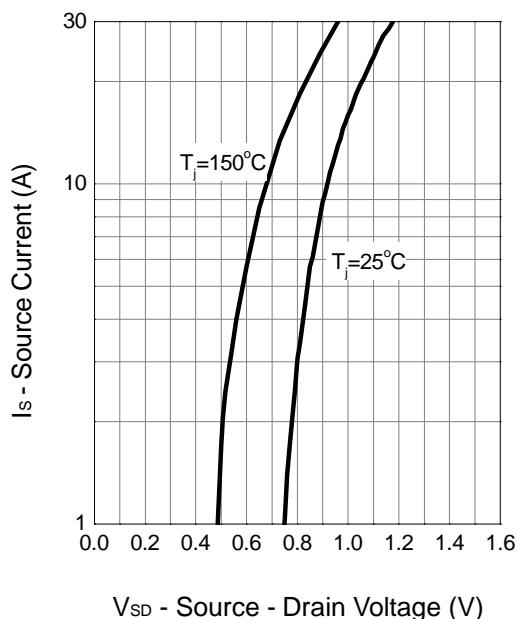
Typical Characteristics (Cont.)

N-Channel

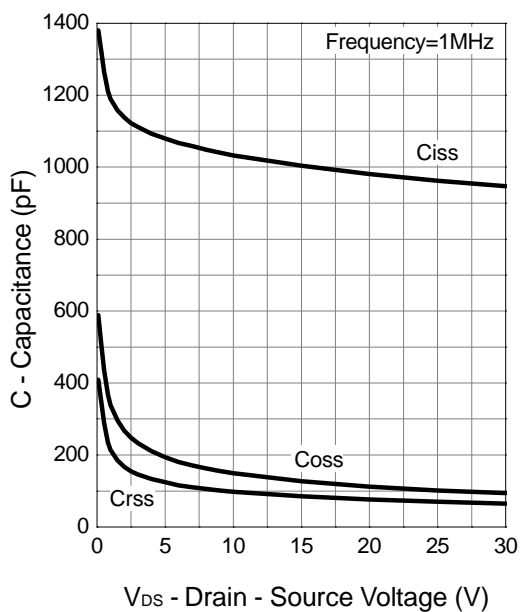
Drain-Source On Resistance



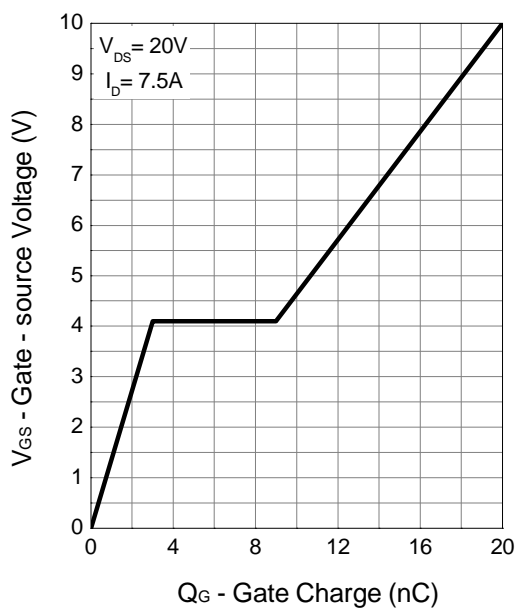
Source-Drain Diode Forward



Capacitance



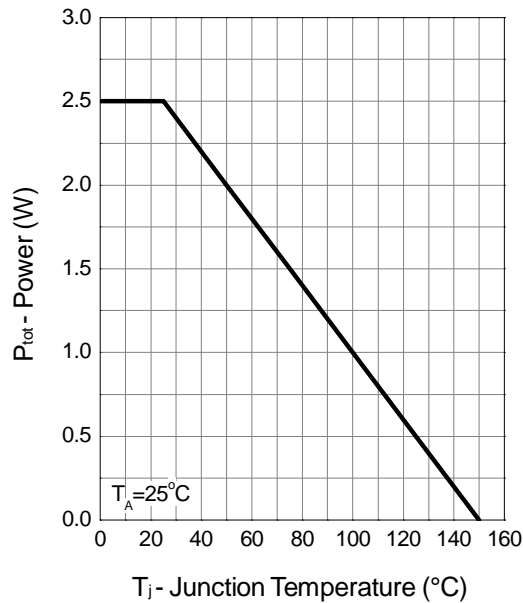
Gate Charge



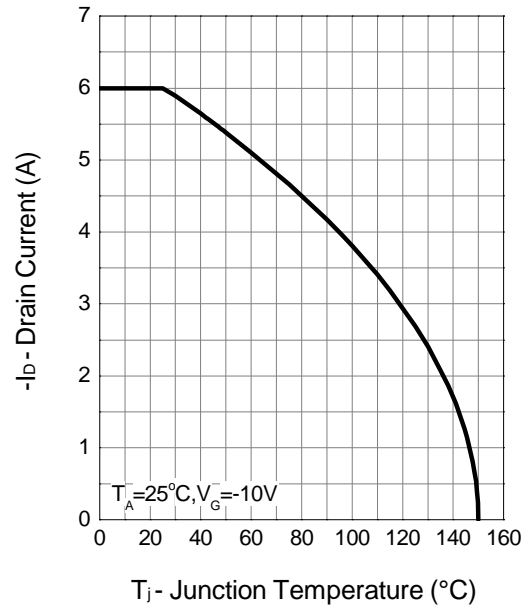
Typical Characteristics (Cont.)

P-Channel

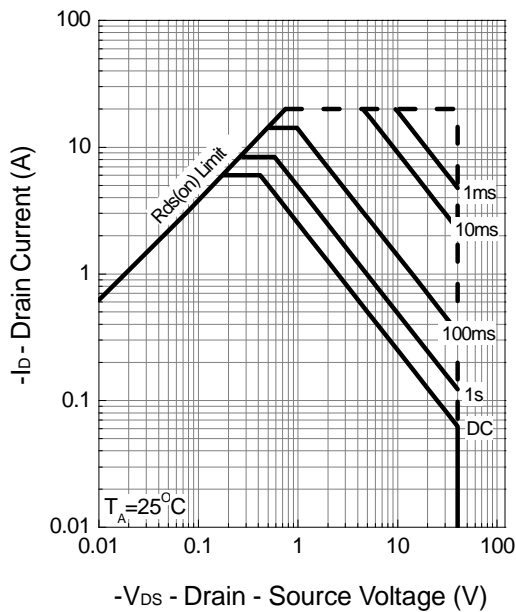
Power Dissipation



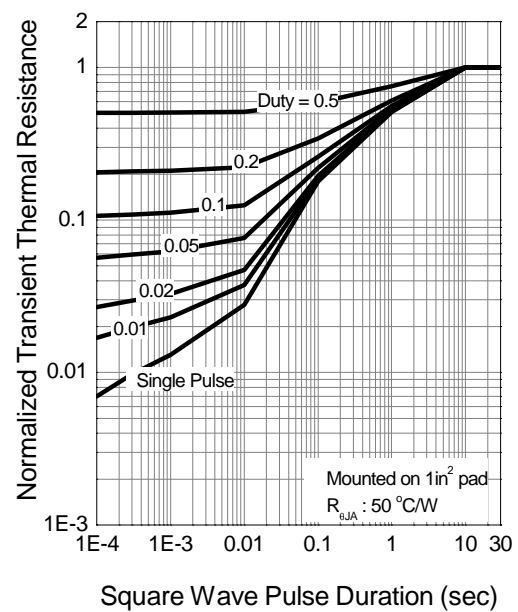
Drain Current



Safe Operation Area



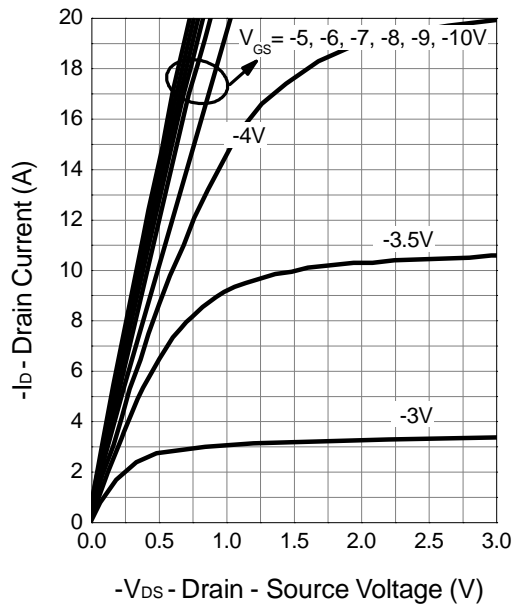
Thermal Transient Impedance



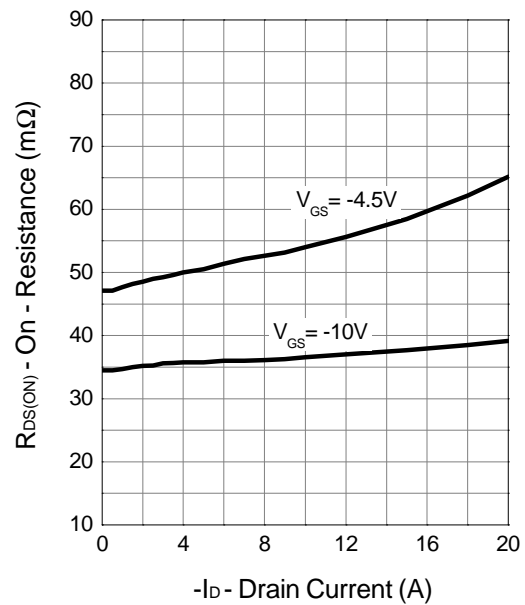
Typical Characteristics (Cont.)

P-Channel

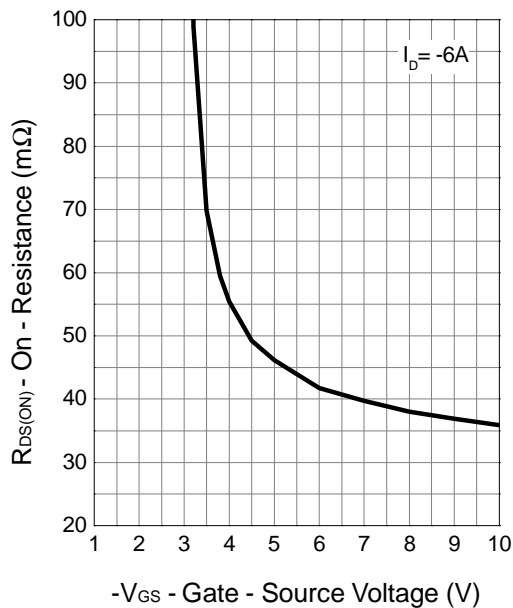
Output Characteristics



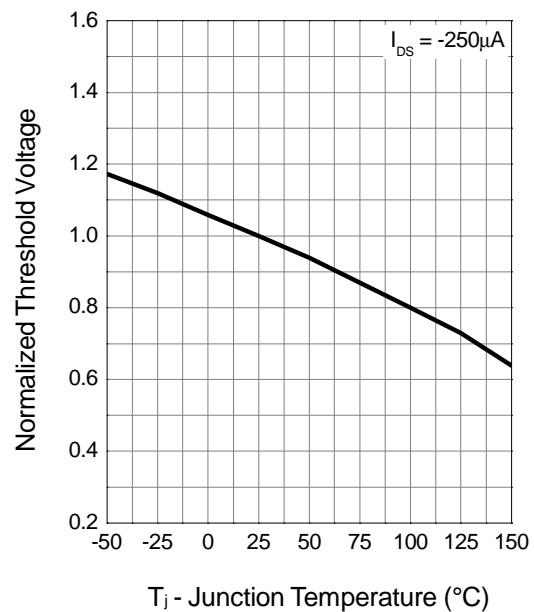
Drain-Source On Resistance



Drain-Source On Resistance



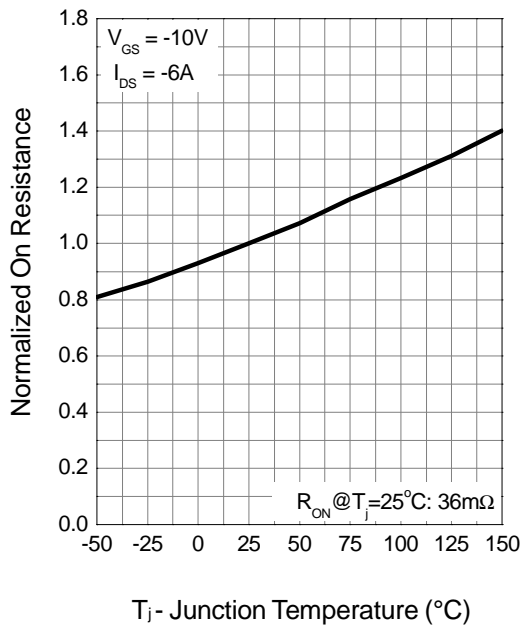
Gate Threshold Voltage



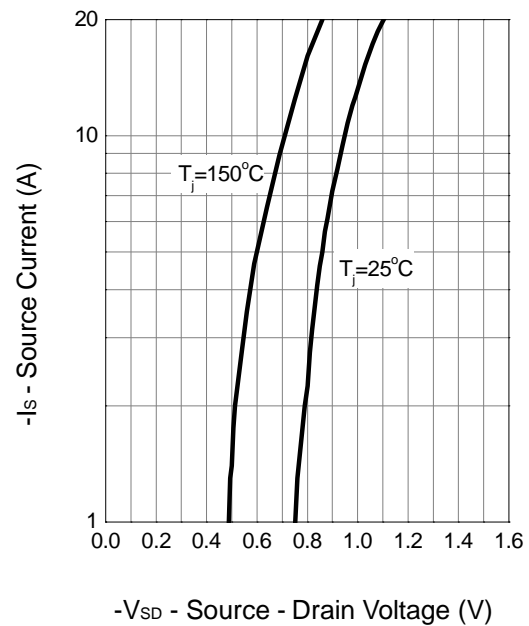
Typical Characteristics (Cont.)

P-Channel

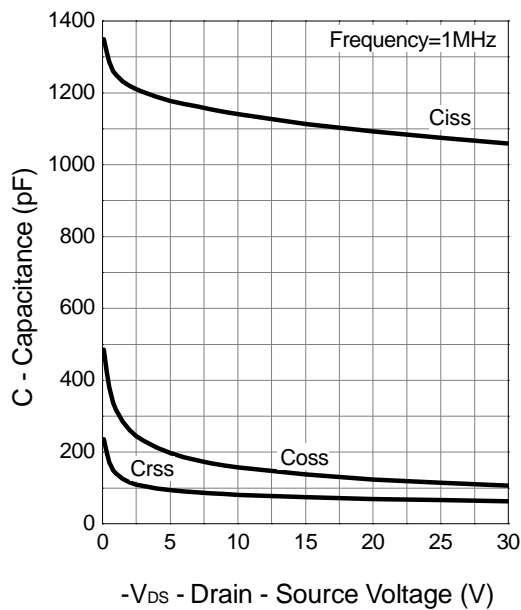
Drain-Source On Resistance



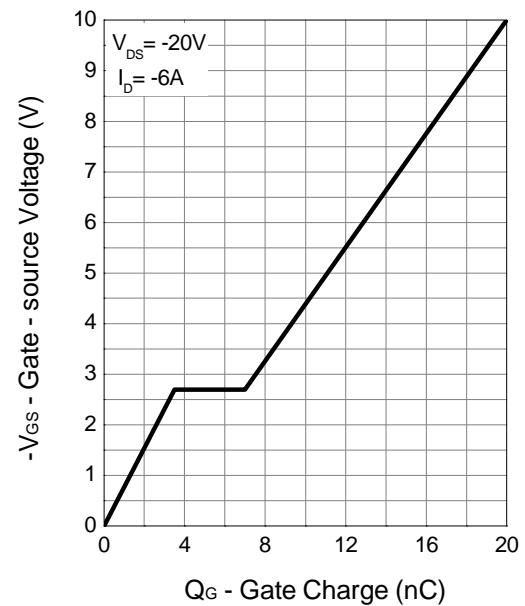
Source-Drain Diode Forward



Capacitance

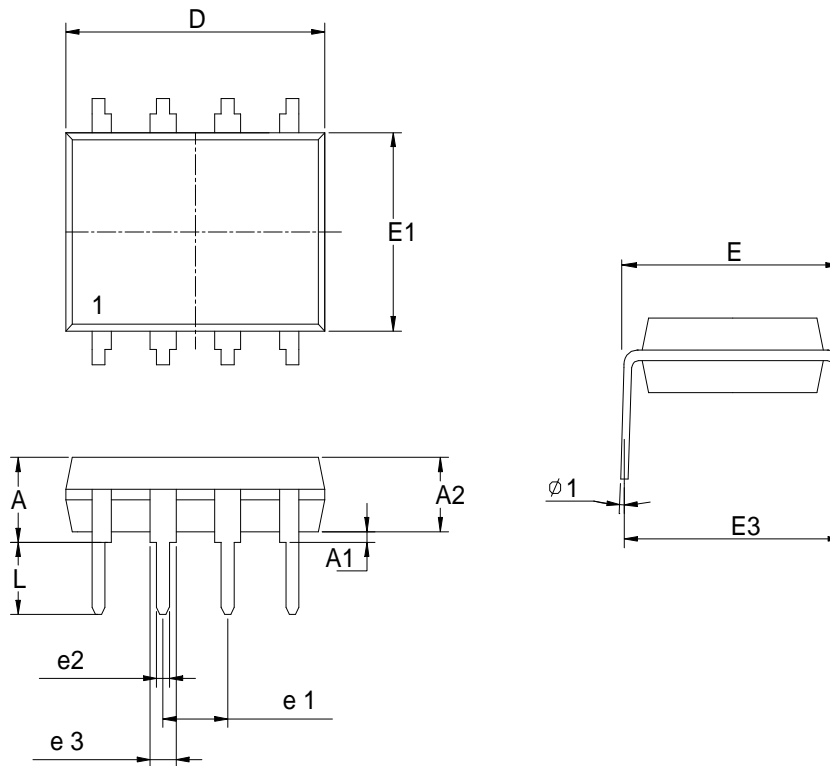


Gate Charge



Packaging Information

PDIP-8 pin (Reference JEDEC Registration MS-001)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	3.68	0.115	0.145
D	9.02	10.16	0.355	0.400
e1	2.54 BSC		0.100 BSC	
e2	0.36	0.56	0.014	0.022
e3	1.14	1.78	0.045	0.070
E	7.62 BSC		0.300 BSC	
E1	6.10	7.11	0.240	0.280
E3		10.92		0.430
L	2.92	3.81	0.115	0.150
φ1	15° REF		15° REF	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C,5 SEC
HOLT	MIL-STD 883D-1005.7	1000 Hrs Bias @ 125°C
PCT	JESD-22-B, A102	168 Hrs, 100% RH, 121°C
TST	MIL-STD 883D-1011.9	-65°C ~ 150°C, 200 Cycles

Customer Service

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