MITSUMI

IC for System Reset (with built-in watchdog timer)
Monolithic IC MM1035

August 19, 2003

Outline

This IC functions in a variety of CPU systems and other logic systems to generate a reset signal and the system accurately when the power is turned on or interrupted.

It includes a watchdog timer which allows diagnosis of the system operation, so that it prevents system runaway by intermittently generating a reset pulse when system misoperation occurs.

Features

1. Built-in watchdog timer
2. Low minimum operating voltage V_{CC}=0.8V typ.
3. Positive and negative logic reset outputs can be extracted
4. Accurate detection of drop in supply voltage
5. Detection voltage with hysteresis
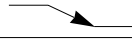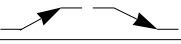6. Few external components   one capacitor

Packages

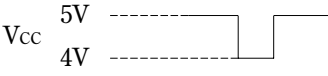DIP-8A (MM1035XD)
SOP-8A (MM1035XF)

Applications

Microcomputers
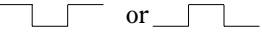
Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Units
Storage temperature	T_{STG}	–40~+125	℃
Operating temperature	T_{OPR}	–20~+70	℃
Power supply voltage	V_{CC} max.	–0.3~+10	V
Voltage applied to VS & CK pins	V_{VS} & V_{CK}	–0.3~+10	V
Voltage applied to $\overline{RESET}$, RESET pin	V_{OH}	–0.3~+10	V
Allowable loss	Pd	400 (DIP-8)	mW
		340 (SOP-8)	

Electrical Characteristics 1 (DC)

(Except where noted otherwise, Ta=25℃, Vcc=5V, measurement circuit 1)
(Except where noted otherwise, resistance unit is Ω)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	I_{CC}	1	During watchdog timer operation		0.7	1.0	mA
Detection voltage	V_{SL}	1	V_S=OPEN, V_{CC} ⬊	4.05	4.20	4.35	V
	V_{SH}	1	V_S=OPEN, V_{CC} ⬈	4.15	4.30	4.45	
Detection voltage temperature coefficient	$V_S/\triangle T$	1			±0.01		%/℃
Hysteresis voltage	V_{HYS}	1	V_{SH}–V_{SL}, V_{CC}	50	100	150	mV
CK input threshold	V_{TH}	1		0.8	1.2	2	V
CK input current	I_{IH}	1	V_{CK}=5V		0	1	μA
	I_{IL}	1	V_{CK}=0V	−20	−10	−3	
Output voltage (High)	$V_{OH}1$	1	$I_{\overline{RESET}}$ =−5μA, V_S=OPEN	4.5	4.8		V
	$V_{OH}2$	1	I_{RESET}=−5μA, V_S=0V	4.5	4.8		
Output voltage (Low)	$V_{OL}1$	1	$I_{\overline{RESET}}$ =3mA, V_S=0V		0.2	0.4	V
	$V_{OL}2$	1	$I_{\overline{RESET}}$ =10mA, V_S=0V		0.3	0.5	
	$V_{OL}3$	1	I_{RESET}=0.5mA, V_S=OPEN		0.2	0.4	
	$V_{OL}4$	1	I_{RESET}=1mA, V_S=OPEN		0.3	0.5	
Output sink current	$I_{OL}1$	1	$V_{\overline{RESET}}$ =1.0V, V_S=0V	10	16		mA
	$I_{OL}2$	1	V_{RESET}=1.0V, V_S=OPEN	1	2		
C_T charge current	$I_{CT}1$	1	V_{TC} = 1.0V during watchdog timer operation	−8	−12	−24	μA
	$I_{CT}2$	1	V_{TV} = 1.0V during power on reset operation	−0.8	−1.2	−2.4	μA
Minimum operating power supply voltage to ensure $\overline{RESET}$	$V_{CCL}1$	1	$V_{\overline{RESET}}$ =0.4V $I_{\overline{RESET}}$ =0.2mA		0.8	1.0	V
Minimum operating power supply voltage to ensure $\overline{RESET}$	$V_{CCL}2$	1	I_{RESET}=V_{CC}−0.1V R_L2 (between Pin 2 and GND) =1M		0.8	1.0	V

Electrical Characteristics 2 (AC)
(Except where noted otherwise, Ta=25℃, Vcc=5V, measurement circuit 2)
(Except where noted otherwise, resistance unit is Ω)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Vcc input pulse width	T_{PI}	2	V_{CC} 5V ⎍ 4V	8			μs
CK input pulse width	T_{CKW}	2	CK ⎍ or ⎍	3			μs
CK input cycle	T_{CK}	2		20			μs
Watchdog timer monitoring time *1	T_{WD}	2	C_T=0.1μF	5	10	15	ms
Reset time for watchdog timer *2	T_{WR}	2	C_T=0.1μF	1	2	3	ms
Reset hold time for power supply rise *3	T_{PR}	2	C_T=0.1μF, V_{CC} ⟋	50	100	150	ms
Output delay time from Vcc *4	$T_{PD}1$	2	$\overline{RESET}$ pin R_L1=2.2k, C_L1=100pF		2	10	μs
	$T_{PD}2$	2	$\overline{RESET}$ pin R_L2=10k, C_L2=20pF		3	10	
Output rise time *5	t_R1	2	$\overline{RESET}$ pin R_L1=2.2k, C_L1=100pF		1.0	1.5	μs
	t_R2	2	$\overline{RESET}$ pin R_L2=10k, C_L2=20pF		1.0	1.5	μs

Notes :

*1: Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse, until reset pulse output. In other words, reset output is output if a clock pulse is not input during this time.

*2: Reset time means reset pulse width. However, this does not apply to power on reset.

*3: Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SH}) during power on reset, until $\overline{RESET}$ output goes high (reset release).

*4: Output delay time is the time from when power supply voltage drops below detection voltage (V_{SL}), until $\overline{RESET}$ output goes low (reset status).

*5: Voltage range when measuring output rise and fall is 10~90%.

*6: Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. The times are expressed by the following formulae. The recommended range for C_T is 0.001~10μF.

$$T_{PR} \text{ (ms)} \fallingdotseq 1000 \times C_T \text{ (μF)}$$
$$T_{WD} \text{ (ms)} \fallingdotseq 100 \times C_T \text{ (μF)}$$
$$T_{WR} \text{ (ms)} \fallingdotseq 20 \times C_T \text{ (μF)}$$

Example : When C_T=0.1μF
$$T_{PR} \fallingdotseq 100ms$$
$$T_{WD} \fallingdotseq 10ms$$
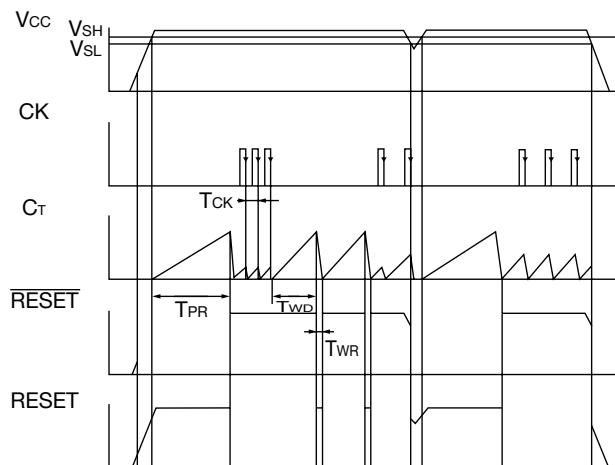$$T_{WR} \fallingdotseq 2ms$$
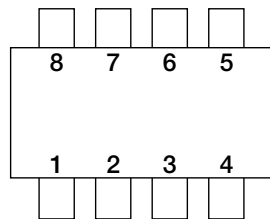
Block Diagram
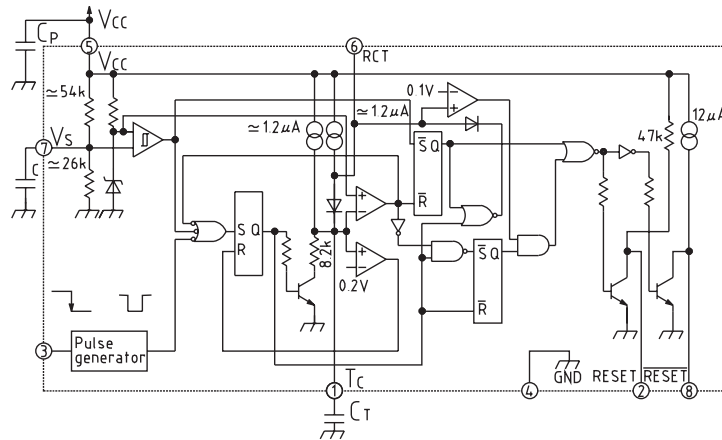
Note 1: CP = 0.1µF approx.

Note 2: C ≧ 1000pF.

Note 3: The watchdog timer can be stopped by connecting the RCT pin to GND.
(Then it functions as a voltage detection circuit.)

Timing Chart

Pin Assignment

1	T_C
2	RESET
3	CK
4	GND
5	V_{CC}
6	RCT
7	V_S
8	$\overline{RESET}$

Pin Description

Pin No.	Pin Name	Function
1	T_C	T_{WD}, T_{WR}, T_{PR} variable pins. (T_{WD}, T_{WR} and T_{PR} times are determined by the external capacitor.)
2	RESET	Reset output pin (High output)
3	CK	Clock input pin (inputs clock from logic system)
4	GND	GND pin
5	V_{CC}	4.2V detection voltage
6	RCT	Watchdog timer stop pin Operation modes: Operation→OPEN, Stop→connect to GND
7	VS	Detection voltage variable pin Variation modes : Lower → pull up resistance, Raise → pull down
8	$\overline{\text{RESET}}$	Reset output pin (Low output)

Measuring Circuit

■ Measuring Circuit 1 (DC)
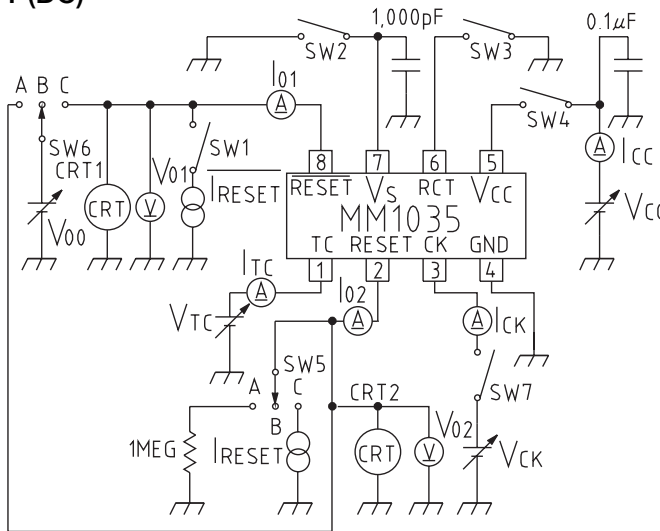
■ Measuring Circuit 2 (AC)
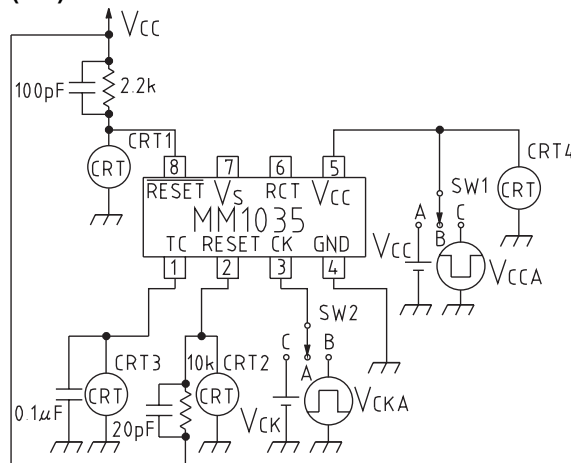
Measuring Circuit 1 SW Table 6-1-2. SW&Power Supply Table 1

Item	Symbol	SW1	SW2	SW3	SW4	SW5	SW6	SW7	Vcc	Vck	Vct	I̅RESET	IRESET	VM, IM	Notes
Consumption current	Icc	OFF	OFF	OFF	ON	B	B	ON	5V	5V	0V	–	–	Icc	
Detection voltage	VSL	OFF	OFF	ON	ON	B	B	ON	5V→0V	3V	3V	–	–	Vo1, CRT1	
	VSH	OFF	OFF	ON	ON	B	B	ON	4V→5V	3V	3V	–	–	Vo1, CRT1	
CK input threshold	VTH	OFF	OFF	OFF	ON	B	B	ON	5V	0V→3V	1V	–	–	Ick	
CK input current	IIH	OFF	OFF	OFF	ON	B	B	ON	5V	5V	0V	–	–	Ick	
	IIL	OFF	OFF	OFF	ON	B	B	ON	5V	0V	0V	–	–	Ick	
Output voltage (High)	VOH1	ON	OFF	ON	ON	B	B	ON	5V	5V	3V	–5µA	–	Vo1	
	VOH2	OFF	ON	ON	ON	C	B	ON	5V	5V	3V	–	–5µA	Vo2	
Output voltage (Low)	VOL1	ON	ON	ON	ON	B	B	ON	5V	5V	3V	3mA	–	Vo1	
	VOL2	ON	ON	ON	ON	B	B	ON	5V	5V	3V	10mA	–	Vo1	
	VOL3	OFF	OFF	ON	ON	C	B	ON	5V	5V	3V	–	0.5mA	Vo2	
	VOL4	OFF	OFF	ON	ON	C	B	ON	5V	5V	3V	–	1mA	Vo2	
Output sink current	IOL1	OFF	ON	ON	ON	B	C	ON	5V	5V	3V	–	–	Io1	Voo=1V
	IOL2	OFF	OFF	ON	ON	B	A	ON	5V	5V	3V	–	–	Io2	Voo=1V
CT charge current 1	ITC1	OFF	OFF	OFF	ON	B	B	OFF	5V	–	1V	–	–	ITC	
CT charge current 2	ITC2	OFF	OFF	ON	ON	B	B	OFF	5V	–	1V	–	–	ITC	
Minimum operating power supply voltage to ensure reset	VCCL1	ON	OFF	ON	ON	B	B	ON	0V→2V	0V	0V		–	Vo1, Vcc	
Minimum operating power supply voltage to ensure reset	VCCL2	OFF	ON	ON	ON	A	B	ON	0V→2V	0V	0V	–	–	Vo2, Vcc	

Measuring Circuit 2 SW Table 6-2-2. SW&Power Supply Table 2

Item	Symbol	SW1	SW2	VCCA	Vcc	VCKA	Vck	CRT	Notes
Vcc input pulse width	TPI	C	B	5V / 4V T1	–	1.4V / 0V T2 T3	–	CRT1,2,3	T1=8µs
CK input pulse width	TCKW	A	B		5V	1.4V / 0V T2 or T2	–	CRT1,2,3	T2=3µs
CK input cycle	TCK	A	B		5V	1.4V / 0V T2 T3	–	CRT1,2,3	T3=20µs
Watchdog timer monitoring time	TWD	A	A		5V		5V	CRT1,2,3	
Reset time for watchdog timer	TWR	A	A		5V		5V	CRT1,2,3	
Reset hold time for power supply rise	TPR	B→A	A		5V		5V	CRT1,2,3	
Output delay time from Vcc	TPD1	C	A	5V / 0V	–		0V	CRT1,3	
	TPD2	C	A	5V / 0V	–		0V	CRT2,3	
Output rise time	TR1	A	A		5V		5V	CRT1	
	TR2	A	A		5V		5V	CRT2	
Output fall time	TP1	A	A		5V		5V	CRT1	
	TP2	A	A		5V		5V	CRT2	

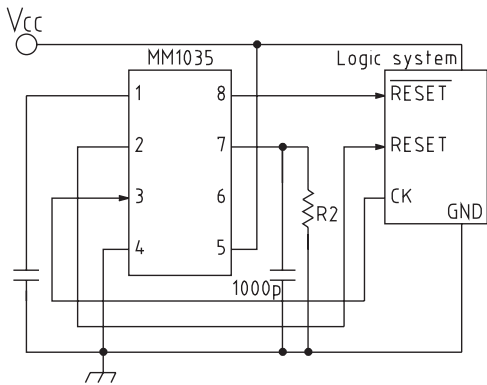## Detection Voltage Variation 1 (lowering detection voltage)
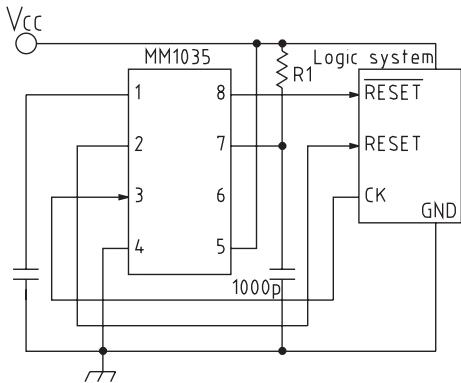
Detection voltage can be changed by connecting resistor R1 externally to MM1035 Vs pin. Determine R1 according to graph 1 when changing Vs.

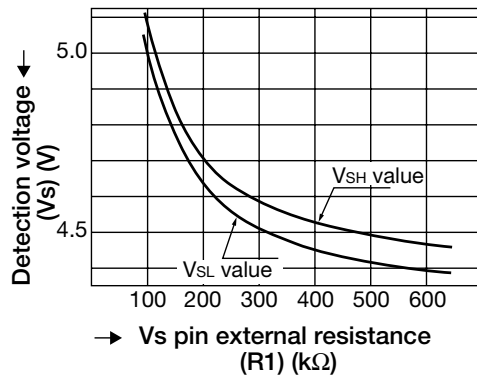Graph 1. Detection voltage change using MM1035 external resistor
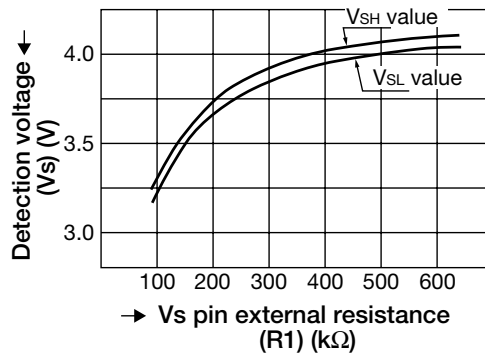
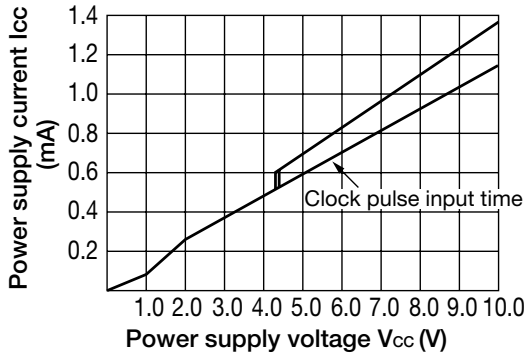## Detection Voltage Variation 2 (raising detection voltage)

Detection voltage can be changed by connecting resistor R2 externally to MM1035 Vs pin. Determine R2 according to graph 2 when changing Vs.

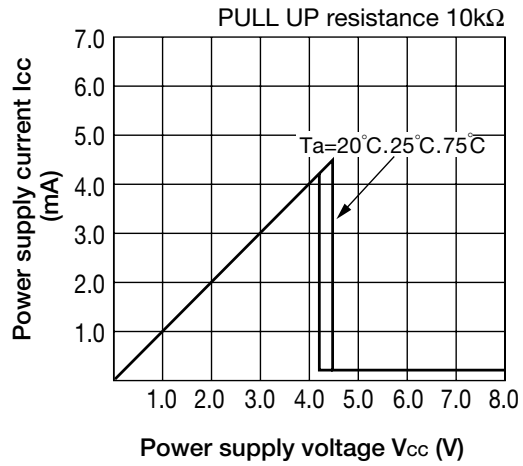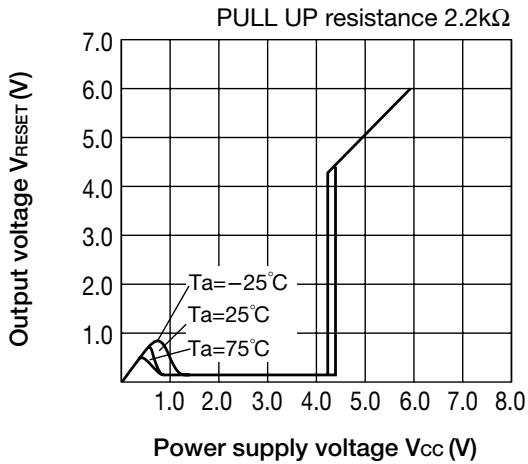Graph 2. Detection voltage change using MM1035 external resistor

Characteristics

■ Power supply current-Power supply voltage

Power supply current Icc (mA) vs Power supply voltage V_{CC} (V)

Clock pulse input time

■ Output voltage-Power supply voltage (RESET pin)

PULL UP resistance 10kΩ

Power supply current Icc (mA) vs Power supply voltage V_{CC} (V)

Ta=20°C.25°C.75°C

■ Output voltage-Power supply voltage ($\overline{\text{RESET}}$ pin)

PULL UP resistance 2.2kΩ

Output voltage V_{RESET} (V) vs Power supply voltage V_{CC} (V)

Ta=−25°C
Ta=25°C
Ta=75°C

■ Detection voltage (V_{SL}, V_{SH}) temperature (RESET, $\overline{\text{RESET}}$ pins)
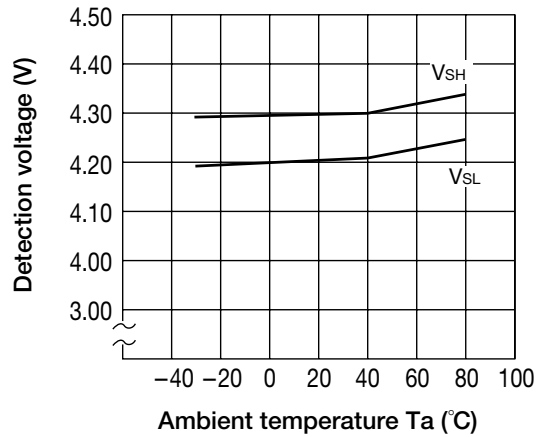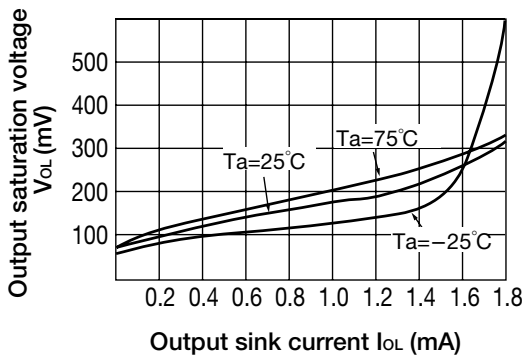
Detection voltage (V) vs Ambient temperature Ta (°C)

V_{SH}
V_{SL}

■ Output saturation voltage-Output sink current ($\overline{\text{RESET}}$ pin)

Output saturation voltage V_{OL} (mV) vs Output sink current I_{OL} (mA)

Ta=75°C
Ta=25°C
Ta=−25°C

■ Output saturation voltage-Output sink current ($\overline{\text{RESET}}$ pin)

Output saturation voltage V_{OL} (mV) vs Output sink current I_{OL} (mA)
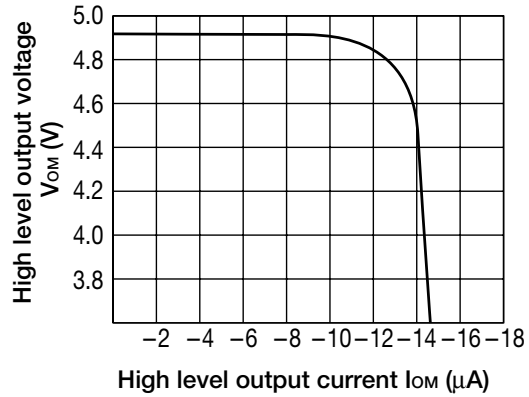
Ta=25°C
Ta=75°C
Ta=−25°C

■ High level output voltage-High level output current (RESET pin)

High level output voltage V_{OM} (V) vs High level output current I_{OM} (μA)

■ High level output voltage - High level output current ($\overline{\text{RESET}}$ pin)

High level output voltage V_{OM} (V) vs High level output current I_{OM} (μA)

■ Reset hold time temperature during power supply rise

V_{CC}=5V (Cr=0.1μF)

Reset hold time temperature during power supply rise T_{PR} (ms) vs Ambient temperature Ta (°C)

■ Watchdog timer monitoring time temperature

V_{CC}=5V (Cr=0.1μF)
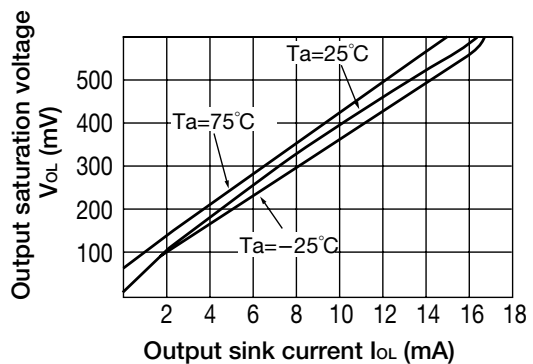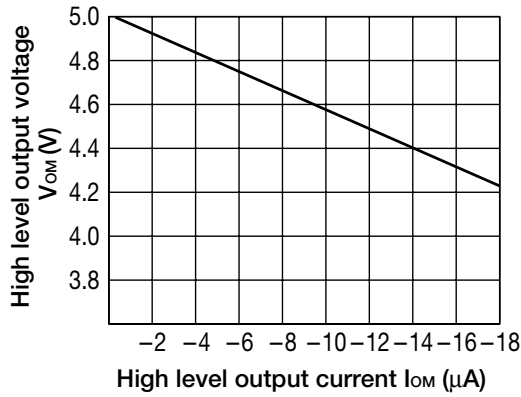
Watchdog timer monitoring time temperature T_{WD} (ms) vs Ambient temperature Ta (°C)
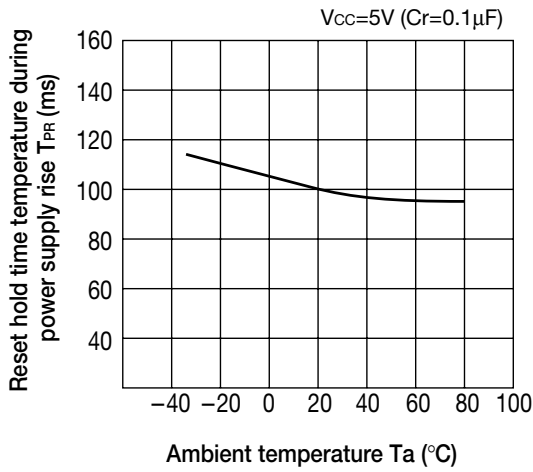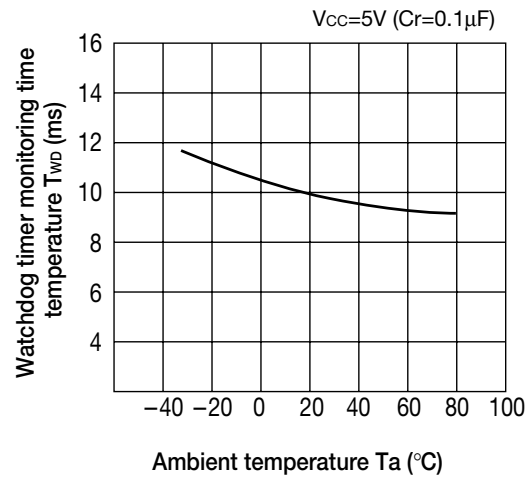
■ Reset time temperature (for watchdog timer)

V_{CC}=5V (Cr=0.1μF)

Reset time T_{WR} (ms) vs Ambient temperature Ta (°C)
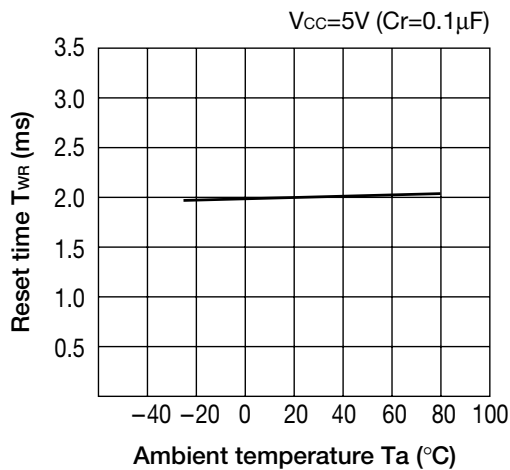
■ C_T value for reset hold time during power supply rise

Hold time T_{WD} (ms) vs C_T capacitance (μF)
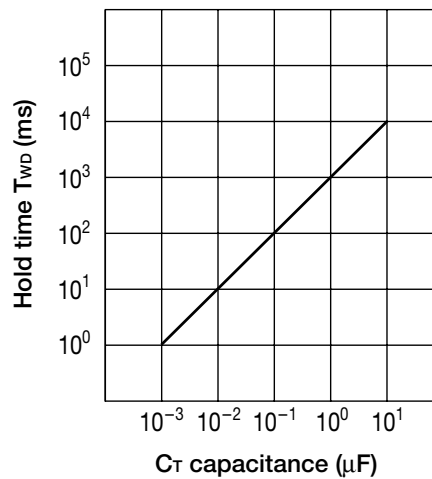
■ CT value for reset time (for watchdog timer)   ■ CT value for watchdog timer monitoring time

Reset time T_{WR} (ms)

10^3
10^2
10^1
10^0
10^{-1}
10^{-2}

10^{-3} 10^{-2} 10^{-1} 10^0 10^1

CT capacitance (μF)

Timer monitoring time T_{WD} (ms)

10^4
10^3
10^2
10^1
10^0
10^{-1}

10^{-3} 10^{-2} 10^{-1} 10^0 10^1

CT capacitance (μF)