# PLL520-05/-06/-07/-08/-09

## Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)

Universal Low Phase Noise IC's

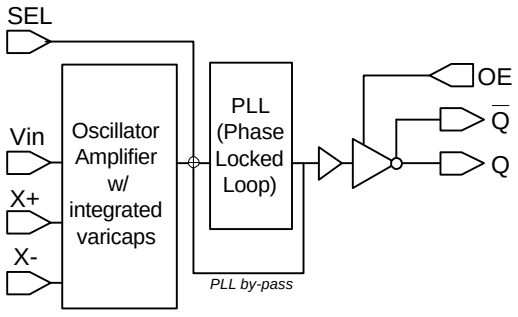
### FEATURES

- 120MHz to 200MHz Fundamental Mode Crystal.
- Output range: 120 – 200MHz (no multiplication), 240 – 400MHz (2x multiplier) or 480 – 700MHz (4x multiplier).
- High yield design support up to 2pF string capacitance at 200MHz.
- CMOS (Standard drive PLL520-07 or Selectoable Drive PLL520-06), PECL (Enable low PLL520-08 or Enable high PLL520-05) or LVDS output (PLL520-09).
- Integrated variable capacitors.
- Supports 3.3V-Power Supply.
- Available in 16-Pin (TSSOP or 3x3mm QFN)
  Note: PLL520-06 only available in 3x3mm.
  Note: PLL520-07 only available in TSSOP.

### DESCRIPTIONS

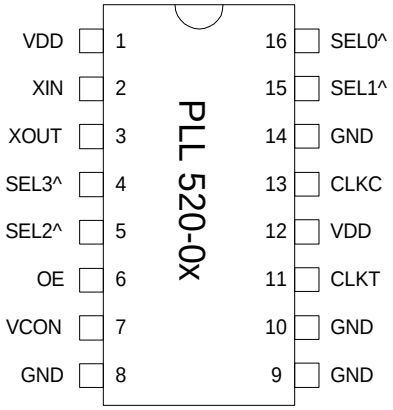
PLL520-05/-06/-07/-08/-09 are VCXO IC specifically designed to pull high frequency fundamental crystals. Their design was optimized to tolerate higher limits of interelectrodes capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. Its internal varicaps allow an on chip frequency pulling, controlled by the VCON input.

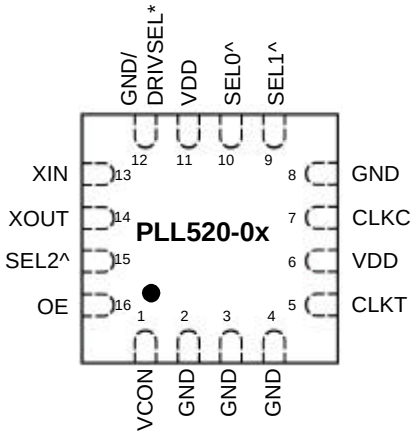
### BLOCK DIAGRAM




### PIN CONFIGURATION

(Top View)




^: Internal pull-up
*: PLL520-06 pin 12 is output drive select (DRIVSEL)
(0 for High Drive CMOS, 1 for Standard Drive CMOS)

### OUTPUT ENABLE LOGICAL LEVELS

| Part # | OE | State |
|---|---|---|
| PLL520-08 | 0 (Default) | Output enabled |
| | 1 | Tri-state |
| PLL520-05<br>PLL520-06<br>PLL520-07<br>PLL520-09 | 0 | Tri-state |
| | 1 (Default) | Output enabled |

OE input: Logical states defined by PECL levels for PLL520-08
Logical states defined by CMOS levels for PLL520-05/-06/-07/-09

## PIN DESCRIPTIONS

| Name | TSSOP* Pin number | 3x3mm QFN* Pin number | Type | Description |
|---|---|---|---|---|
| XIN | 2 | 13 | I | Crystal in connector. |
| XOUT | 3 | 14 | I | Crystal out connector. |
| OE | 6 | 16 | I | Output enable pin. |
| VCON | 7 | 1 | I | Frequency control input (0.3V to 3.0V) |
| GND | 8,9, 10, 14 | 2,3,4,8,12 | P | GND (except pin 12 on PLL520-06: DRIVSEL see below). |
| DRIVSEL** | - | 12 | I | PLL520-06 only: Drive Select Input. This pin has an internal pull-up that will default DRIVSEL to '1' when not connect to GND. CMOS output of PLL520-06 will be high drive CMOS when DRIVSEL is set to '0', and will be standard CMOS otherwise. |
| CLKT | 11 | 5 | O | True output PECL (PLL520-08) or LVDS (PLL520-09)<br>(N/C for PLL520-07) |
| CLKC | 13 | 7 | O | Complementary output PECL (PLL520-08) or LVDS (PLL520-09)<br>(CMOS out for PLL520-07). |
| SEL0 | 16 | 10 | I | Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND. |
| SEL1 | 15 | 9 | I | |
| SEL2 | 5 | 15 | I | |
| SEL3 | 4 | Not available | I | |
| VDD | 1, 12 | 6,11 | P | +3.3V VDD. |

***** Note: PLL520-06 only available in 3x3mm QFN, PLL520-07 only available in TSSOP.
** Note: DRIVSEL on pin 12 on PLL520-06 only.

## FREQUENCY SELECTION TABLE

| SEL3 | SEL2 | SEL1 | SEL0 | Selected Multiplier |
|---|---|---|---|---|
| 1 | 0 | 1 | 1 | Fin x 4 |
| 1 | 1 | 1 | 0 | Fin x 2 |
| 1 | 1 | 1 | 1 | No multiplication |

**Note:** SEL3 is not available (always "1") in 3x3mm package
All pins have internal pull-ups (default value is 1). Connect to GND to set to 0.

## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 7 | V |
| Input Voltage, dc | $V_I$ | $V_{SS}$-0.5 | $V_{DD}$+0.5 | V |
| Output Voltage, dc | $V_O$ | $V_{SS}$-0.5 | $V_{DD}$+0.5 | V |
| Storage Temperature | $T_S$ | -65 | 150 | °C |
| Ambient Operating Temperature* | $T_A$ | -40 | 85 | °C |
| Junction Temperature | $T_J$ | | 125 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| Input Static Discharge Voltage Protection | | | 2 | kV |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

### 2. Crystal Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| Built-in Capacitance | CX+ | 120MHz to 200MHz (VDD=3.3V) | | 2 | pF |
| | CX- | | | 2 | |
| Inter-electrode capacitance | $C_0$ | | | 2 | |
| C0/C1 ratio (gamma) | γ | | | 300 | - |
| Oscillation Frequency | OF | Fund. | 120 | 200 | MHz |

### 3. Voltage Control Crystal Oscillator

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| VCXO Stabilization Time * | $T_{VCXOSTB}$ | From power valid | | 10 | | ms |
| VCXO Tuning Range | | XTAL $C_0/C_1$ < 300 | 200* | | | ppm |
| CLK output pullability | | 0V ≤ VCON ≤ 3.3V, at room temp. | | ±100* | | ppm |
| On-chip Varicaps control range | | VCON = 0 to 3.3V | | 4 – 18* | | pF |
| Linearity | | | | 5* | 10* | % |
| VCXO Tuning Characteristic | | | | 65 | | ppm/V |
| VCON input impedance | | | | 60 | | kΩ |
| VCON modulation BW | | 0V ≤ VCON ≤ 3.3V, -3dB | 25 | | | kHz |

**Note:** Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

## 4. General Electrical Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Supply Current (Loaded Outputs) | $I_{DD}$ | PECL/LVDS/CMOS | | | 100/80/40 | mA |
| Operating Voltage | $V_{DD}$ | | 3.13 | | 3.47 | V |
| Output Clock Duty Cycle | | @ 1.4V (CMOS)<br>@ 1.25V (LVDS)<br>@ Vdd – 1.3V (PECL) | 45<br>45<br>45 | 50<br>50<br>50 | 55<br>55<br>55 | % |
| Short Circuit Current | | | | ±50 | | mA |

## 5. Jitter specifications

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Period jitter RMS | At 155.52MHz, with capacitive decoupling between VDD and GND. | | 4 | | ps |
| Period jitter peak-to-peak | | | 25 | | |
| Accumulated jitter RMS | At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles. | | 7* | | ps |
| Accumulated jitter peak-to-peak | | | 45* | | |
| Integrated jitter RMS at 155MHz | Integrated 12 kHz to 20 MHz | | 0.3 | | ps |

*: To be measured

## 6. Phase noise specifications

| PARAMETERS | FREQUENCY | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | UNITS |
|---|---|---|---|---|---|---|---|
| Phase Noise relative to carrier | 155.52MHz | -75 | -95 | -125 | -140 | -145 | dBc/Hz |
| | 622.08MHz | -75 | -95 | -110 | -125 | -120 | |

Note: Phase Noise measured at VCON = 0V

## 7. CMOS Output Electrical Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -12mA (Standard drive) | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{LO}$ = 12mA (Standard drive) | | | 0.4 | V |
| Output High Voltage at CMOS level | $V_{OHC}$ | $I_{OH}$ = -4mA (Standard drive) | $V_{DD}$– 0.4 | | | V |
| Output drive current | | At TTL level (High drive*) | 36 | 51 | | mA |
| | | At TTL level (Standard drive) | 12 | 17 | | mA |

* Note: High Drive CMOS is available on PLL520-06 through DRIVSEL selector input on pin 12.

## 8. CMOS Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Clock Rise/Fall Time (Standard Drive) | | 0.8V ~ 2.0V with 10 pF load | | 1.15 | | ns |
| | | 0.3V ~ 3.0V with 15 pF load | | 3.7 | | |
| Output Clock Rise/Fall Time (High Drive*) | | 0.8V ~ 2.0V with 10 pF load | | 0.5 | | |
| | | 0.3V ~ 3.0V with 15 pF load | | 1.5 | | |

* Note: High Drive CMOS is available on PLL520-06 through DRIVSEL selector input on pin 12.

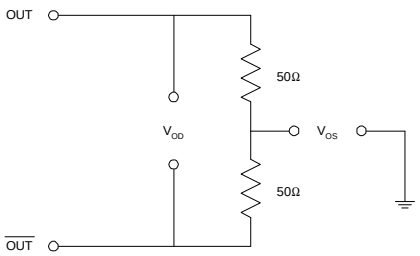
## 9. LVDS Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Differential Voltage | $V_{OD}$ | $R_L$ = 100 Ω (see figure) | 247 | 355 | 454 | mV |
| $V_{DD}$ Magnitude Change | $\Delta V_{OD}$ | | -50 | | 50 | mV |
| Output High Voltage | $V_{OH}$ | | | 1.4 | 1.6 | V |
| Output Low Voltage | $V_{OL}$ | | 0.9 | 1.1 | | V |
| Offset Voltage | $V_{OS}$ | | 1.125 | 1.2 | 1.375 | V |
| Offset Magnitude Change | $\Delta V_{OS}$ | | 0 | 3 | 25 | mV |
| Power-off Leakage | $I_{OXD}$ | $V_{out}$ = $V_{DD}$ or GND, $V_{DD}$ = 0V | | ±1 | ±10 | uA |
| Output Short Circuit Current | $I_{OSD}$ | | | -5.7 | -8 | mA |

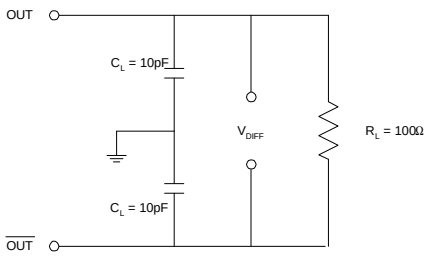
## 10. LVDS Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Differential Clock Rise Time | $t_r$ | $R_L$ = 100 Ω, $C_L$ = 10 pF (see figure) | 0.2 | 0.7 | 1.0 | ns |
| Differential Clock Fall Time | $t_f$ | | 0.2 | 0.7 | 1.0 | ns |

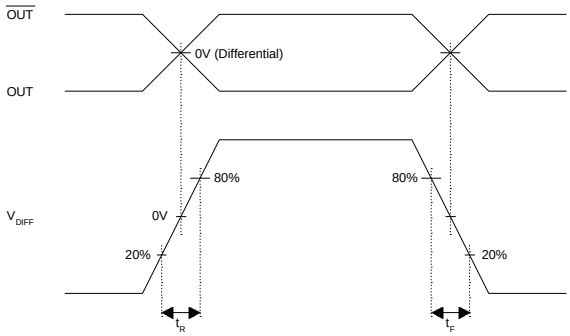
LVDS Levels Test Circuit




LVDS Switching Test Circuit




LVDS Transistion Time Waveform



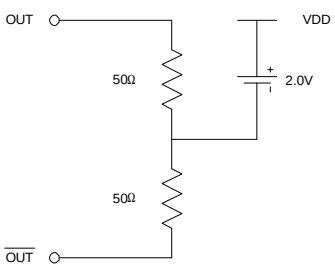
## 11. PECL Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | MAX. | UNITS |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $R_L$ = 50 Ω to ($V_{DD}$ – 2V) (see figure) | $V_{DD}$ – 1.025 | | V |
| Output Low Voltage | $V_{OL}$ | | | $V_{DD}$ – 1.620 | V |

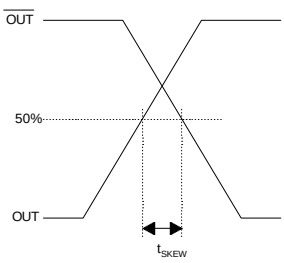
## 12. PECL Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Clock Rise Time | $t_r$ | @20/80% - PECL | | 0.6 | 1.5 | ns |
| Clock Fall Time | $t_f$ | @80/20% - PECL | | 0.5 | 1.5 | ns |

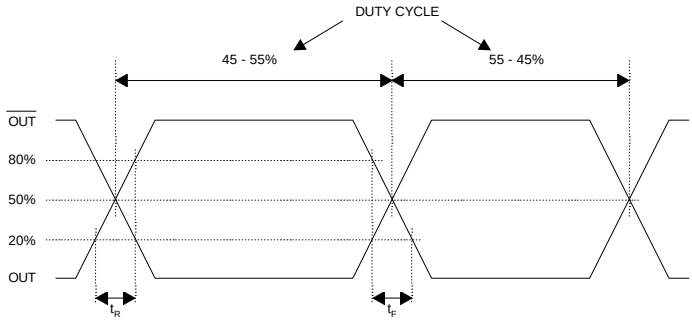
PECL Levels Test Circuit




PECL Output Skew



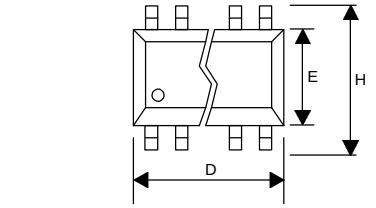

PECL Transistion Time Waveform

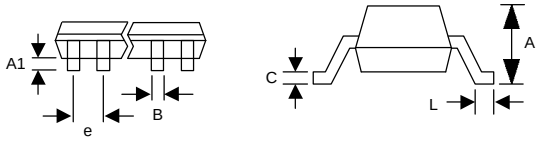


## PACKAGE INFORMATION

16 PIN Narrow SOIC, TSSOP ( mm )

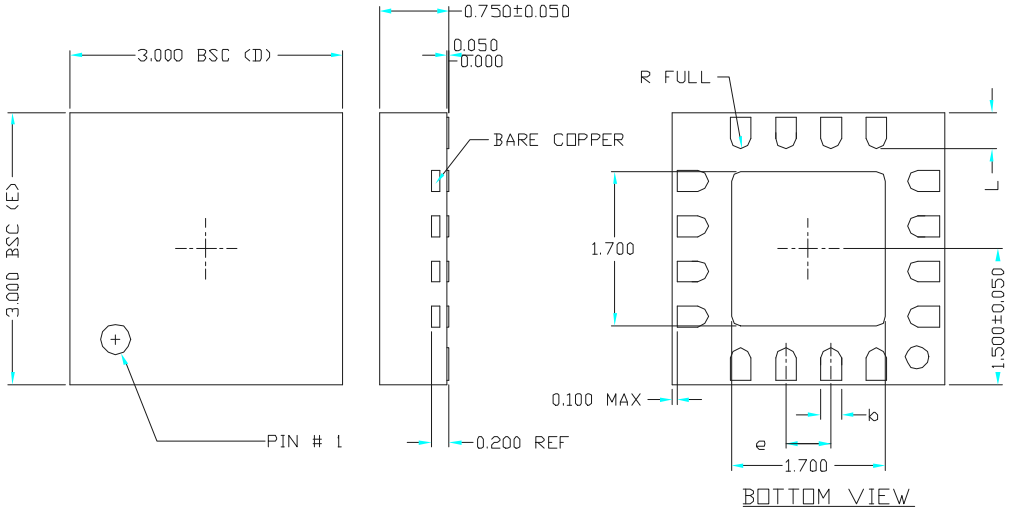
| | SOIC | | TSSOP | |
|---|---|---|---|---|
| Symbol | Min. | Max. | Min. | Max. |
| A | 1.35 | 1.75 | - | 1.20 |
| A1 | 0.10 | 0.25 | 0.05 | 0.15 |
| B | 0.33 | 0.51 | 0.19 | 0.30 |
| C | 0.19 | 0.25 | 0.09 | 0.20 |
| D | 9.80 | 10.00 | 4.90 | 5.10 |
| E | 3.80 | 4.00 | 4.30 | 4.50 |
| H | 5.80 | 6.20 | 6.40 BSC | |
| L | 0.40 | 1.27 | 0.45 | 0.75 |
| e | 1.27 BSC | | 0.65 BSC | |




VARIATIONS:

| SYMBOL | 16 LD | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| e | 0.50 BSC | | |
| b | 0.18 | 0.23 | 0.30 |
| L | 0.30 | 0.40 | 0.50 |
| ND | 4 | | |
| NE | 4 | | |



## ORDERING INFORMATION

***For part ordering, please contact our Sales Department:***

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

***PART NUMBER***

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

**PLL520-0x O C**

*PART NUMBER*

TEMPERATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
O=TSSOP O=OFN