

**Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)**

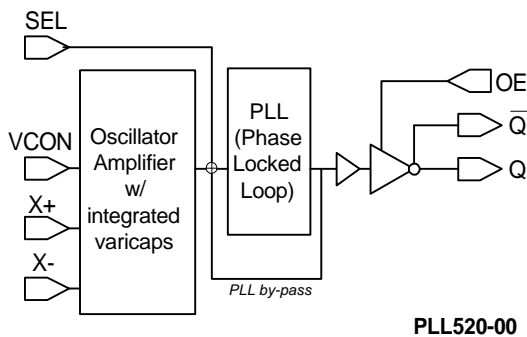
**FEATURES**

- 120MHz to 200MHz Fundamental Mode Crystal.
- Output range: 120 – 200MHz (no multiplication), 240 – 400MHz (2x multiplier) or 480 – 700MHz (4x multiplier).
- Available outputs: PECL, LVDS, or CMOS.
- Selectable OE Logic (enable high or enable low).
- Integrated variable capacitors.
- Supports 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

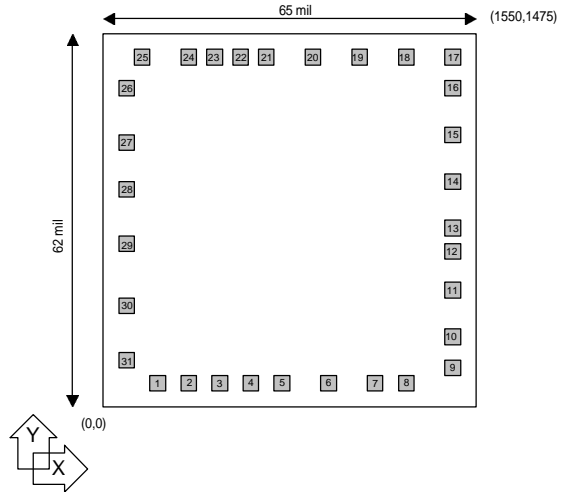
**DESCRIPTIONS**

PLL520-00 is a VCXO IC specifically designed to pull high frequency fundamental crystals. Its design was optimized to tolerate higher limits of interelectrodes capacitance and bonding capacitance to improve yield. It achieves very low current into the crystal resulting in better overall stability. Its internal varicaps allow an on chip frequency pulling, controlled by the VCON input.

**BLOCK DIAGRAM**



**DIE CONFIGURATION**



**DIE SPECIFICATIONS**

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

**OUTPUT SELECTION AND ENABLE**

Pad #18 OUTSEL1	Pad #25 OUTSEL0	Selected Output
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	LVDS
1	1	PECL (default)

OE_SELECT (Pad #9)	OE_CTRL (Pad #30)	State
0	0	Tri-state
	1 (Default)	Output enabled
1 (Default)	0 (Default)	Output enabled
	1	Tri-state

Pad #9, 18, 25: Bond to GND to set to "0", bond to VDD to set to "1"  
 No connection results to "default" setting through internal pull-up/-down.  
 Pad #30: Logical states defined by PECL levels if OE\_SELECT (pad #9) is "1"  
 Logical states defined by CMOS levels if OE\_SELECT is "0"

## Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)

### FREQUENCY SELECTION TABLE

Pad #28 SEL3	Pad #29 SEL2	Pad #19 SEL1	Pad #20 SEL0	Selected Multiplier
1	0	1	1	Fin x 4
1	1	1	0	Fin x 2
1	1	1	1	No multiplication (no PLL)

All pads have internal pull-ups (default value is 1). Bond to GND to set to 0.

### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		7	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

#### 2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	120		200	MHz
Crystal Loading Rating	$C_L (xtal)$	Die at VCON = 1.65V		4		pF
Interelectrode Capacitance	$C_0$				3.5	pF
Crystal Pullability	$C_0/C_1 (xtal)$	AT cut			300	-
Recommended ESR	$R_E$	AT cut			30	$\Omega$

## Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)

### 3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid		10		ms
VCXO Tuning Range		XTAL $C_0/C_1 < 300$	200*			ppm
CLK output pullability		$0V \leq VCON \leq 3.3V$ at room temperature		$\pm 100^*$		ppm
On-chip Varicaps control range		$VCON = 0$ to 3.3V		4 – 18*		pF
Linearity				5*	10*	%
VCXO Tuning Characteristic				65		ppm/V
VCON input impedance				60		$k\Omega$
VCON modulation BW		$0V \leq VCON \leq 3.3V, -3dB$	25			kHz

Note: Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

### 4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	$I_{DD}$	PECL/LVDS/CMOS			100/80/40	mA
Operating Voltage	$V_{DD}$		3.13		3.47	V
Output Clock Duty Cycle		@ 1.4V (CMOS) @ 1.25V (LVDS) @ $V_{dd} - 1.3V$ (PECL)	45 45 45	50 50 50	55 55 55	%
Short Circuit Current				$\pm 50$		mA

**Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)**
**5. Jitter specifications**

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		2.5		ps
Period jitter peak-to-peak			18.5	20	
Accumulated jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.5		ps
Accumulated jitter peak-to-peak			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.5		ps
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.3	0.4	ps
Period jitter RMS	At 622.08MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		11		ps
Period jitter peak-to-peak			45	49	
Accumulated jitter RMS	At 622.08MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		11		ps
Accumulated jitter peak-to-peak			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		3		ps
Integrated jitter RMS at 622MHz	Integrated 12 kHz to 20 MHz		1.6	1.8	ps

Measured on Wavecrest SIA 3000

**6. Phase noise specifications**

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	155.52MHz	-75	-95	-125	-140	-145	dBc/Hz
	622.08MHz	-75	-95	-110	-125	-120	

Note: Phase Noise measured at VCON = 0V

**Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)**
**7. CMOS Output Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$I_{OH} = -12\text{mA}$ (Standard drive)	2.4			V
Output Low Voltage	$V_{OL}$	$I_{LO} = 12\text{mA}$ (Standard drive)			0.4	V
Output High Voltage at CMOS level	$V_{OHC}$	$I_{OH} = -4\text{mA}$ (Standard drive)	$V_{DD} - 0.4$			V
Output drive current		At TTL level (High drive)	36	51		mA
		At TTL level (Standard drive)	12	17		mA

**8. CMOS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Clock Rise/Fall Time (Standard Drive)		0.8V ~ 2.0V with 10 pF load		1.15		ns
		0.3V ~ 3.0V with 15 pF load		3.7		
Output Clock Rise/Fall Time (High Drive)		0.8V ~ 2.0V with 10 pF load		0.5		
		0.3V ~ 3.0V with 15 pF load		1.5		

**Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)**

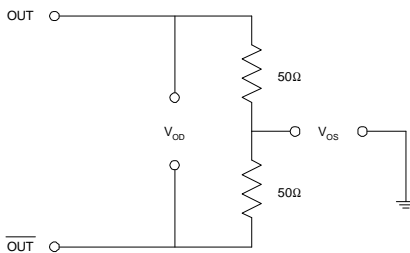
**9. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

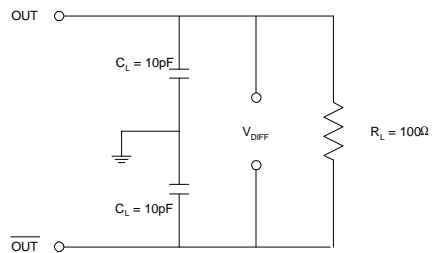
**10. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

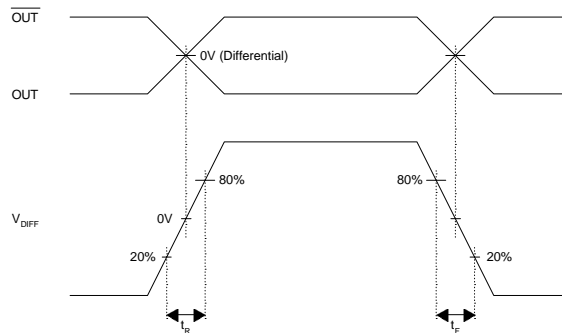
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



**Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)**

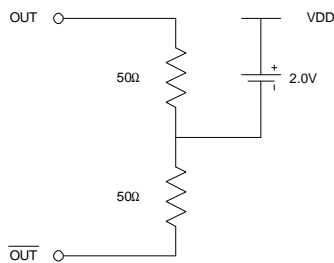
**11. PECL Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	$V_{OL}$			$V_{DD} - 1.620$	V

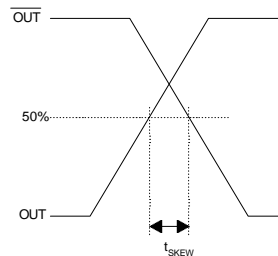
**12. PECL Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	$t_r$	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	$t_f$	@80/20% - PECL		0.5	1.5	ns

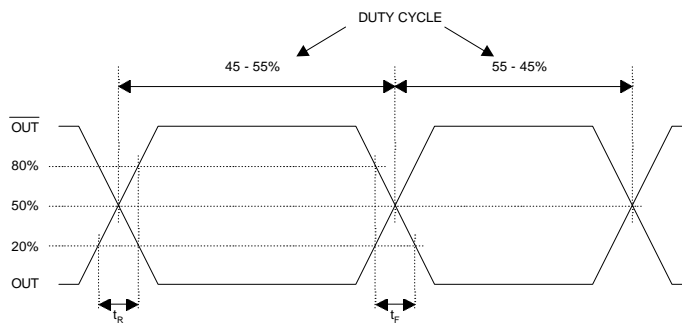
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



**Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)**
**PAD ASSIGNMENT**

Pad #	Name	X (μm)	Y (μm)
1	GND	248	109
2	GND	361	109
3	GND	473	109
4	GND	587	109
5	GND	702	109
6	N/C	874	109
7	GND	1042	109
8	GNDBUF	1171	109
9	OE_SELECT	1400	125
10	LVDS	1400	259
11	PECL	1400	476
12	VDDBUF	1400	616
13	VDDBUF	1400	716
14	PECLB	1400	871
15	LVDSB	1400	1089
16	CMOS	1400	1227
17	GNDBUF	1389	1365
18	OUTSEL1	1232	1365
19	SEL1	1042	1365
20	SEL0	854	1365
21	VDD	659	1365
22	VDD	559	1365
23	VDD	459	1365
24	VDD	358	1365
25	OUTSEL0	194	1365
26	XIN	109	1223
27	XOUT	109	1017
28	SEL3	109	858
29	SEL2	109	646
30	OE_CTRL	109	397
31	VCON	109	181



**Low Phase Noise VCXO with multipliers (for 120-200MHz Fund Xtal)**

**ORDERING INFORMATION**

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range

**PLL520-00**    **DC - D1**

<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
P520-00DC-D1	PLL520-00DC-D1	Die – Waffle Pack

*PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.*

**LIFE SUPPORT POLICY:** *PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.*