

750kHz – 400MHz Low Phase Noise VCXO (for 12 – 25MHz Crystals)

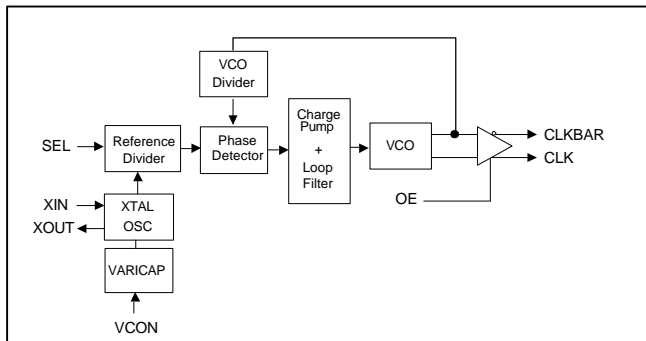
FEATURES

- 750kHz to 400MHz output range.
- Low phase noise output (@ 10kHz frequency offset, -140dBc/Hz for 19.44MHz, -127dBc/Hz for 106.25MHz, -125dBc/Hz for 155.52MHz).
- Selectable CMOS, PECL and LVDS output.
- 12 to 25MHz crystal input.
- No external load capacitor or varicap required.
- Output Enable selector.
- Wide pull range (+/-190 ppm)
- 3.3V operation.
- Available in DIE (65 mil x 62 mil).

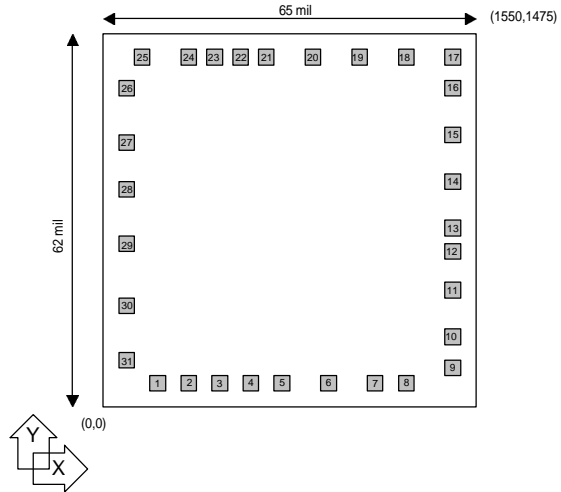
DESCRIPTIONS

The PLL502-10 is a monolithic low jitter and low phase noise (-140dBc/Hz @ 10kHz offset) VCXO IC Die, with CMOS, LVDS and PECL output, covering the 750kHz to 400MHz output range. It allows the control of the output frequency with an input voltage (VCON), using a low cost crystal. The same die can be used as a VCXO with output frequencies ranging from $F_{XIN} / 16$ to $F_{XIN} \times 16$ thanks to frequency selector pads. This makes the PLL502-10 ideal as a universal die for applications ranging from ADSL to SONET.

BLOCK DIAGRAM



DIE CONFIGURATION



DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

OUTPUT SELECTION AND ENABLE

Pad #18 OUTSEL1	Pad #25 OUTSEL0	Selected Output
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	PECL
1	1	LVDS

OE_SELECT (Pad #9)	OE_CTRL (Pad #30)	State
0	0 (Default)	Output enabled
	1	Tri-state
1 (Default)	0	Tri-state
	1 (Default)	Output enabled

Pad #9: Bond to GND to set to "0", bond to VDD to set to "1"
 Pad #30: Logical states defined by PECL levels if OE_SELECT (pad #9) is "0"
 Logical states defined by CMOS levels if OE_SELECT is "1"

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FREQUENCY SELECTION TABLE

Pad #28 SEL3	Pad #29 SEL2	Pad #19 SEL1	Pad #20 SEL0	Selected Multiplier
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Fin / 8
0	1	1	1	Fin x 2
1	0	0	0	Reserved
1	0	0	1	Fin / 2
1	0	1	0	Fin / 16
1	0	1	1	Fin x 4
1	1	0	0	Fin / 4
1	1	0	1	Fin x 8
1	1	1	0	Fin x 16
1	1	1	1	No multiplication

All pads have internal pull-ups (default value is 1). Bond to GND to set to 0.

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ELECTRICAL SPECIFICATIONS
1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_L (x_{tal})$	at $V_{CON} = 1.65V$		9.5		pF
Crystal Pullability	$C_0/C_1 (x_{tal})$	AT cut			250	-
Recommended ESR	R_E	AT cut			30	Ω

Note: Crystal Loading rating: 9.5pF is the loading the crystal sees from the VCXO chip at $V_{CON} = 1.65V$. It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid		10		ms
VCXO Tuning Range		$F_{XIN} = 12 - 25MHz$; $XTAL C_0/C_1 < 250$	380			ppm
CLK output pullability		$0V \leq V_{CON} \leq 3.3V$	± 190			ppm
Linearity				5	10	%
VCXO Tuning Characteristic				115		ppm/V
V_{CON} input impedance			2000			$k\Omega$
V_{CON} modulation BW		$0V \leq V_{CON} \leq 3.3V, -3dB$	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

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4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Supply Current, Dynamic (with Loaded Outputs)	I _{DD}	PECL/LVDS/CMOS	F _{out} < 24MHz			25/25/15	mA
			24MHz < F _{out} < 96MHz			65/45/30	
			96MHz < F _{out} < 400MHz			100/80/40	
Operating Voltage	V _{DD}		3.13		3.47	V	
Output Clock Duty Cycle		@ 1.4V (CMOS)	45	50	55	%	
		@ 1.25V (LVDS)	45	50	55		
		@ V _{dd} – 1.3V (PECL)	45	50	55		
Short Circuit Current				±50		mA	

5. Jitter specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND.	19.44MHz		5		ps
		77.76MHz		8		
		155.52MHz		9		
Accumulated jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	155.52MHz		TBM		ps
Integrated jitter RMS	Integrated 12 kHz to 20 MHz	155.52MHz		3	4	ps

6. Phase noise specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	19.44MHz	-60	-90	-112	-140	-150	dBc/Hz
	106.25MHz	-60	-90	-112	-127	-125	
	155.52MHz	-60	-90	-112	-125	-123	

Note: Phase Noise measured at VCON = 0V

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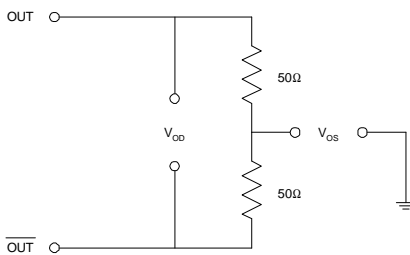
7. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

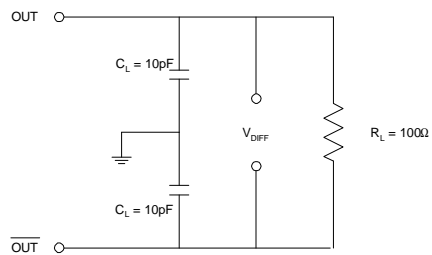
8. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

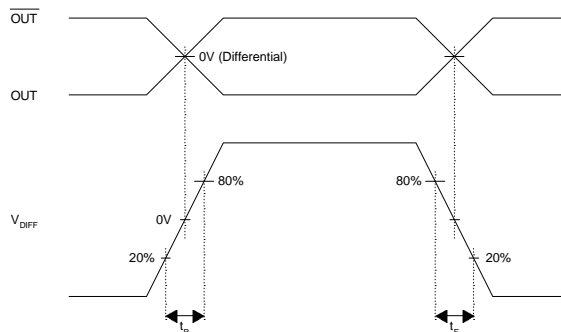
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



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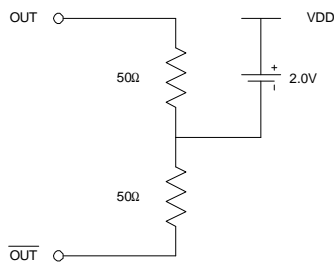
9. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	V_{OL}			$V_{DD} - 1.620$	V

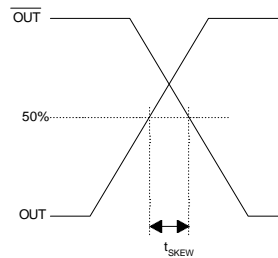
10. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

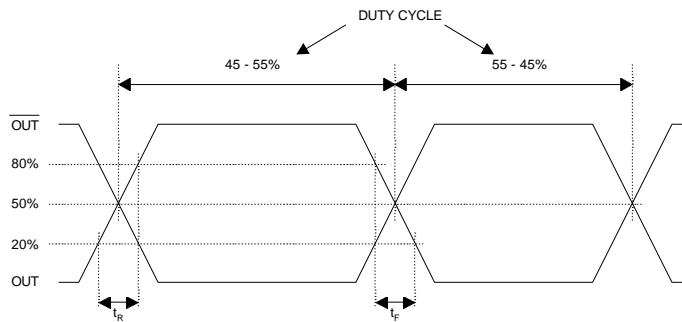
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



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PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)
1	GND	248	109
2	GND	361	109
3	GND	473	109
4	GND	587	109
5	GND	702	109
6	N/C	874	109
7	GND	1042	109
8	GNDBUF	1171	109
9	OE_SELECT	1400	125
10	LVDS	1400	259
11	PECL	1400	476
12	VDDBUF	1400	616
13	VDDBUF	1400	716
14	PECLB	1400	871
15	LVDSB	1400	1089
16	CMOS	1400	1227
17	GNDBUF	1389	1365
18	OUTSEL1	1232	1365
19	SEL1	1042	1365
20	SEL0	854	1365
21	VDD	659	1365
22	VDD	559	1365
23	VDD	459	1365
24	VDD	358	1365
25	OUTSEL0	194	1365
26	XIN	109	1223
27	XOUT	109	1017
28	SEL3	109	858
29	SEL2	109	646
30	OE_CTRL	109	397
31	VCON	109	181

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ORDERING INFORMATION

For part ordering, please contact our Sales Department:

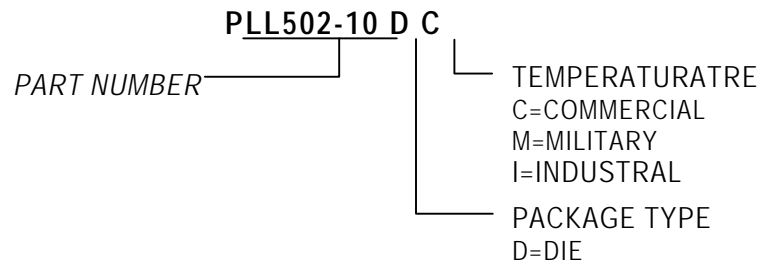
47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range



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