CY22800

Universal Programmable Clock Generator (UPCG)

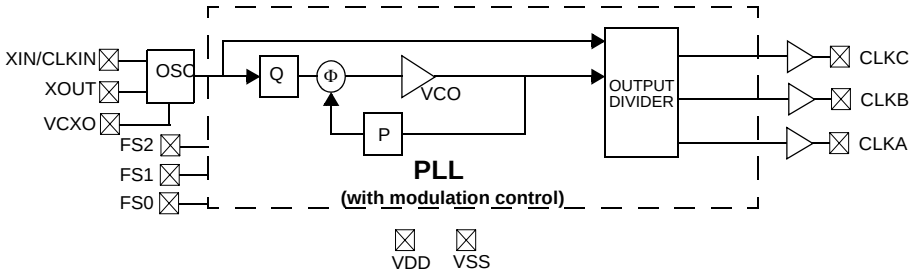
Features

- Spread Spectrum, VCXO, and Frequency Select
- Input frequency range:
  - — Crystal: 8–30 MHz
  - — CLKIN: 0.5–100 MHz
- Output frequency:
  - — LVCMOS: 1–200 MHz
- Integrated phase-locked loop
- Low jitter, high accuracy outputs
- 3.3V operation
- 8-pin SOIC package

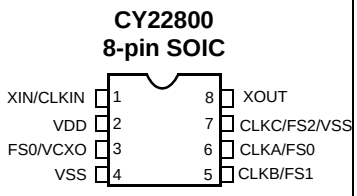
Benefits

- Make inventory of only one device, CY22800, to use in various applications such as HDTV, STB, DVDR, etc.
- Multiple predefined configurations that can be programmed into a single chip
- Eliminates the need for expensive and difficult to use higher-order crystal
- High-performance PLL tailored for multiple applications
- Meets critical timing requirements in complex system designs
- Enables application compatibility
- Allows up to three different frequency selects

Logic Block Diagram



Pin Configuration



Pin Description

Name	Pin Number	Description
XIN	1	Reference Input; Crystal or External Clock
VDD	2	3.3V Voltage Supply
FS0/VCXO	3	Frequency Select 0/VCXO Analog Control Voltage[1]
VSS	4	Ground
CLKB/FS1	5	Clock Output B/Frequency Select 1[1]
CLKA/FS0	6	Clock Output A/Frequency Select 0[1]
CLKC/FS2/VSS	7	Clock Output C/Frequency Select 2/VSS[1]
XOUT	8	Reference Output (No Connect when the reference is a clock)

Note
1. Pin definition changes for different configurations. Refer to the specific one-page data sheet for more details.

General Description

The CY22800 is a multi-function clock generator that supports various applications in consumer and communications markets. The device uses the Cypress proprietary PLL along with Spread Spectrum and VCXO technology to make it one of the most versatile clock synthesizer in the market place. The CY22800 is a field-programmable synthesizer that can be programmed using an easy-to-use programmer dongle, CY36800, with one of many predefined configuration files for fast sample generation of prototype builds. The CY22800 is a reprogrammable device that can be programmed up to five thousand times. The latest configurations available for this device are summarized in *Table 1*.

Spread Spectrum Clock Generation (SSCG)

The CY22800 is capable of generating Spread Spectrum Clocks (SSCG) for the purpose of reducing EMI found in today's high-speed digital electronic systems.

The device uses proprietary Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By modulating the frequency of the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency (EMC) requirements and improve time-to-market without degrading system performance.

The CY22800 uses a preprogrammed configuration of memory arrays to synthesize output frequency and offers eight different spread percentages (refer to *Table 1* – Code numbers -015 to -022), and an additional option to turn the spread on and off.

For the above-mentioned configurations, the modulation frequency varies with the reference frequency as follows:

$$f_{mod} = \frac{f_{ref}}{1000}$$

VCXO

One of the key components of the CY22800 device is the VCXO. The VCXO is used to "pull" the reference crystal higher or lower in order to lock the system frequency to an external source. This is ideal for applications where the output frequency needs to track along with an external reference frequency that is constantly shifting.

A special pullable crystal must be used in order to have adequate VCXO pull range. Pullable Crystal specifications are included in this data sheet.

VCXO Profile

Figure 1 shows an example of what a VCXO profile looks like. The analog voltage input is on the X-axis and the PPM range is on the Y-axis. An increase in the VCXO input voltage results in a corresponding increase in the output frequency. This has the effect of moving the PPM from a negative to positive offset.

Figure 1. VCXO Profile

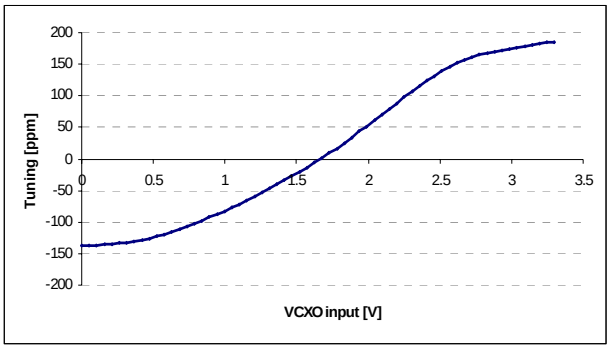


Table 1. CY22800 Configurations

Base part #	Code #	Code name	Input freq. (MHz)	Output freq. (MHz)	SS	VCXO
CY22800	001A	X2 multiplier	CLKIN: 0.5 - 100.0 XTAL: 8.0 - 30.0	CLKA: 1.0 - 200.0	N	N

Cypress offers a wide range of programmable clock synthesizers that can be used to generate any other frequencies not covered by the CY22800. *Table 2* summarizes all Cypress programmable devices including CY22800.

Table 2. Cypress Programmable Clocks[2]

Part #	No. of PLL	Input Freq.	Output Freq.	Package	No. of Outputs	Spread Spectrum	VCXO	I^2C
CY22800	1	0.5–100	1–200	8-SOIC	up to 3	Yes	Yes	No
CY22050	1	1–133	0.08–200	16-TSSOP	up to 6	No	No	No
CY22150	1	1–133	0.08–200	16-TSSOP	up to 6	No	No	Yes
CY25100	1	8–166	3–200	8-SOIC/TSSOP	up to 2	Yes	No	No
CY25200	1	3–166	3–200	16-TSSOP	up to 6	Yes	No	No
CY241V08	1	27/13.5	27/13.5	8-SOIC	up to 2	No	Yes	No
CY22392	3	1–166	1–200	16-TSSOP	up to 6	No	No	No
CY22381	3	1–166	1–200	8-SOIC	up to 3	No	No	No
CY22393	3	1–166	1–200	16-TSSOP	up to 6	No	No	Yes
CY22394/5	3	1–166	1–200	16-TSSOP	up to 5	No	No	No
CY22388/89/91	4	1–100	4.2–166	16/20-TSSOP, 32-QFN	up to 8	No	Yes	No

Note
2. The CY3672 programmer can be used to program all Cypress chips. Refer to the CY3672 data sheet for programming procedures.

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	4.6	V
T_S	Storage Temperature	–65	125	°C
T_J	Junction Temperature	–	125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electro-Static Discharge	2	–	kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.14	3.3	3.47	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Max. Load Capacitance on the CLK output	–	–	15	pF
f_{REF}[3]	Reference Frequency	0.5	–	100	MHz
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

Pullable Crystal Specifications for VCXO Application ONLY

Parameter	Name	Min.	Typ.	Max.	Unit
C_{LNOM}	Crystal Load Capacitance	–	14	–	pF
R_1	Equivalent Series Resistance	–	–	25	Ω
R_3/R_1	Ratio of Third Overtone Mode ESR to Fundamental Mode ESR. Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	–
DL	Crystal Drive Level. No external series resistor assumed	–	0.5	2	mW
F_{3SEPHI}	Third overtone separation from 3*F_{NOM} (High Side)	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from 3*F_{NOM} (Low Side)	–	–	–150	ppm
C0	Crystal shunt capacitance			7	pF
C0/C1	Ratio of Shunt to motional capacitance	180	–	250	
C_1	Crystal motional capacitance	14.4	18	21.6	pF

Recommended Crystal Specifications for ALL other Applications

Parameter	Name	Description	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, and AT cut	8	–	30	MHz
C_{LNOM}	Nominal Load Capacitance		–	12	–	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode	–	35	50	Ω
DL	Crystal Drive Level	No external series resistor assumed	–	0.5	2	mW

Note
3. Configuration dependent, see the one-page document.

DC Electrical Specifications

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$ (source)	12	24	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$ (sink)	12	24	–	mA
C_{IN1}	Input Capacitance	All input pins except XIN and XOUT	–	–	7	pF
C_{IN2}	Input Capacitance	XIN and XOUT pins	–	24	–	pF
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	–	5	10	µA
I_{IL}	Input Low Current	$V_{IL} = 0V$	–	–	50	µA
$f_{\Delta XO}$	VCXO Pullability Range		±150	–		ppm
V_{VCXO}	VCXO Input Range		0	–	V_{DD}	V
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	–	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3	V_{DD}

AC Electrical Characteristics (V_{DD} = 3.3V)

Parameter	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 3*, 50% of V_{DD}	45	50	55	%
t_3	Rising Edge Slew Rate	Output Clock Rise Time, 20% - 80% of V_{DD}	0.8	1.4	–	V/ns
t_4	Falling Edge Slew Rate	Output Clock Fall Time, 80% - 20% of V_{DD}	0.8	1.4	–	V/ns
t_{10}	PLL Lock Time		–	–	3	ms

Test Circuit

Figure 2. Test Circuit Diagram

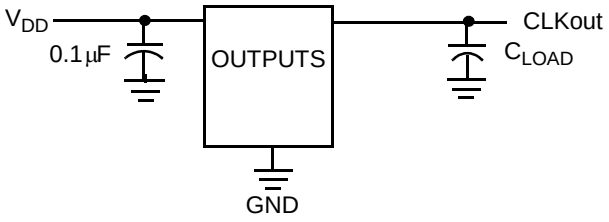


Figure 4. Rise and Fall Time Definitions

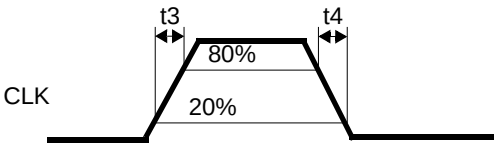
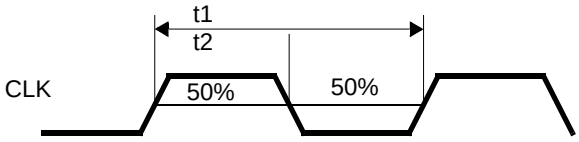


Figure 3. Duty Cycle Definition; DC = t2/t1

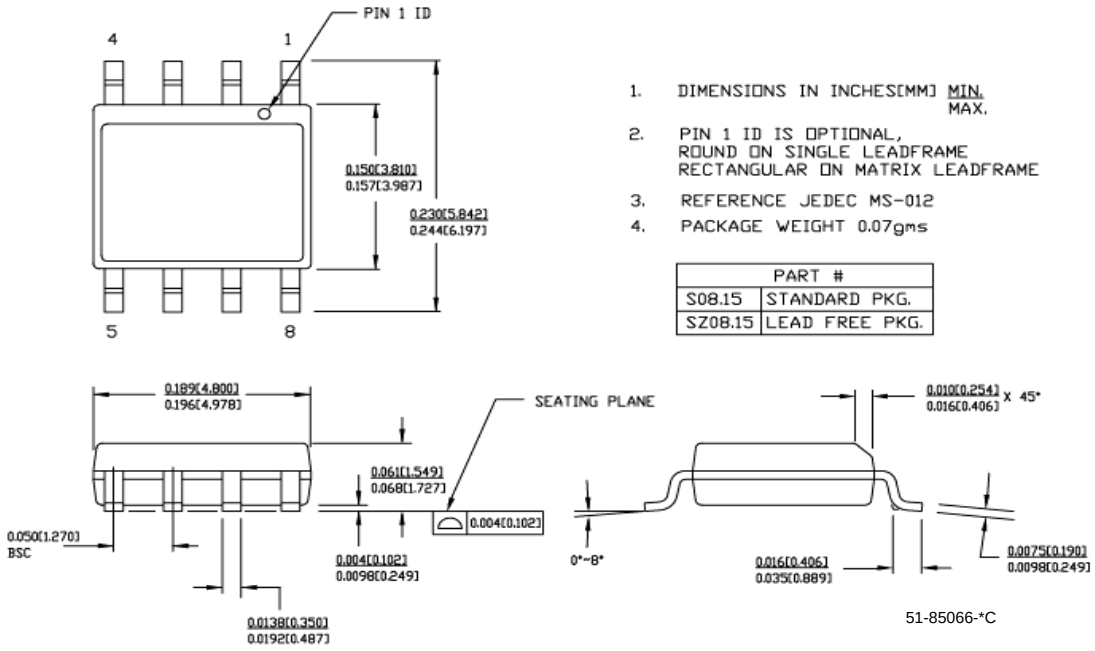


Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY22800FXC	8-Pin SOIC	Commercial	3.3V

Package Diagram

Figure 5. 8-Lead (150-Mil) SOIC S8



Document History Page

Document Title: CY22800 Universal Programmable Clock Generator (UPCG) Document Number: 001-07704				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	478688	See ECN	KKVTMP	New data sheet