Low Phase Noise VCXO (17MHz to 36MHz)

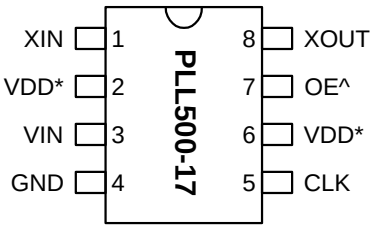
FEATURES

- VCXO output for the 17MHz to 36MHz range
- Low phase noise (-130 dBc @ 10kHz offset at 35.328MHz).
- CMOS output with OE tri-state control.
- 17 to 36MHz fundamental crystal input.
- Integrated high linearity variable capacitors.
- 12mA drive capability at TTL output.
- +/- 150 ppm pull range, max 5% linearity.
- Low jitter (RMS): 2.5ps period jitter.
- 2.25V to 3.63V DC operation.
- Available in 8-Pin SOIC or DIE.

DESCRIPTION

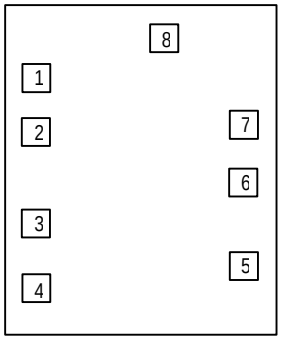
The PLL500-17 is a low cost, high performance and low phase noise VCXO for the 17 to 36MHz range, providing less than -130dBc at 10kHz offset at 35.328MHz. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. Input crystal can range from 17 to 36MHz (fundamental resonant mode).

PIN CONFIGURATION



^: Denotes internal Pull-up
*: Only one VDD pin needs to be connected

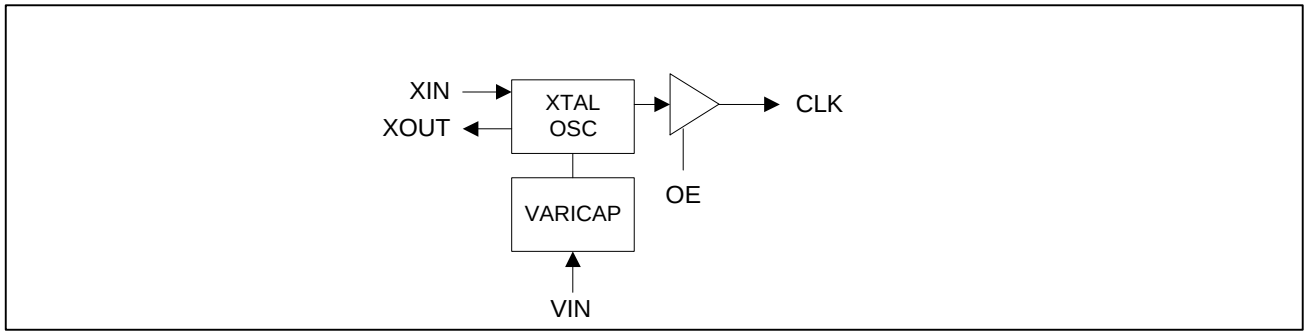
DIE PAD LAYOUT



FREQUENCY RANGE

MULTIPLIER	FREQUENCY	OUTPUT BUFFER
1x	17 – 36 MHz	CMOS

BLOCK DIAGRAM



PIN AND PAD DESCRIPTION

Name	Pin#	Die Pad Position		Type	Description
		X (μm)	Y (μm)		
XIN	1	94.183	768.599	I	Crystal input pin.
VDD	2,6	94.157	605.029	P	+3.3V VDD power supply pin. Only one VDD pin is necessary.
VIN	3	94.183	331.756	I	Frequency control voltage input pin.
GND	4	94.193	140.379	P	Ground pin.
CLK	5	715.472	203.866	O	Output clock pin.
VDD	2,6	715.307	455.726	P	+3.3V VDD power supply pin. Only one VDD pin is necessary.
OE	7	715.472	626.716	I	Output Enable input pin. Tri-states output if set to '0'. Enables output if set to '1'. Internal pull-up.
XOUT	8	715.472	888.881	I	Crystal output pin.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{CC}+0.5	V
Output Voltage Range	V_O	-0.5	V_{CC}+0.5	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		0	70	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			17		36	MHz
Output Clock Rise/Fall Time		0.8V ~ 2.0V with 10 pF load		1.15		ns
		0.3V ~ 3.0V with 15 pF load		3.7		
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%
Short Circuit Current				±50		mA

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid		10		ms
VCXO Tuning Range		F_{XIN} = 17 – 36MHz; XTAL C_0/C_1 < 250	300			ppm
CLK output pullability		0V ≤ VIN ≤ 3.3V	±150			ppm
VCXO Tuning Characteristic				100		ppm/V
Pull range linearity					5	%
Power Supply Rejection	PWSRR	Frequency change with Vdd varied +/- 10%	-1		+1	ppm
VIN pin input impedance			1000			kΩ
VIN modulation BW		0V ≤ VIN ≤ 3.3V, -3dB	45			kHz

Note: Preliminary Specifications still to be characterized. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. Jitter and Phase Noise specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	with capacitive decoupling between VDD and GND.		2.5		ps
Phase Noise relative to carrier	36MHz @100Hz offset		-80		dBc/Hz
Phase Noise relative to carrier	36MHz @1kHz offset		-110		dBc/Hz
Phase Noise relative to carrier	36MHz @10kHz offset		-130		dBc/Hz
Phase Noise relative to carrier	36MHz @100kHz offset		-138		dBc/Hz
Phase Noise relative to carrier	36MHz @1MHz offset		-145		dBc/Hz

Note: Preliminary Specifications still to be characterized.

5. DC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	F_{XIN} = 36MHz Ouput load of 15pF		5	6	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output High Voltage	V_{OH}	I_{OH} = -12mA	2.4			V
Output Low Voltage	V_{OL}	I_{LO} = 12mA			0.4	V
Output High Voltage at CMOS level	V_{OHC}	I_{OH} = -4mA	V_{DD} – 0.4			V
Output drive current		At TTL level	12	17		mA
Short Circuit Current				±50		mA
VCXO Control Voltage	VIN		0		3.3	V
ESD Protection		Human Body Model	3000			

6. Crystal Specifications

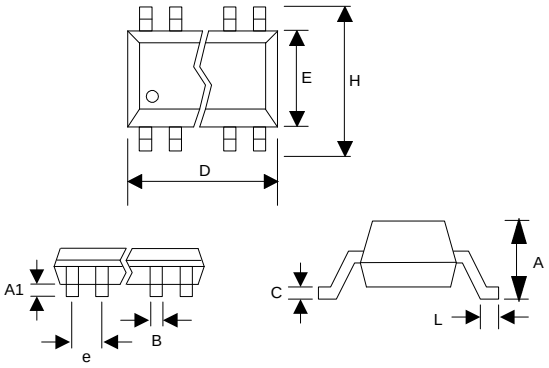
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	17		36	MHz
Crystal Loading Rating (VIN = 1.65V)	$C_{L\ (xtal)}$		8.5		pF
Maximum Sustainable Drive Level				200	µW
Operating Drive Level			50		µW
C0				5	pF
C0/C1				250	-
ESR	R_S			30	Ω

Note: The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above.
If the crystal requires more load to be at nominal frequency, the additional load must be added externally.
This however may reduce the pull range.

PACKAGE INFORMATION

8 PIN (dimensions in mm)

	Narrow SOIC		TSSOP	
Symbol	Min.	Max.	Min.	Max.
A	1.47	1.73	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	4.80	4.95	2.90	3.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.20	6.60
L	0.38	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	



ORDERING INFORMATION

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL500-17 S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL

PACKAGE TYPE
S=SOIC
D=Die

Order Number	Marking	Package Option
PLL500-17SC-R	P500-17 SC	SOIC - Tape and Reel
PLL500-17DC	P500-17	Die - Waffe Pack