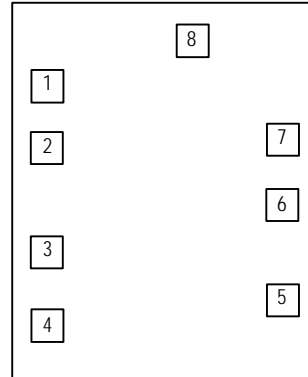


Low Phase Noise VCXO (8MHz to 40MHz)

FEATURES

- VCXO output for the 8MHz to 40MHz range
- Low phase noise (-130 dBc @ 10kHz offset at 30MHz).
- CMOS output with OE tri-state control.
- 16 to 40MHz fundamental crystal input.
- Selectable divider by 2 or no division.
- Integrated high linearity variable capacitors.
- 12mA drive capability at TTL output.
- +/- 250 ppm pull range, max 4% linearity.
- Low jitter (RMS): 2.5ps period jitter.
- 2.25V to 3.63V DC operation.
- Available in die.

PAD LAYOUT



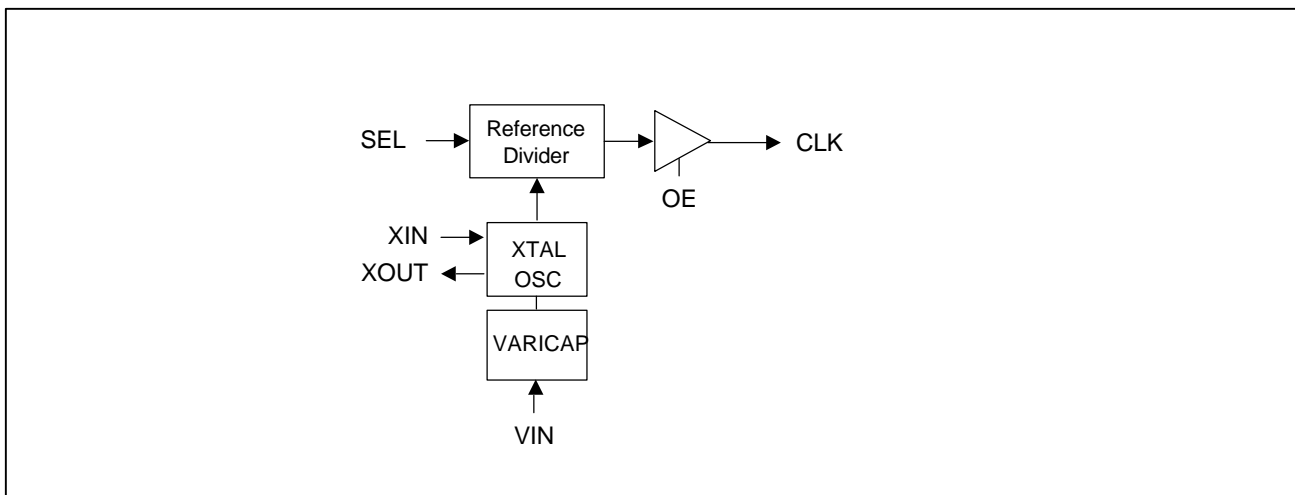
DESCRIPTION

The PLL500-10 is a low cost, high performance and low phase noise VCXO for the 8 to 40MHz range, providing less than -130dBc at 10kHz offset at 30MHz. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for applications requiring voltage controlled frequency sources. Input crystal can range from 16 to 40MHz (fundamental resonant mode).

SELECTABLE DIVIDER

| SEL | DIVIDER | OUTPUT BUFFER |
|-----------------|-------------|---------------|
| 1 | / 2 | CMOS |
| 0 or No connect | No division | CMOS |

BLOCK DIAGRAM



Low Phase Noise VCXO (8MHz to 40MHz)
PAD DESCRIPTION

| Name | Number | Type | Description |
|------|--------|------|--|
| XOUT | 1 | I | Crystal output pin. |
| VIN | 2 | I | Frequency control voltage input pin. |
| OE | 3 | I | Output Enable input pin. Tri-states output if low. Enables output if high. |
| GND | 4 | P | Ground pin. |
| CLK | 5 | O | Output clock pin. |
| VDD | 6 | P | +3.3V VDD power supply pin. |
| SEL | 7 | I | Divider select input pin. Allows user to choose between divider by 2 or 1. |
| XIN | 8 | I | Crystal input pin. |

See also pad coordinates table at the end of this document.

ELECTRICAL SPECIFICATIONS
1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|--------------------------------|----------|------|--------------|-------|
| Supply Voltage Range | V_{CC} | -0.5 | 7 | V |
| Input Voltage Range | V_I | -0.5 | $V_{CC}+0.5$ | V |
| Output Voltage Range | V_O | -0.5 | $V_{CC}+0.5$ | V |
| Soldering Temperature | | | 260 | °C |
| Storage Temperature | T_S | -65 | 150 | °C |
| Ambient Operating Temperature* | | -40 | 85 | °C |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for INDUSTRIAL grade only.

Low Phase Noise VCXO (8MHz to 40MHz)
2. AC Electrical Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|--------|-----------------------------|------|------|------|-------|
| Input Crystal Frequency | | | 16 | | 40 | MHz |
| Output Clock Rise/Fall Time | | 0.8V ~ 2.0V with 10 pF load | | 1.15 | | ns |
| | | 0.3V ~ 3.0V with 15 pF load | | 3.7 | | |
| Output Clock Duty Cycle | | Measured @ 1.4V | 45 | 50 | 55 | % |
| Short Circuit Current | | | | ±50 | | mA |

3. Voltage Control Crystal Oscillator

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|----------------------------|----------------------|---|------|------|------|-------|
| VCXO Stabilization Time * | T _{VCXOSTB} | From power valid | | 10 | | ms |
| VCXO Tuning Range | | F _{XIN} = 16 – 40MHz; XTAL C ₀ /C ₁ < 250 | 300 | | | ppm |
| CLK output pullability | | 0V ≤ V _{IN} ≤ 3.3V | ±150 | | | ppm |
| VCXO Tuning Characteristic | | | | 100 | | ppm/V |
| Pull range linearity | | | | 3.5 | 4 | % |
| Power Supply Rejection | PWSRR | Frequency change with V _{dd} varied +/- 10% | -1 | | 1 | ppm |
| VIN pin input impedance | | | 1000 | | | kΩ |
| VIN modulation BW | | 0V ≤ V _{IN} ≤ 3.3V, -3dB | 45 | | | kHz |

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. Jitter and Phase Noise specification

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|------|------|------|--------|
| RMS Period Jitter (1 sigma – 1000 samples) | with capacitive decoupling between VDD and GND. | | 2.3 | 2.5 | ps |
| Phase Noise relative to carrier | 30MHz @100Hz offset | | -80 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @1kHz offset | | -110 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @10kHz offset | | -130 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @100kHz offset | | -138 | | dBc/Hz |
| Phase Noise relative to carrier | 30MHz @1MHz offset | | -145 | | dBc/Hz |

Low Phase Noise VCXO (8MHz to 40MHz)
5. DC Specification

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|--|------------------|-------------------------------|-----------------------|------|------|-------|
| Supply Current, Dynamic, with Loaded Outputs | I _{DD} | 35.328MHz, Output load = 15pF | | 3.2 | 4 | mA |
| | | 17.664MHz, Output load = 15pF | | 2.2 | 3 | |
| Operating Voltage | V _{DD} | | 2.25 | | 3.63 | V |
| Output High Voltage | V _{OH} | I _{OH} = -12mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{LO} = 12mA | | | 0.4 | V |
| Output High Voltage at CMOS level | V _{OHC} | I _{OH} = -4mA | V _{DD} - 0.4 | | | V |
| Output drive current | | At TTL level | 12 | 17 | | mA |
| Short Circuit Current | | | | ±50 | | mA |
| VCXO Control Voltage | V _{IN} | | 0 | | 3.3 | V |
| ESD Protection | | Human Body Model | 3000 | | | |

6. Crystal Specifications

| PARAMETERS | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|--|-----------------------|------|------|------|-------|
| Crystal Resonator Frequency | F _{XIN} | 16 | | 40 | MHz |
| Crystal Loading Rating (V _{IN} = 1.65V) | C _{L (xtal)} | | 8 | | pF |
| Drive Level | | | 500 | | μW |
| C0 | | | | 7 | pF |
| C0/C1 | | | | 250 | - |
| ESR | R _s | | | 30 | Ω |

Note: The crystal must be such that it oscillates (parallel resonant) at nominal frequency when presented a C Load as specified above. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

Low Phase Noise VCXO (8MHz to 40MHz)

PAD ASSIGNMENT

| Pad # | Name | X (μm) | Y (μm) |
|-------|------|--------|--------|
| 1 | XOUT | TBD | TBD |
| 2 | VIN | TBD | TBD |
| 3 | OE | TBD | TBD |
| 4 | GND | TBD | TBD |
| 5 | CLK | TBD | TBD |
| 6 | VDD | TBD | TBD |
| 7 | SEL | TBD | TBD |
| 8 | XIN | TBD | TBD |

Die dimensions and reference coordinates in μm excluding scribe lines:

Lower left: X=0, Y=0
Upper right: X=812, Y=986

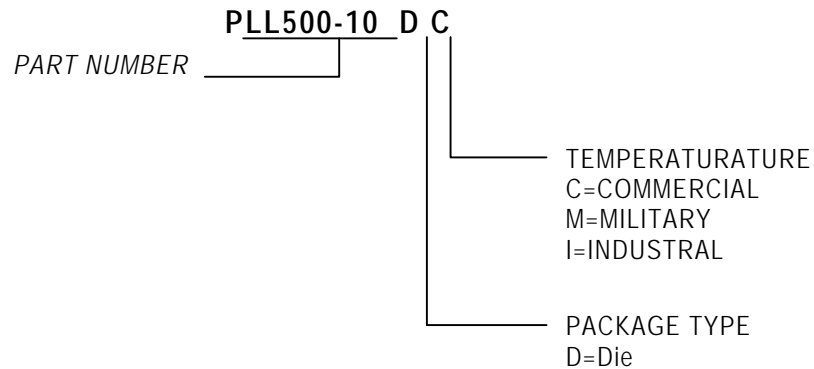
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



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