

PE4256

**75 Ω SPDT CATV UltraCMOS™ Switch
DC - 3.0 GHz**

Features

- 75 Ω characteristic impedance
- Integrated 75 Ω 0.25 watt terminations
- CTB performance of -90 dBc
- High isolation 65 dB at 1000 MHz
- Low insertion loss: typically 0.5 dB at 5 MHz, 0.9 dB at 1000 MHz
- High input IP3: >50 dBm
- CMOS two-pin control
- Single +3 volt supply operation
- Low current consumption: 8 μ A
- Unique all off terminated mode
- 4x4 mm QFN package

Product Description

The PE4256 is an UltraCMOS™ Switch designed for CATV applications, covering a broad frequency range from DC up to 3000 MHz. This single-supply SPDT switch integrates a two-pin CMOS control interface. It also provides low insertion loss with extremely low bias requirements while operating on a single 3-volt supply. In a typical CATV application, the PE4256 provides for a cost effective and manufacturable solution when compared to mechanical relays.

The PE4256 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

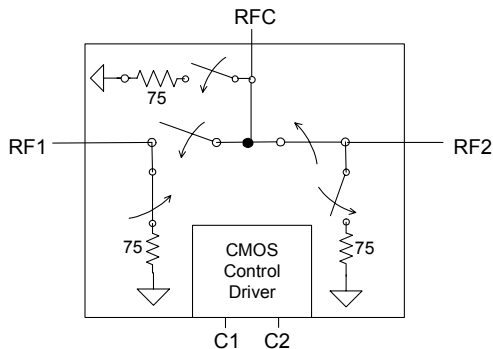


Figure 2. Package Type
20-lead 4x4 mm QFN



Table 1. Electrical Specifications @ +25 °C, V_{DD} = +3 V (Z_S = Z_L = 75 Ω)

Parameter	Condition	Minimum	Typical	Maximum	Units
Operating Frequency ¹		DC		3000	MHz
Insertion Loss	5 MHz – 250 MHz		0.5	0.6	dB
	250 MHz – 750 MHz		0.8	0.95	
	750 MHz – 1000 MHz		0.9	1.1	
	1000 MHz – 2200 MHz		1.1	1.3	
Isolation	5 MHz – 250 MHz	75	80		dB
	250 MHz – 750 MHz	65	70		
	750 MHz – 1000 MHz	62	65		
	1000 MHz – 2200 MHz	49	52		
Input IP2 ²	5 MHz - 1000 MHz		80		dBm
Input IP3 ²	5 MHz - 1000 MHz	50	55		dBm
Input 1dB Compression ²	1000 MHz	29	31		dBm
CTB / CSO	77 & 110 channels; Power Out = 44 dBmV		-90		dBc
Switching Time	50% CTRL to 10/90% RF		2		μ s
Video Feedthrough ³	5 MHz - 1000 MHz			15	mV _{pp}

Notes:

1. Device linearity will begin to degrade below 1 MHz.
2. Measured in a 50 Ω system.
3. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth

Figure 3. Pin Configuration (Top View)

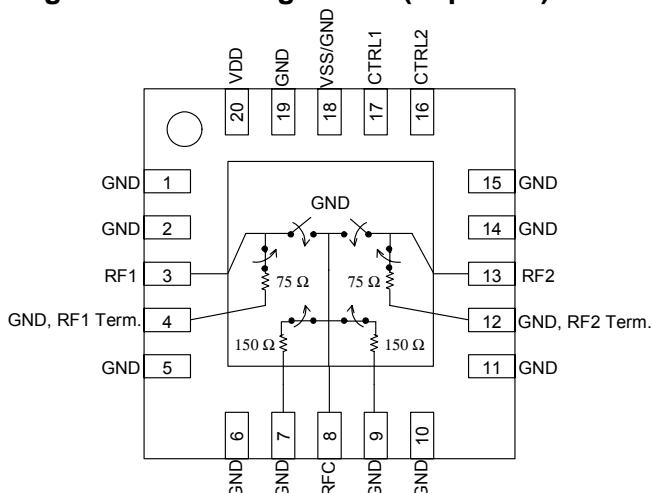


Table 2. Pin Descriptions

No.	Name	Description
1	GND	Ground
2	GND	Ground
3 ¹	RF1	RF I/O
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8 ¹	RFC	Common
9	GND	Ground
10	GND	Ground
11	GND	Ground
12	GND	Ground
13 ¹	RF2	RF I/O
14	GND	Ground
15	GND	Ground
16 ²	C2	Control 2
17 ²	C1	Control 1
18 ³	VSS / GND	Negative Supply Option
19	GND	Ground
20	VDD	Supply
Pad	GND	Ground Pad

Notes:

1. RF pins 3, 8, and 13 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pins 16 and 17 are the CMOS controls that set the three operating states.
3. Connect pin 18 to GND to enable the on-chip negative voltage generator. Connect pin 18 to V_{SS} (-3V) to bypass and disable internal -3V supply generator.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on CTRL input	-0.3	V _{DD} + 0.3	V
P _{RF}	RF CW power		24	dBm
T _{ST}	Storage temperature	-65	150	°C
T _{OP}	Operating temperature	-40	85	°C
V _{ESD}	ESD voltage (Human Body Model)		1000	V

Table 4. DC Electrical Specifications @ 25 °C

Parameter	Min	Typ	Max	Unit
V _{DD} Power Supply	2.7	3.0	3.3	V
I _{DD} Power Supply Current (V _{DD} = 3V, V _{CNTL} = 3V)		8	20	μA
Control Voltage High	70% V _{DD}			V
Control Voltage Low			30% V _{DD}	V

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE4256 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 18=GND).

Table 5. RF Path Truth Table

C1	C2	RFC – RF1	RFC – RF2
Low	Low	OFF	OFF
Low	High	OFF	ON
High	Low	ON	OFF
High	High	N/A ¹	N/A ¹

Table 6. Termination Truth Table

C1	C2	RFC – 75 Ω	RF1 – 75 Ω	RF2 – 75 Ω
Low	Low	X ²	X ²	X ²
Low	High		X ²	
High	Low			X ²
High	High	N/A ¹	N/A ¹	N/A ¹

Notes: 1. The operation of the PE4256 is not supported or characterized in the C1=V_{DD} and C2=V_{DD} state.
2. "X" denotes termination enabled.

Evaluation Kit

The SPDT Switch Evaluation Kit was designed to ease customer evaluation of the PE4256 SPDT switch. The RF common port (RFC) is connected through a 75 Ω transmission line to J2. Port 1 and Port 2 are connected through 75 Ω transmission lines to J1 and J3. A through transmission line connects F connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed with four metal layers in FR4 material with a total thickness of 0.062". The transmission lines were designed using a coplanar waveguide with ground plane (28 mil core, 21 mil width, 30 mil gap).

J6 provides a means for controlling DC and digital inputs to the device. The provided jumpers short the package pin to ground for logic low. When the jumper is removed, the pin is pulled up to V_{DD} for logic high.

When the jumper is in place, 3 μ A of current will flow through the 1 M Ω pull-up resistor. This extra current should not be attributed to the device.

Proper PCB design is essential for full isolation performance. This evaluation board demonstrates good trace and ground management for minimum coupling and radiation.

Figure 4. Evaluation Board Layouts

Peregrine Specification 101/0148~03A

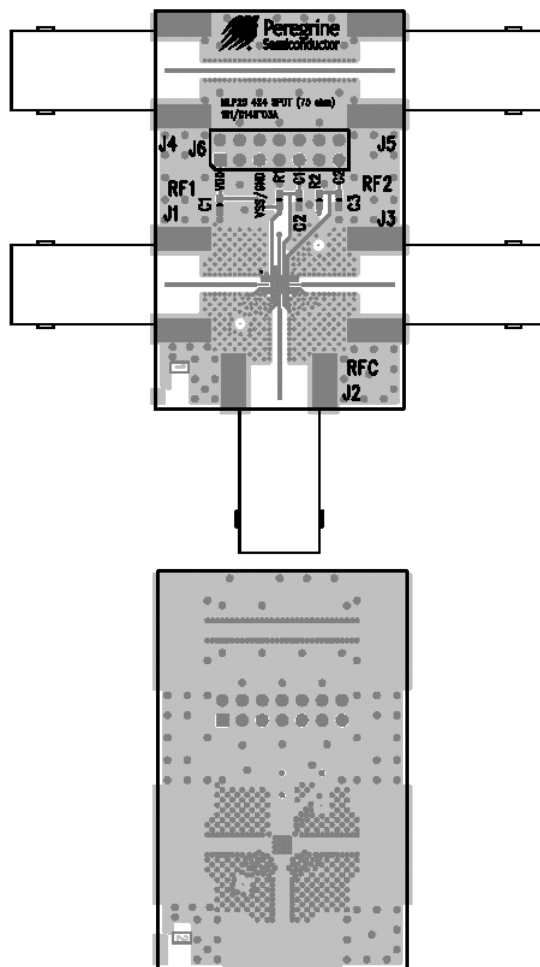
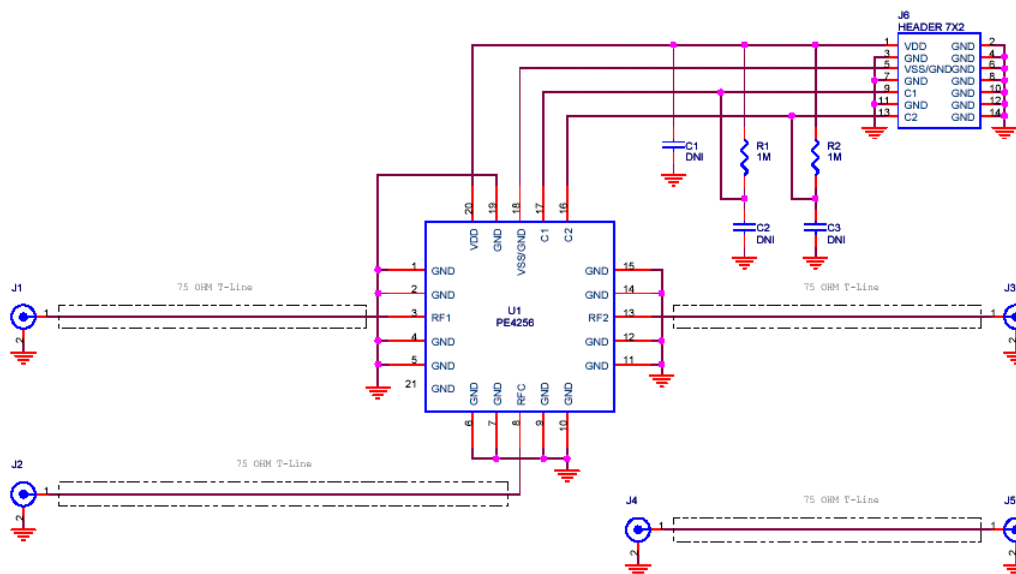


Figure 5. Evaluation Board Schematic

Peregrine Specification 102/0195~02A



Typical Performance Data from -40°C to +85°C, 75 Ω Impedance

Figure 6. Insertion Loss (RFC to RF1 or RF2)

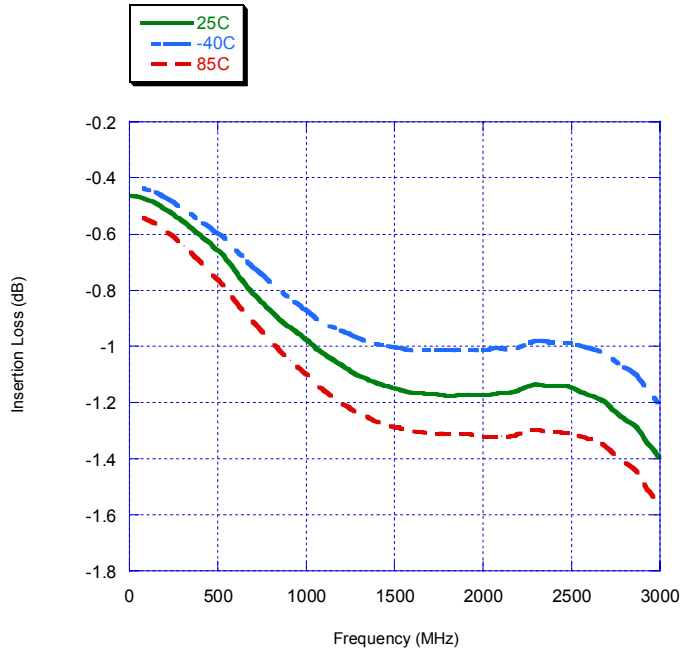


Figure 7. Input to Output Isolation

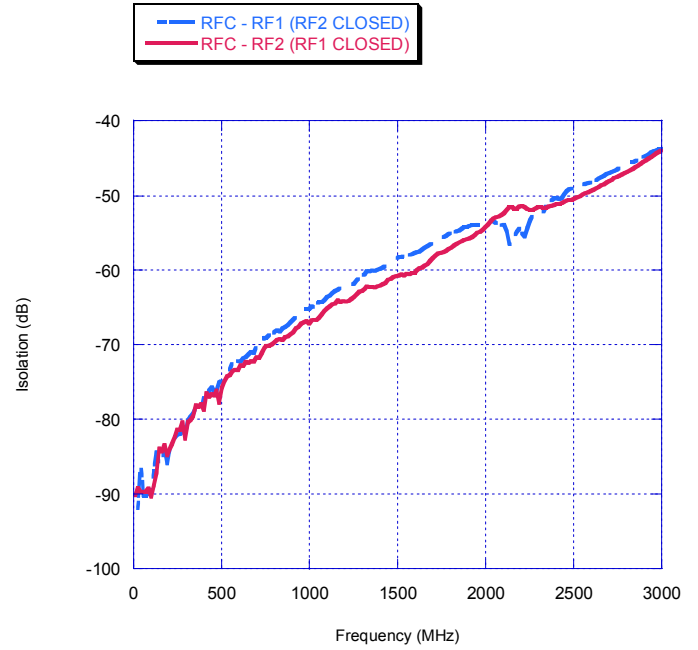


Figure 8. Input to Output Isolation

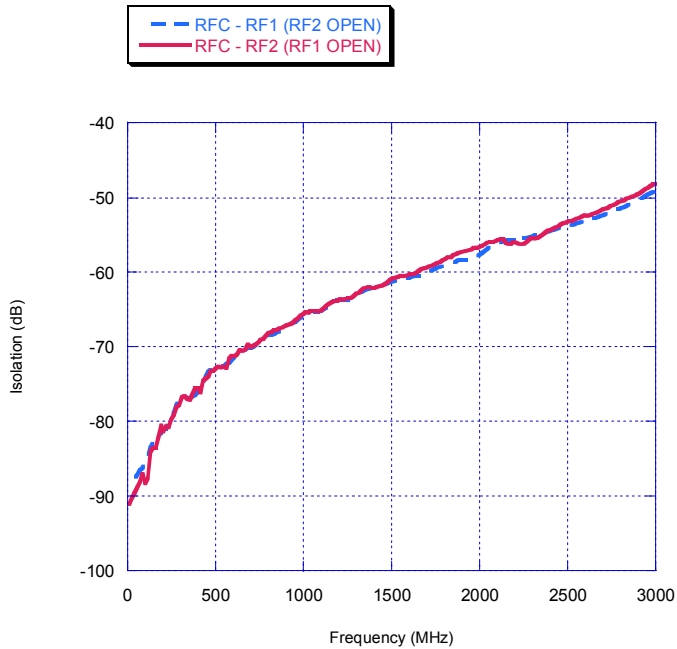
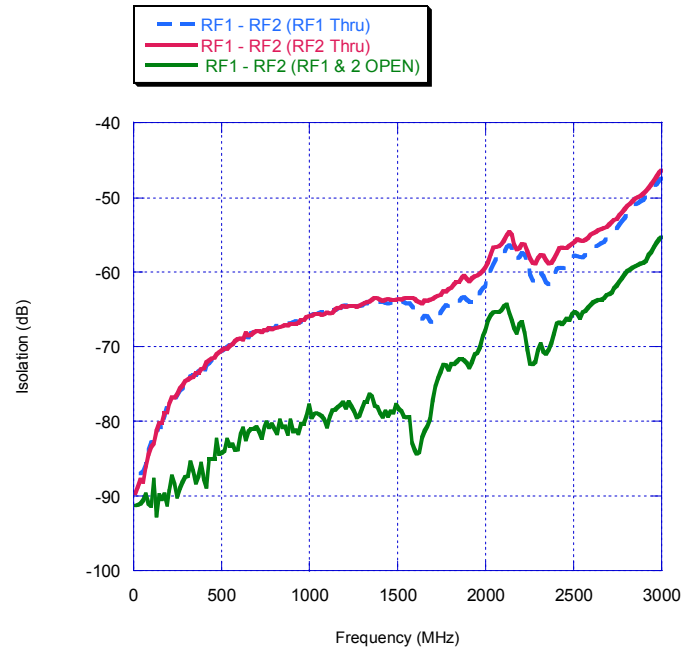


Figure 9. Isolation – RF1 To RF2



Typical Performance Data @ +25°C, 75 Ω Impedance (unless otherwise noted)

Figure 10. RFC Return Loss

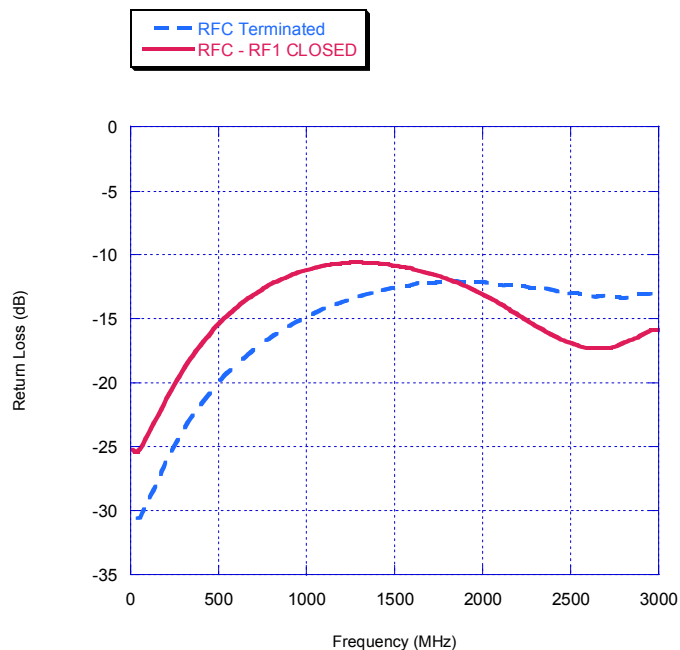


Figure 11. RF1 Return Loss

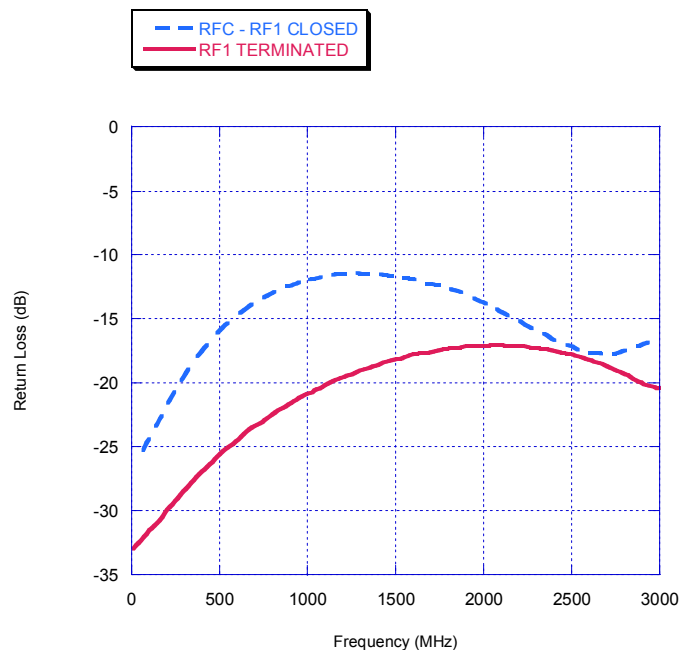


Figure 12. RF2 Return Loss

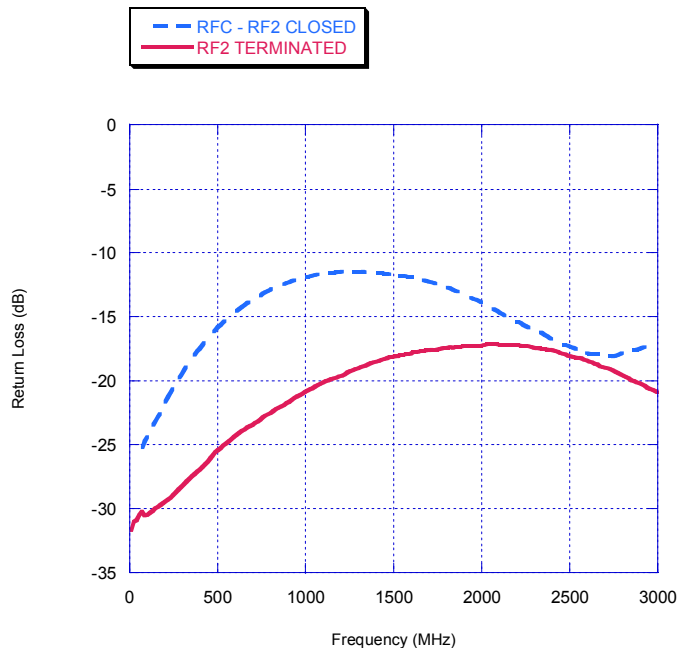
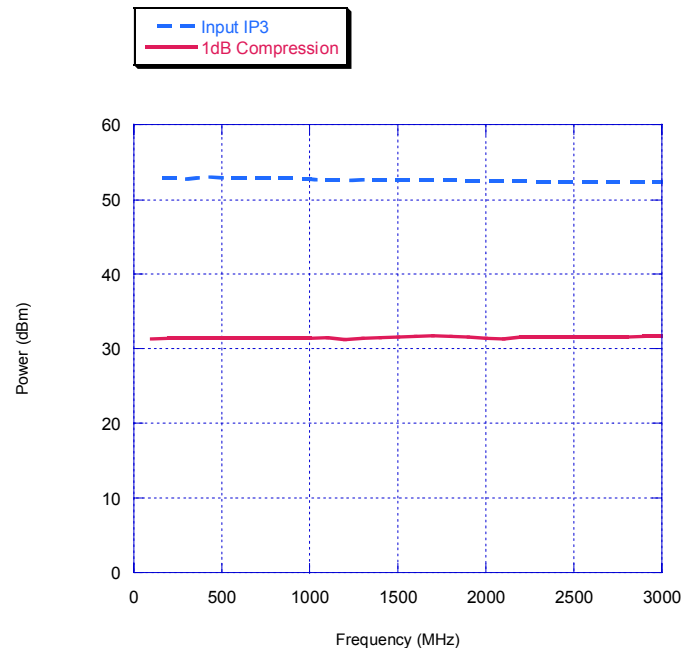


Figure 13. Linearity (50 Ω System Impedance)



20-lead 4x4 mm QFN

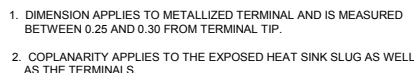


Figure 15. Tape and Reel Drawing



Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4256-01	4256	PE4256-20QFN 4x4 mm-75A	20-lead 4x4 mm QFN	75 units / Tube
4256-02	4256	PE4256-20QFN 4x4 mm-3000C	20-lead 4x4 mm QFN	3000 units / T&R
4256-00	PE4256-EK	PE4256-20QFN 4x4 mm-EK	Evaluation Kit	1 / Box
4256-51	4256	PE4256G-20QFN 4x4 mm-75A	Green 20-lead 4x4 mm QFN	75 units / Tube
4256-52	4256	PE4256G-20QFN 4x4 mm-3000C	Green 20-lead 4x4 mm QFN	3000 units / T&R

Sales Offices

United States

Peregrine Semiconductor Corp.

9450 Carroll Park Drive
San Diego, CA 92121
Tel 1-858-731-9400
Fax 1-858-731-9499

Europe

Peregrine Semiconductor Europe

Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches, France
Tel: 011- 33-1-47-41-91-73
Fax : 011-33-1-47-41-91-73

Japan

Peregrine Semiconductor K.K.

5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 011-81-3-3502-5211
Fax: 011-81-3-3502-5213

China

Peregrine Semiconductor

28G, Times Square,
No. 500 Zhangyang Road,
Shanghai, 200122, P.R. China
Tel: 011-86-21-5836-8276
Fax: 011-86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS is a trademark of Peregrine Semiconductor Corp.