# Product Brief

# PE42694 Flip Chip

## *SP9T UltraCMOS™ 2.75 V Switch*
## *100 – 3000 MHz, +69 dBm IIP3*

**Figure 1. Functional Diagram**

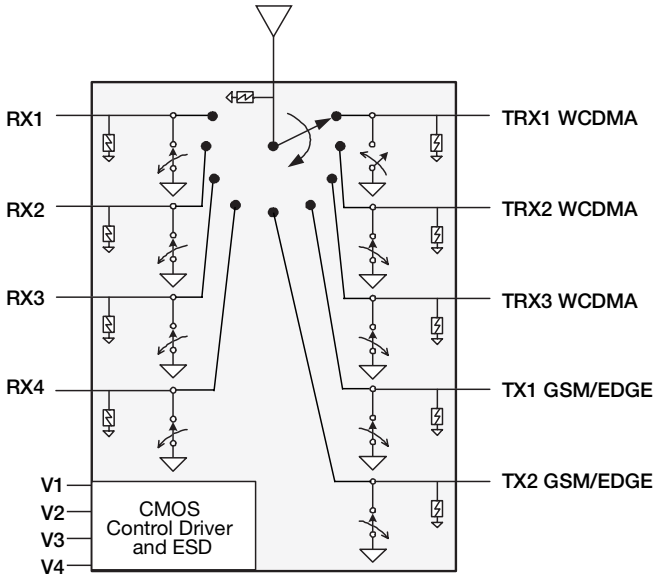



**Figure 2. Die Top View**

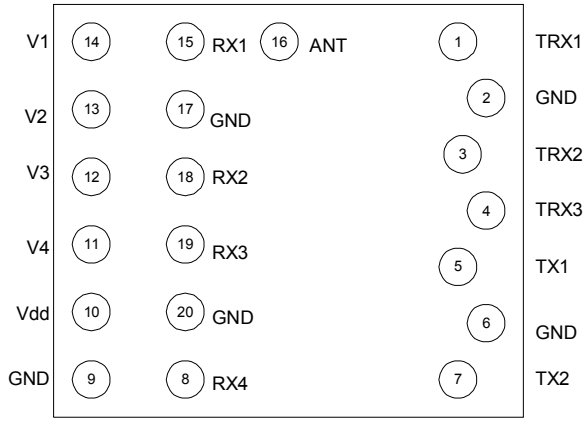
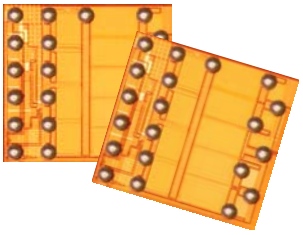



**Figure 3. Package Type: Flip Chip**



## *Features*

- Two GSM/PCS/EDGE compliant TX ports, three TRX ports (WCDMA band or receive ports), and four RX ports
- Four pin CMOS logic control with integral decoder/driver
- Exceptional harmonic performance: $2f_o$ = -76 dBc and $3f_o$ = -76 dBc
- Low TRX insertion loss: 0.55 dB at 900 MHz, 0.7 dB at 1900 MHz
- TX – RX Isolation of 51 dB at 900 MHz, 45 dB at 1900 MHz
- 1500 V HBM ESD tolerance all ports
- +69 dBm IIP3 @ 50 Ω
- -112 dBm IMD3
- No blocking capacitors required

## *Product Description*

*The PE42694 is a HaRP™-enhanced SP9T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market for use in GSM/ PCS/EDGE/DCS/WCDMA handsets. The switch is comprised of two transmit ports that can be used for GSM/PCS/EDGE, three transmit/receive ports (TRX1, TRX2 and TRX3) that can be used for either WCDMA or as receive ports, and four symmetric receive ports. An on-chip CMOS decode logic facilitates four-pin low voltage CMOS control. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.*

*Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.*

## Table 1. Target Electrical Specifications @ +25 °C, $V_{DD}$ = 2.75 V ($Z_S$ = $Z_L$ = 50 Ω)

| Parameter | Condition | Typ | Units |
|---|---|---|---|
| Insertion Loss[1] | TRX - Ant (850 WCDMA)<br>TRX - Ant (1950 / 2140 WCDMA)<br>TX - Ant (850 / 900)<br>TX - Ant (1800 / 1900)<br>RX - Ant (850 / 900)<br>RX - Ant (1800 / 1900) | 0.55<br>0.7<br>0.55<br>0.7<br>0.8<br>1.0 | dB<br>dB<br>dB<br>dB<br>dB<br>dB |
| Return Loss | All Ports in On State | 20 | dB |
| Isolation[2] | TX - RX (850 / 900)<br>TX - RX (1800 / 1900)<br>TRX - RX (850 / 900)<br>TRX - RX (2200)<br>TX - TRX (850 / 900)<br>TX - TRX (2200)<br>TX - TX (850 / 900)<br>TX - TX (1800 / 1900) | 51<br>45<br>43<br>34<br>34<br>28<br>31<br>26 | dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB<br>dB |
| 2nd Harmonic[3] | TX 850/900 MHz, +35 dBm output power, 50 Ω<br>TX 1800/1900 MHz, +33 dBm output power, 50 Ω | -76<br>-76 | dBc<br>dBc |
| 3rd Harmonic[3] | TX 850/900 MHz, +35 dBm output power, 50 Ω<br>TX 1800/1900 MHz, +33 dBm output power, 50 Ω | -76<br>-76 | dBc<br>dBc |
| WCDMA Band I IMD3 | TRX – Measured in a 50 Ω system at 2.14 GHz at the TX1 port. Input signals are referenced to the ANT port with +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz | -112 | dBm |
| WCDMA Band I IIP3 | TRX – Measured in a 50 Ω system at 2.14 GHz at the TX1 port. Input signals are referenced to the ANT port with +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz | +69 | dBm |
| Switching time | 50% of control to (10/90%) RF | 2 | µs |

Notes: 1. Insertion loss specified with optimal ANT impedance matching.
2. EK board limited isolation.
3. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.

## Table 2. Operating Ranges

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Temperature range | $T_{OP}$ | -40 | | +85 | °C |
| $V_{DD}$ Supply Voltage | $V_{DD}$ | 2.65 | 2.75 | 2.85 | V |
| $I_{DD}$ Power Supply Current ($V_{DD}$ = 2.75V) | $I_{DD}$ | | 100 | | µA |
| TX input power[4] (VSWR 3:1) | $P_{IN}$ | | | +35 | dBm |
| TRX input power[4] (VSWR 3:1) | $P_{IN}$ | | | +32 | dBm |
| RX input power[4] (VSWR 3:1) | $P_{IN}$ | | | +20 | dBm |
| Control Voltage High | $V_{IH}$ | 1.4 | | | V |
| Control Voltage Low | $V_{IL}$ | | | 0.4 | V |

Note: 4. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.

Part performance is not guaranteed under absolute maximum conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

## Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | -0.3 | 4.0 | V |
| $V_I$ | Voltage on any DC input | -0.3 | $V_{DD}$+ 0.3 | V |
| $T_{ST}$ | Storage temperature range | -65 | +150 | °C |
| $T_{OP}$ | Operating temperature range | -40 | +85 | °C |
| $P_{IN}$(50 Ω) | TX input power (50 Ω)[5,6] | | +38 | dBm |
| | TRX input power (50 Ω)[5,6] | | +35 | |
| | RX input power (50 Ω) [5,6] | | +23 | |
| $P_{IN}$ (∞ :1) | TX input power (VSWR ∞ :1) [5,6] | | +35 | dBm |
| | TRX input power (VSWR ∞ :1)[5,6] | | +32 | |
| $V_{ESD}$ | ESD Voltage (HBM, MIL_STD 883 Method 3015.7) | | 1500 | V |
| | ESD Voltage (MM, JEDEC, JESD22-A114-B) | | 100 | V |

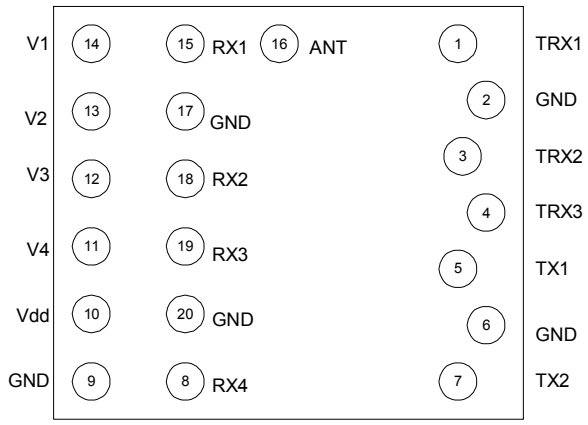
Notes: 5. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005.
6. $V_{DD}$ within operating range specified in Table 2.

## Table 4. Pin Descriptions

| Pad # | Pad Name | Description |
|---|---|---|
| 1 | TRX1[7] | RF I/O – TRX1 |
| 2 | GND | Ground |
| 3 | TRX2[7] | RF I/O – TRX2 |
| 4 | TRX3[7] | RF I/O – TRX3 |
| 5 | TX1[7] | RF I/O – TX1 |
| 6 | GND | Ground |
| 7 | TX2[7] | RF I/O – TX2 |
| 8 | RX4[7] | RF I/O – RX4 |
| 9 | GND | Ground |
| 10 | $V_{DD}$[8] | Supply |
| 11 | V4[8] | Switch control input, CMOS logic level |
| 12 | V3[8] | Switch control input, CMOS logic level |
| 13 | V2[8] | Switch control input, CMOS logic level |
| 14 | V1[8] | Switch control input, CMOS logic level |
| 15 | RX1[7] | RF I/O – RX1 |
| 16 | ANT | RF Common – Antenna |
| 17 | GND | Ground |
| 18 | RX2[7] | RF I/O – RX2 |
| 19 | RX3[7] | RF I/O – RX3 |
| 20 | GND | Ground |

Notes: 7. Blocking capacitors needed only when non-zero DC voltage present.
8. Application must ensure at least 40 dB of voltage isolation from the RF signal.

## Figure 4. Pad Configuration (bump side up)




## Table 5. Truth Table

| Path | V4 | V3 | V2 | V1 |
|---|---|---|---|---|
| **TX1-ANT** | 0 | 0 | 0 | 1 |
| **TX2-ANT** | 0 | 0 | 1 | 1 |
| **TRX1-ANT** | 1 | 0 | 0 | 0 |
| **TRX2-ANT** | 1 | 0 | 1 | 0 |
| **TRX3-ANT** | 1 | 1 | 0 | 0 |
| **RX1-ANT** | 0 | 0 | 0 | 0 |
| **RX2-ANT** | 0 | 0 | 1 | 0 |
| **RX3-ANT** | 0 | 1 | 0 | 0 |
| **RX4-ANT** | 0 | 1 | 1 | 0 |

## Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

## Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

## Table 6. Ordering Information

| Order Code | Package | Shipping Method |
|---|---|---|
| PE42694DTI | Bumped Wafer on Film Frame | Wafer (Gross Die / Wafer Quantity) |
| PE42694DBI | Die in Waffle Pack | 380 Dice / Waffle Pack |
| EK-42694-01 | Evaluation Kit | 1/ box |

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## Data Sheet Identification

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### *Preliminary Specification*

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### *Product Specification*

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