GENERAL DESCRIPTION

The pll2109x is a Phase Locked Loop(PLL) frequency synthesizer. The PLL provides frequency multiplication capabilities. Its output clock frequency FOUT is related to the input clock frequency FIN by the following equation:

$$FOUT = (m \times FIN) / (p \times 2^S)$$

where FOUT is the output clock frequency. FIN is the input clock frequency. m, p and s are the values for programmable dividers. pll2109x consists of a Phase Frequency Detector(PFD), a Charge Pump, an Off-chip Loop Filter, a Voltage Controlled Oscillator (VCO), a 6-bit Pre-divider, an 8-bit Main-divider and 2-bit Post-scaler as will be shown in functional block diagram.

FEATURES

- 0.13um CMOS device technology
- 1.2V single power supply
- Output frequency range: 100M ~ 500MHz
- Jitter: ±75ps at 500MHz
- Duty ratio: 40% to 60% (All tuned range)
- Power down mode
- Off-chip loop filter
- Frequency is changed by programmable divider

NOTES:

1. Don't set the P or M value as zero, that is, setting the P=000000, M=00000000 can cause malfunction of the PLL.
2. The proper range of P and M: $1 \le P \le 62$, $1 \le M \le 248$ (refer to page6 functional description)
3. The P and M must be selected considering stability of PLL and VCO output frequency range.
4. **Please contact SEC application engineer for proper selection of the P, M, S values of the PLL.**

Ver_1.0.3 (May. 2003)

FUNCTIONAL BLOCK DIAGRAM

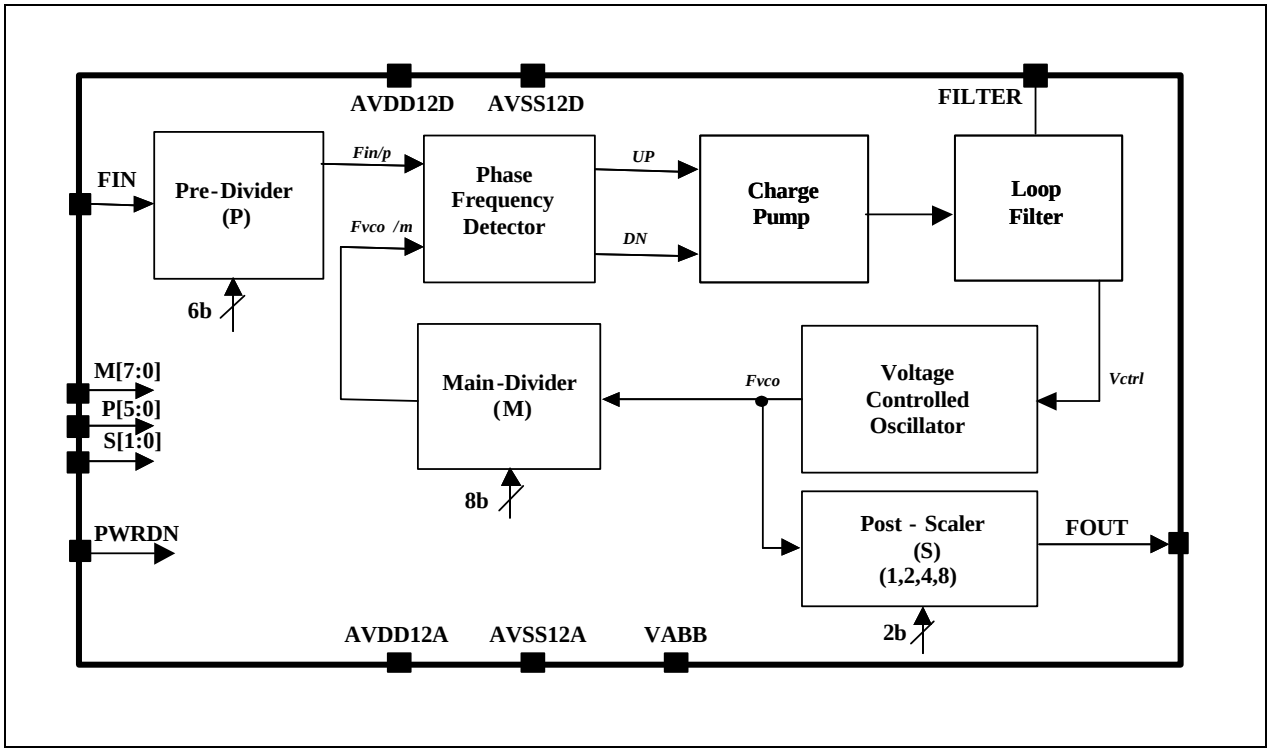


Figure 1. Block Diagram

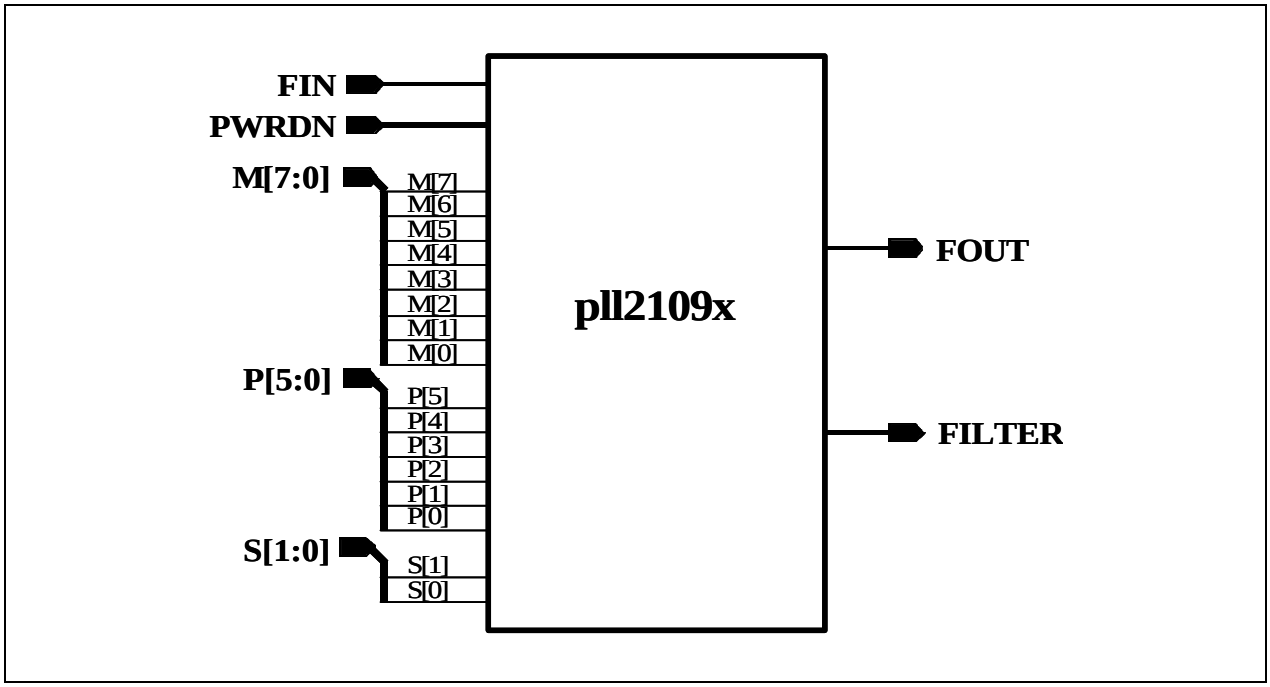
CORE PIN DESCRIPTION

Name	I/O Type	Pin Description
AVDD12D	DP	Digital power supply
AVSS12D	DG	Digital ground
AVDD12A	AP	Analog power supply
AVSS12A	AG	Analog ground
VABB	AB/DB	Analog / Digital bulk bias
FIN	DI	PLL clock input
FOUT	DO	100MHz ~ 500MHz clock output
FILTER	AO	The external loop filter capacitor should be connected between FILTER and analog ground
PWRDN	DI	Power down. - If PWRDN is high, power down mode is enabled.
P[5:0]	DI	6-bit programmable pre-divider.
M[7:0]	DI	8-bit programmable main-divider.
S[1:0]	DI	2-bit programmable post-scaler.

I/O Type Abbr.

— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AP: Analog Power
— AG: Analog Ground
— AB: Analog Sub Bias
— DP: Digital Power
— DG: Digital Ground
— DB: Digital Sub Bias

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATING

Characteristics	Symbol	Value	Unit	Applicable Pin
Supply voltage	AVDD12D AVDD12A	1.8	V	AVDD12D, AVDD12A
Storage temperature	Tstg	–65 ~ 150	°C	–

NOTES:

1. Absolute maximum rating specifies the values beyond which the device may be damaged permanently. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit	Remark
Supply voltage differential	AVDD12D-AVDD12A	–0.1		+0.1	V	
External loop filter capacitor	LF		1.7		nF	Capacitor tolerance (±5%)
Operating temperature	Topr	–40		85	°C	

NOTE: It is strongly recommended that all the supply pins (AVDD12D, AVDD12A) be powered to the same supply voltage to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	AVDD12D/AVDD12A	1.14	1.20	1.26	V
Digital input voltage high	V_{IH}	0.7VDD	–	–	V
Digital input voltage low	V_{IL}	–	–	0.3VDD	V
Dynamic current	I_{DD}	–	–	3	mA
Power down current	I_{PD}	–	–	TBD	uA

NOTE: Operating voltage Min/Max are preliminary values and expected to be updated.

AC ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Min	Typ	Max	Unit
Input frequency		Fin	10	–	50	MHz
VCO output frequency		Fvco	200	–	500	MHz
Output frequency		Fout	100	–	500	MHz
Input clock duty ratio		T_{ID}	40	50	60	%
Output clock duty ratio		T_{OD}	40	50	60	%
Locking time		T_{LT}	–	300	–	us
Cycle to cycle jitter	100M ~ 200MHz	T_{JCC}	–	±300	TBD	ps
	200M ~ 300MHz	T_{JCC}	–	±150	TBD	ps
	300M ~ 400MHz	T_{JCC}	–	±100	TBD	ps
	400M ~ 500MHz	T_{JCC}	–	±75	TBD	ps

FUNCTIONAL DESCRIPTION

A PLL is the circuit synchronizing an output signal (generated by a VCO) with a reference or input signal in frequency as well as in phase. The pll2109x can provide frequency multiplication capabilities, but does not support functions such as deskew and phase synchronization between Fin and Fout.

PLL2109X consists of the following basic blocks.

— The phase frequency detector (PFD) detects the phase difference between the reference clock and feedback clock, then generates UP/DOWN error signals. If reference clock leads or lags feedback clock, the charge pump charges or discharges the following loop filter according to UP/DOWN signal.

— The loop filter suppresses high frequency components in the charge pump voltage (Vctrl), allowing the dc value to control the VCO frequency.

— The voltage-controlled oscillator generates the clock signal proportional to control voltage.
Required frequency is produced by appropriate selection of P, M and S dividers.

Fout = Fin × m/(p × s)

m = M+8 , p = P+2, s = 1, 2, 4, 8

— Don't set the value P or M to all zero, that is 000000 / 00000000.

— The range of P and M: $1 \le P \le 62$, $1 \le M \le 248$

— The M and P must be selected considering stability and VCO range.
VCO output frequency range of pll2109x is from 200MHz to 500MHz.

Digital Data Format:

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

NOTE: M[7] - M[0]: main-divider $1 \le M \le 248$
P[5] - P[0]: pre-divider $1 \le P \le 62$
S[1] - S[0]: post-scaler $0 \le S \le 3$

Important Notice: Please contact SEC application engineer for proper selection of M, P, S values.

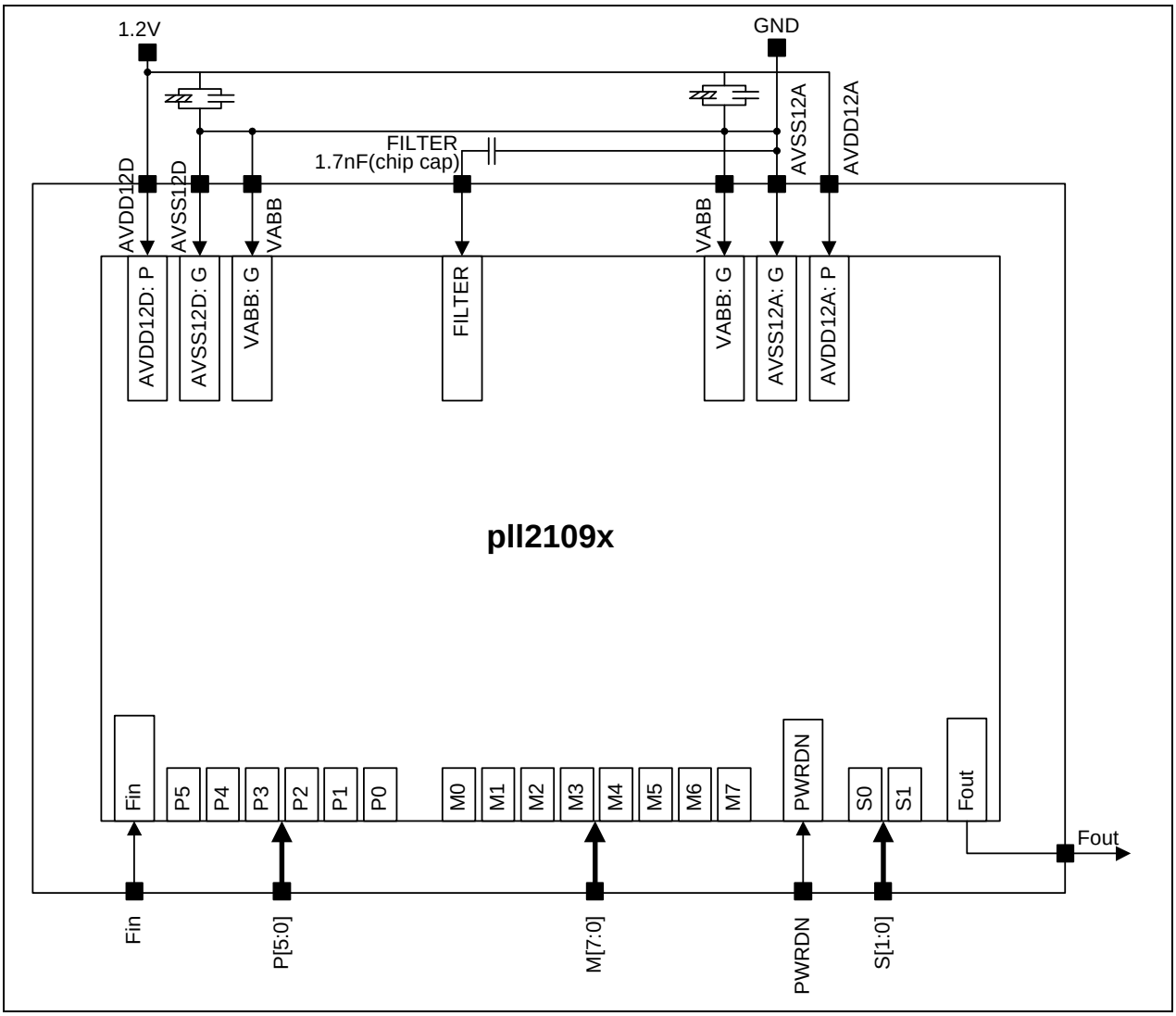
CORE EVALUATION GUIDE

You can generate various output frequencies by changing M/P/S setting. There are two methods of controlling divider values.

— Method 1: 16-bit register can be used for easy control of divider values.

— Method 2: P, M and S pins are bypassed to the external port, and you can control each port directly.

It is undesirable to connect P[5:0], M[7:0] and S[1:0] to the internal power or ground directly because of ESD issue.



NOTE: : 10uF electrolytic capacitor
Unless otherwise specified
: 0.1uF ceramic capacitor
Unless otherwise specified

CORE LAYOUT GUIDE

1. The Digital power(AVDD12D, AVSS12D) and the analog power(AVDD12A, AVSS12A) must be dedicated to PLL only and separated. Please consult PLL dedicated I/O assign with SEC application engineer.
2. The FOUT and FILTER pins and routings must be placed far from the internal signals in order to avoid cross-talk.
3. Those blocks consume a large amount of digital switching current must be located away from the PLL core.

LAYOUT DESIGN CONSIDERATIONS

The following design considerations must be applied.

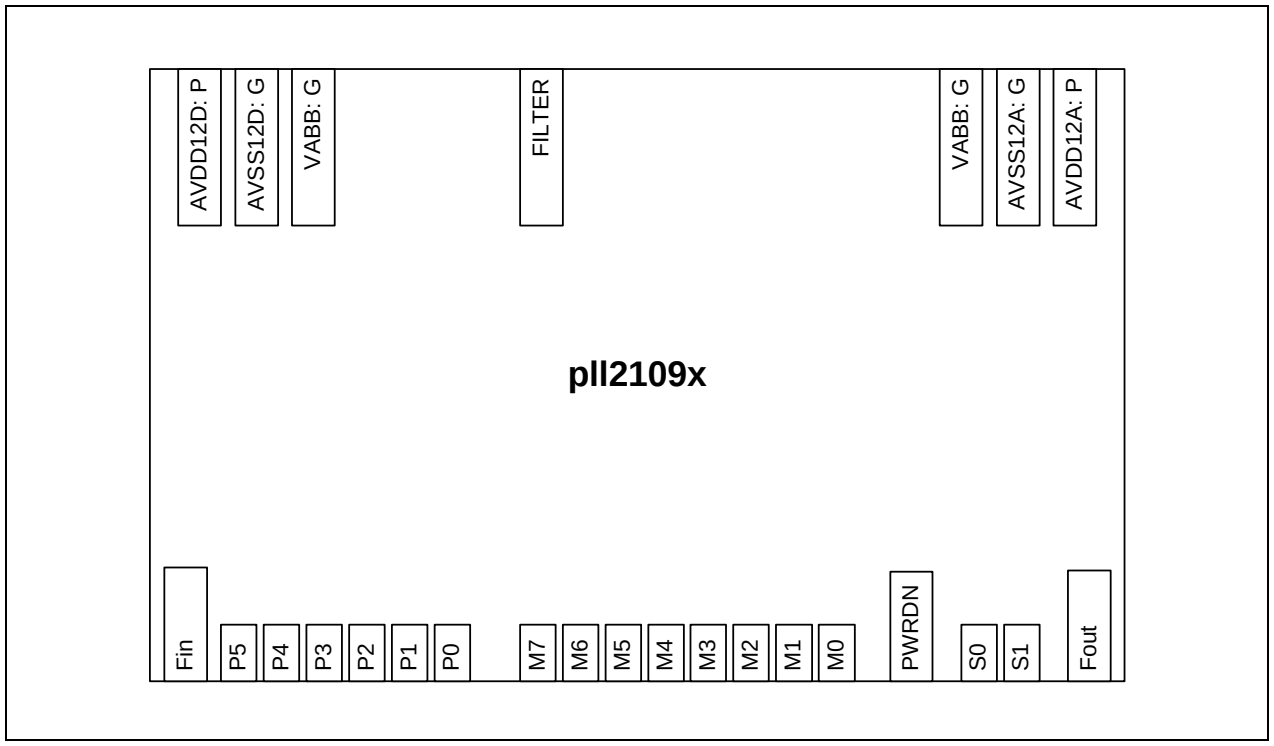
1. Jitter is affected by the power noise, substrate noise, etc. It depends on embedded environment noise level.
2. A CMOS-level input reference clock is recommended for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
3. The use of two, or more PLLs requires special layout considerations. Please consult it with SEC application engineer for more information.
4. The PLL core should be placed as close as possible to the dedicated loop filter and analog power and ground pads & pins.
5. It is not recommended to locate high frequency noise-generating signals and cores near the PLL and its I/O cells. For example, data buses, high frequency outputs and high current consuming cells.

PHANTOM CELL INFORMATION

Pins of the core can be assigned externally(package pins) or internally(internal ports) depending on design methods.

— The term "external" implies that the pins should be assigned externally like power pins.

— The term "internal/external" implies that those pins are user dependent.



PIN LAYOUT GUIDE

Pin Name	Pin Usage	Pin Layout Guide
AVDD12D	External	– Use dedicated power/ground pins for PLL – Power cuts are required to provide on-chip isolation → between dedicated PLL power/ground and all other power/ground – Use good power and ground source on board
AVSS12D	External	
AVDD12A	External	
AVSS12A	External	
VABB	External	
FIN	External	– Do not place noisy, high frequency and high power consuming circuitry pads near the FIN pin. – Use proper low jitter reference clock
FOUT	External/Internal	– Do not place noisy, high frequency and high power consuming circuitry pads near the FOUT pin. – Internal routing path should be as short as possible. This will minimize loading effect. – FOUT signals should not be crossed by any signals and should not run next to digital signals. This will minimize capacitive coupling between the two signals.
FILTER	External	– Do not place the noisy, high frequency and high power consuming circuitry pads near the FILTER. – Ground shielding is needed for internal routing path. – FILTER routing path should not be crossed by any other signals and should not be placed next to digital signals. – External loop filter pin should be placed between analog power and ground to avoid stray coupling outside the chip and magnetic coupling via bond wires. – External loop filter components and internal routing should be as short as possible.
PWRDN	Internal /External	
M[7] ~ M[0]	Internal/External	
P[5] ~ P[0]	Internal/External	
S[1] ~ S[0]	Internal/External	

FEEDBACK REQUEST

Thank you for having an interest in our products. Please fill out this form, especially the items which you want to request.

Parameter		Customer	SEC	Unit
Process			0.13um CMOS	
Supply voltage (VDD)			1.2 ± 0.06	V
Input frequency (FIN)			10 ~ 50	MHz
Output frequency (FOUT)			100 ~ 500	MHz
Cycle to cycle jitter (TJCC)	100M ~ 200M		TBD	psec (pk-pk)
	200M ~ 300M		TBD	
	300M ~ 400M		TBD	
	400M ~ 500M		TBD	
Period jitter (TJP)	100M ~ 200M		TBD	psec (pk-pk)
	200M ~ 300M		TBD	
	300M ~ 400M		TBD	
	400M ~ 500M		TBD	
Output duty ratio (TOD)			40 ~ 60	%
Lock up time (TLT)			TBD	usec
Dynamic current			< 3m	A
Stand by current			TBD	A
Filter capacitor			External	–

— How many PLLs are embedded in your system ?

— Do you need synchronization between input clock and output clock ?

— Do you need another spec of jitter ?

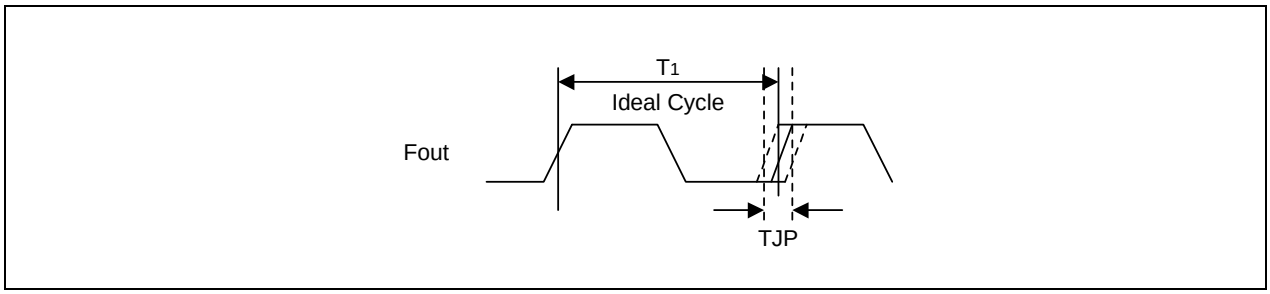
Parameter	Customer	Unit
Long-term jitter (TJLT)		psec (pk-pk)
Tracking Jitter (TJT)		psec (pk-pk)

If you have another special request, please describe below.

JITTER DEFINITION

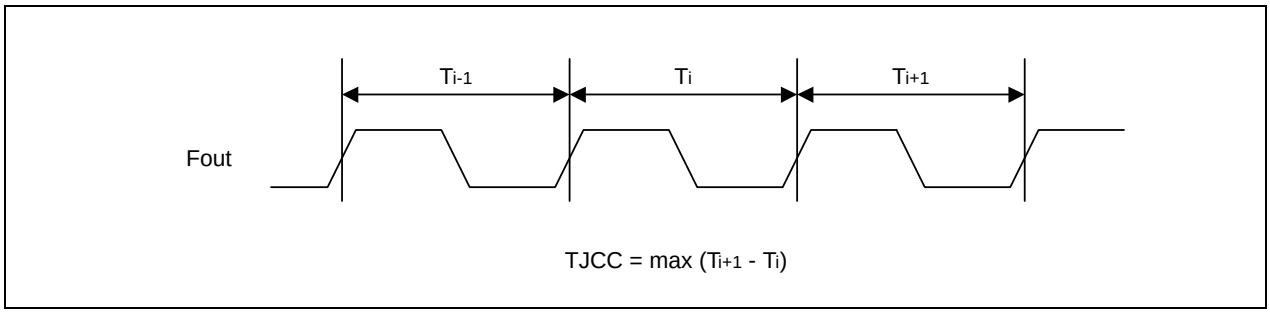
Period Jitter

Period jitter is the maximum deviation of output clock's transition from its ideal position.



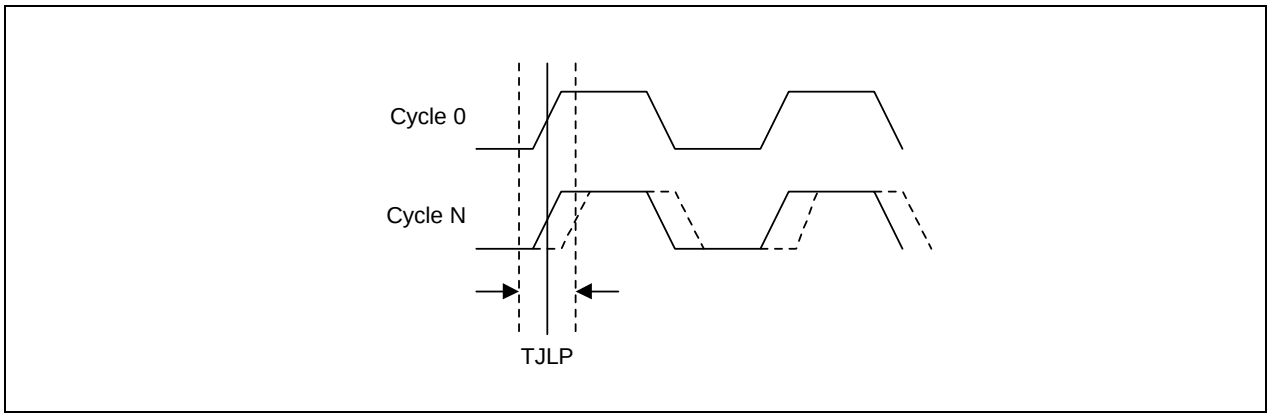
Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the maximum deviation of output clock's transition from its corresponding position of the previous cycle.



Long-Term Jitter

Long-term jitter is the maximum deviation of output clock' transition from its ideal position, after many cycles. The term "many" depends on the application and the frequency.



Tracking Jitter

Tracking jitter is the maximum deviation of output clock(FOUT)'s transition from input clock (FIN) position.