GENERAL DESCRIPTION

The pll2073x is a Phase-Locked Loop (PLL) frequency synthesizer constructed in CMOS on single monolithic structure. The PLL macro-functions provide frequency multiplication capabilities. The output clock frequency FOUT is related to the input clock frequency FIN by the following equation:

$$\mathbf{FOUT = (m \times FIN) / (p \times 2^S)}$$

Where, FOUT is the output clock frequency. FIN is the input clock frequency. m, p and s are the values for programmable dividers. pll2073x consists of a Phase/Frequency Detector(PFD), a Charge Pump, an Internal Loop Filter, a Voltage Controlled Oscillator(VCO), a 6-bit Pre-divider, an 8-bit Main divider and 2-bit Post Scaler as shown in block diagram.

FEATURES

- 0.18um CMOS device technology
- 1.8V single power supply
- Output frequency range: 20 ~ 300MHz
- Jitter: ±120ps at 300MHz
- Duty ratio: 45% to 55% (All tuned range)
- Frequency changed by programmable divider
- Power down mode

NOTES

1. Don't set the P or M as zero, that is 000000 / 00000000
2. The proper range of P and M : $1 \le P \le 62$, $1 \le M \le 248$
3. The P and M must be selected considering stability of PLL and VCO output frequency range
4. Please consult with SEC application engineer to select the proper P, M and S values

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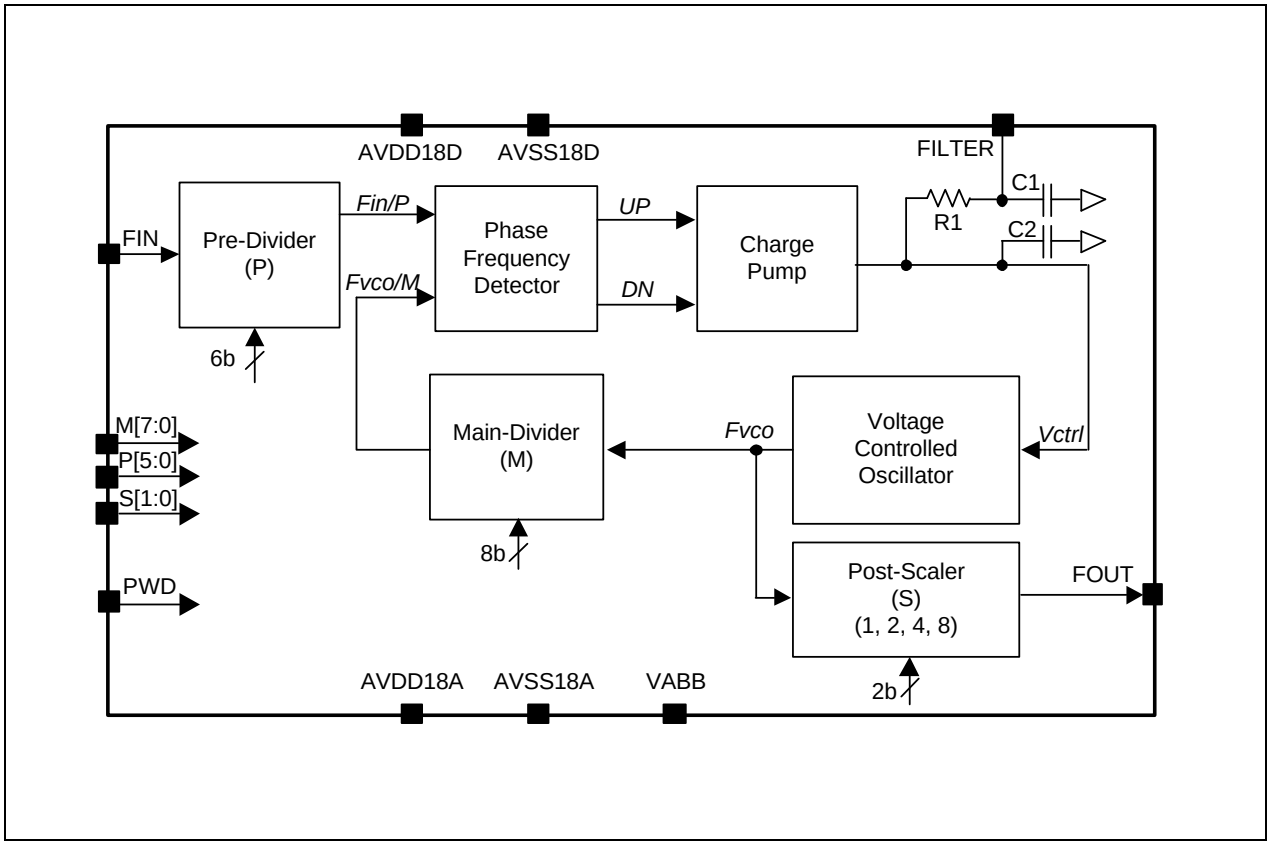
FUNCTIONAL BLOCK DIAGRAM



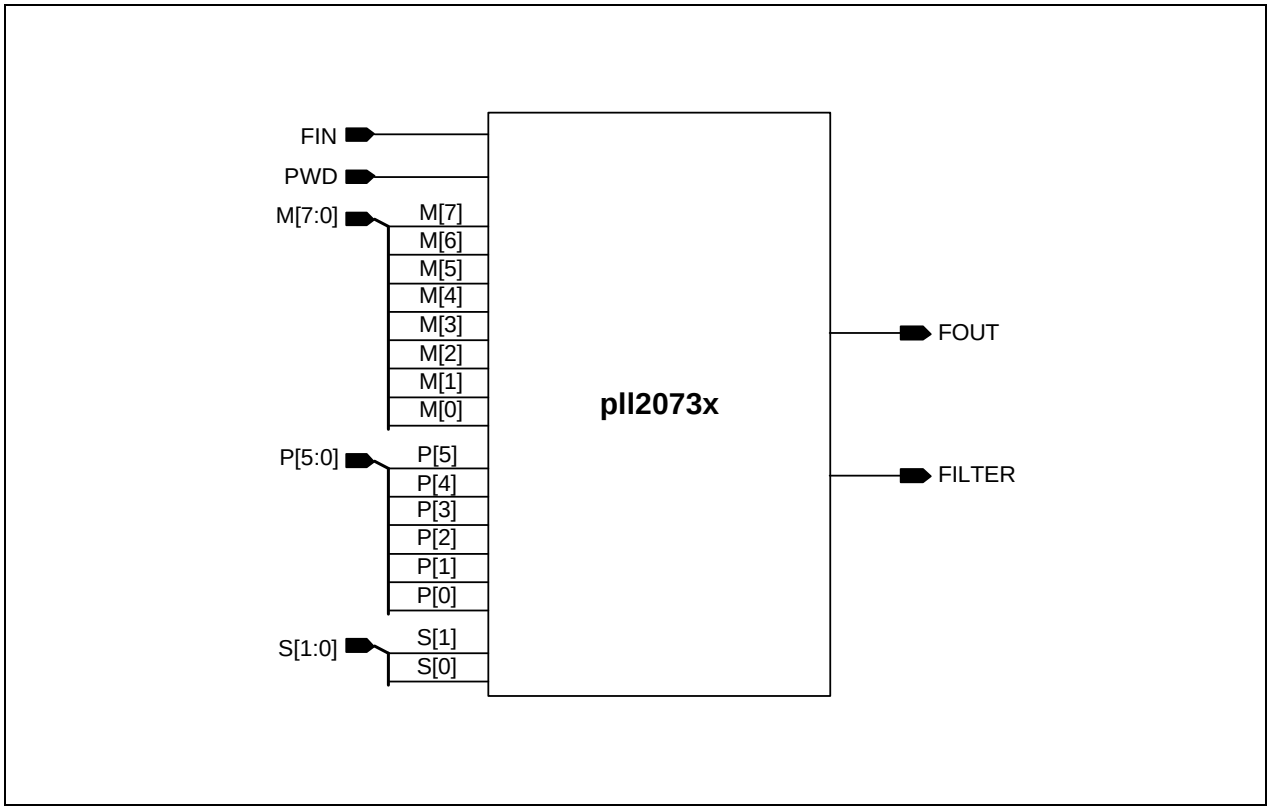
CORE PIN DESCRIPTION

Pin Name	I/O Type	Pin Description
AVDD18D	DP	Digital power supply
AVSS18D	DG	Digital ground
AVDD18A	AP	Analog power supply
AVSS18A	AG	Analog ground
VABB	AB/DB	Analog / Digital bulk bias
FIN	DI	PLL clock input
FOUT	DO	20MHz ~ 300MHz clock output
FILTER	AO	
PWD	DI	Power down. - If PWD is high, power down mode is enabled.
P[5:0]	DI	6-bit programmable pre-divider.
M[7:0]	DI	8-bit programmable main-divider.
S[1:0]	DI	2-bit programmable post-scaler.

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bi-direction
— DB: Digital Bi-direction
— AP: Analog Power
— AG: Analog Ground
— DP: Digital Power
— DG: Digital Ground
— BD: Bi-directional Port

CORE CONFIGURATION



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage differential	AVDD18D-AVDD18A	–0.1		+0.1	V
Operating temperature	Topr	–40		85	°C

NOTE: It is strongly recommended that all the supply pins (AVDD18D, AVDD18A) be powered to the same supply voltage to avoid power latch-up.

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating voltage	AVDD18D/AVDD18A	1.65	1.8	1.95	V
Digital input voltage high	V_{IH}	0.7VDD			V
Digital input voltage low	V_{IL}			0.3VDD	V
Dynamic current	I_{dd}			3	mA
Power down current	I_{pd}			220	uA

AC ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Min	Typ	Max	Unit
Input frequency		F_{IN}	4		40	MHz
Output clock frequency		F_{OUT}	20		300	MHz
VCO output frequency		F_{vco}	160		400	MHz
Input clock duty cycle		T_{ID}	40		60	%
Output clock duty cycle		T_{OD}	45		55	%
Locking time		T_{LT}			150	us
Cycle to cycle jitter	20M ~ 100MHz	T_{JCC}	–300		+300	ps
	100M ~ 200MHz	T_{JCC}	–200		+200	ps
	200M ~ 300MHz	T_{JCC}	–120		+120	ps

NOTE: It is strongly recommended that input signal is not generated glitch, but if consumer cannot help generating glitch, Consumer must carefully considerate the specification.

FUNCTIONAL DESCRIPTION

A PLL is the circuit synchronizing an output signal (generated by an VCO) with a reference or input signal in frequency as well as in phase. The pll2073x can provide frequency multiplication capabilities, but does not guarantee phase synchronization between FIN and FOUT.

In this application, it includes the following basic blocks.

- The voltage-controlled oscillator (VCO) generates VCO output frequency (Fvco) with loop filter DC voltage.
- The Pre-divider divides the input frequency by p.
- The Main-divider divides the Fvco by m.
- The Post-divider divides the Fvco by s and generates FOUT.
- The phase frequency detector detects the phase difference between the reference frequency (=FIN/p) and the feedback frequency (=Fvco/m) and controls the loop filter DC voltage.
- The loop filter removes high frequency components and generates stable DC control voltage for VCO.

The m, p, s values can be programmed by **16-bit digital data** from the external source. So the PLL be locked in the desired frequency.

Fout = m×Fin / p×s (m=M+8 , p=P+2, $s=2^S$)

Digital data format:

Main Divider	Pre Divider	Post Scaler
M7, M6, M5, M4, M3, M2, M1, M0	P5, P4, P3, P2, P1, P0	S1, S0

NOTE: S[1] - S[0]: Output Frequency Scaler
M[7] - M[0] : VCO Frequency Divider
P[5] - P[0] : Input Frequency Divider

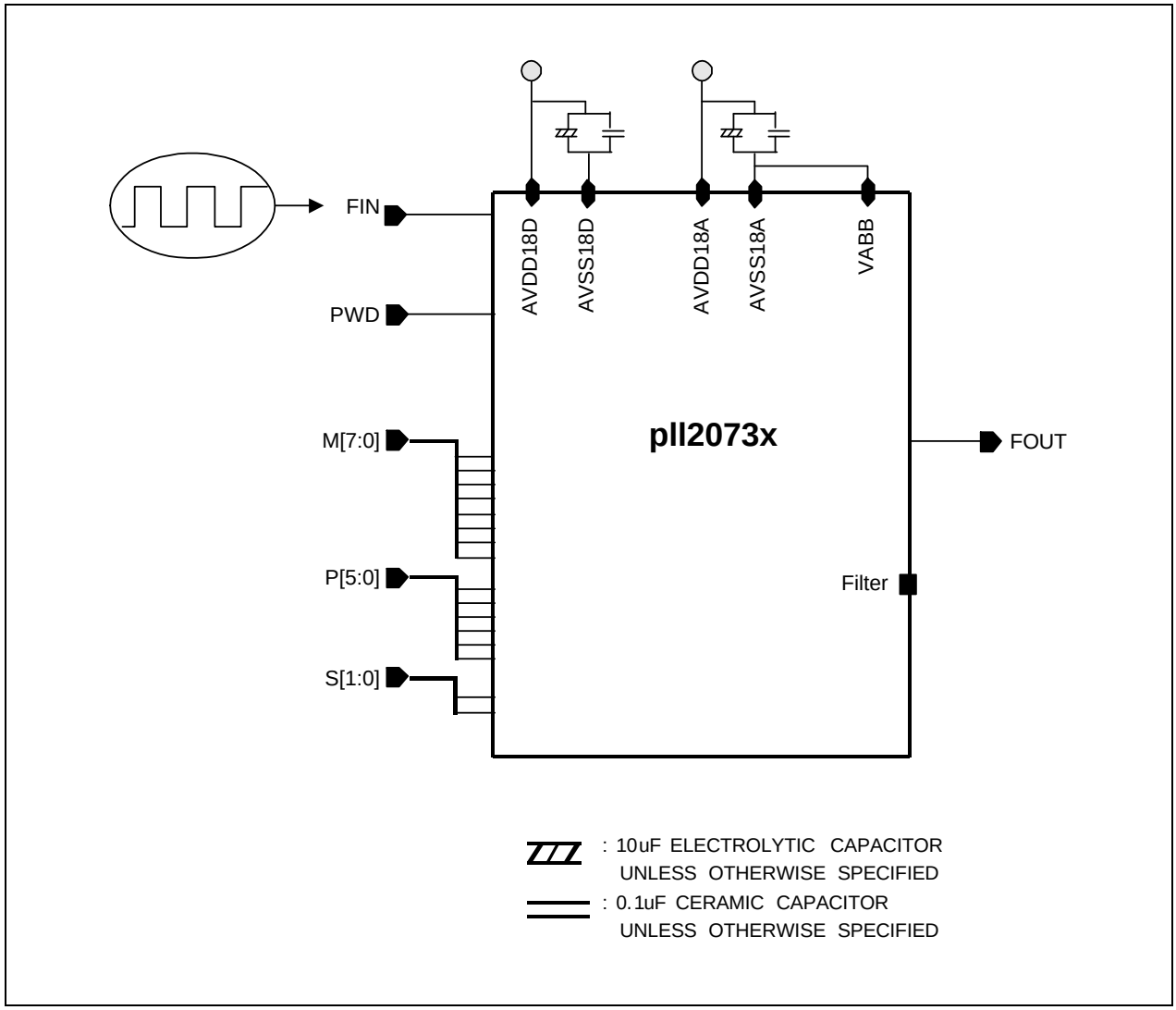
NOTE

Please contact SEC application engineer to confirm the proper selection of M, P, S values.

CORE EVALUATION GUIDE

1. The FOUT should be bypassed for external test.
2. The pll2073x contains loop filter (resistor and capacitor), so the FILTER does not necessarily to be connected to external pin.
   But it is recommended to connect the FILTER to external pin for calibration of loop performance.
3. You can generate various output frequencies by changing M/P/S setting. There are two methods of controlling divider values.
   - Method 1: 16-bit register can be used for easy control of divider values.
   - Method 2: P, M and S pins are bypassed to the external port, and you can control each port directly.

It is undesirable to connect P[5:0], M[7:0] and S[1:0] to the internal power or ground directly.



CORE LAYOUT GUIDE

- The digital power(AVDD18D, AVSS18D) and the analog power(AVDD18A, AVSS18A) must be dedicated to PLL only and separated. If the dedicated AVDD18D and AVSS18D are not allowed, that of the least power consuming block is shared with the PLL.
- The FOUT and FILTER pins must be placed far from the internal signals in order to avoid overlapping signal lines.
- The blocks having a large digital switching current must be located away from the PLL core.
- The PLL core must be shielded by guard ring.
- For the FOUT pad, you can use a custom drive buffer or pot8_abb buffer considering the drive current.

DESIGN CONSIDERATIONS

The following design considerations apply

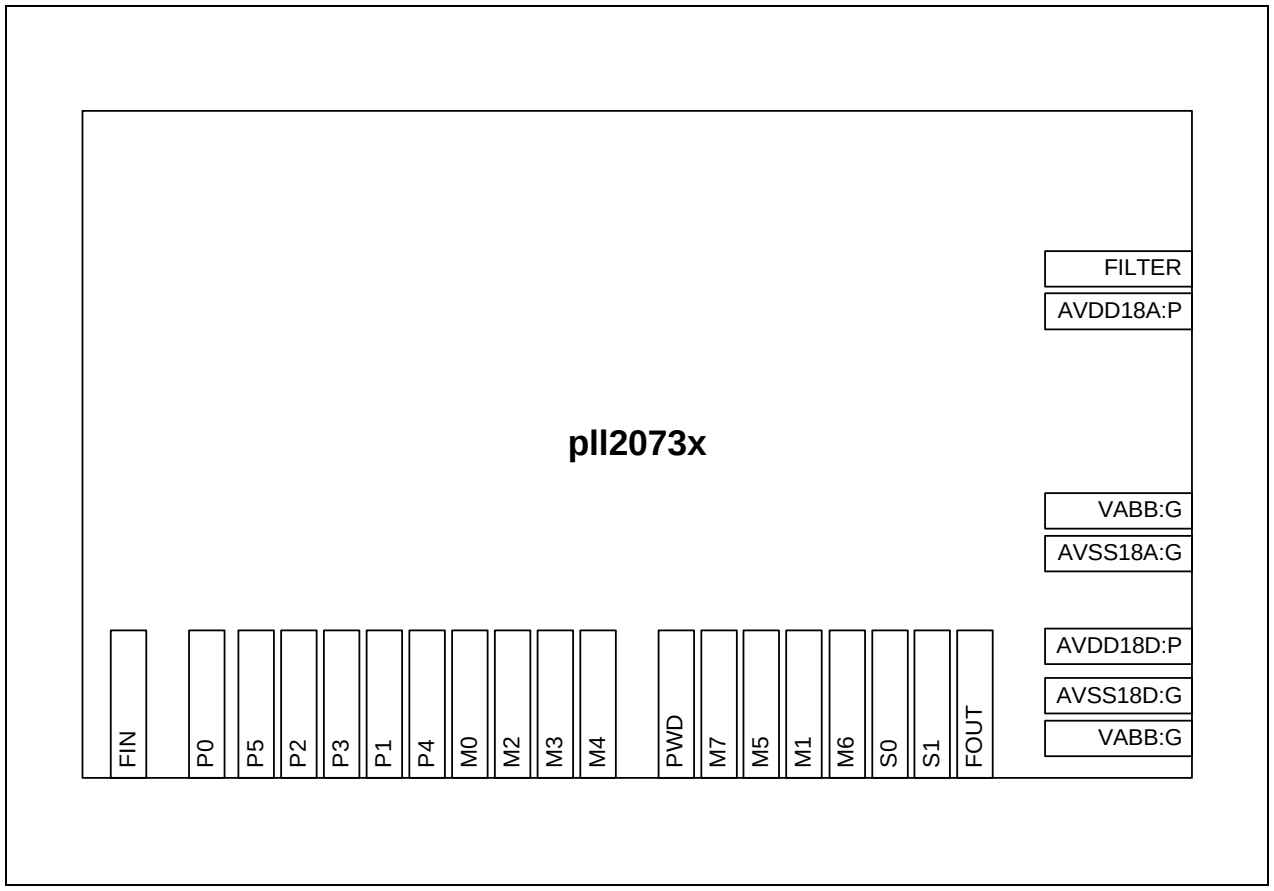
- Jitter is affected by the power noise, substrate noise...etc. It increases when the noise level increases.
- A CMOS-level input reference clock is recommend for signal compatibility with the PLL circuit. Other levels such as TTL may degrade the tolerances.
- The use of two, or more PLLs requires special design considerations. Please consult your application engineer for more information.
- The PLL core should be placed as close as possible to the dedicated loop filter and analog Power and ground pins.
- It is inadvisable to locate noise-generating signals, such as data buses and high-current outputs, near the PLL I/O cells.
- Other related I/O signals should be placed near the PLL I/O but do not have any pre-defined placement restriction.

PHANTOM CELL INFORMATION

Pins of the core can be assigned externally(Package Pins) or internally(Internal Ports) depending on design methods.

— The term "External" implies that the pins should be assigned externally like power pins.

— The term "Internal/External" implies that these pins are user dependent.



PIN LAYOUT GUIDE

Pin Name	Pin Usage	Pin Layout Guide
AVDD18D	External	Use dedicated power/ground pins for PLL Power cuts are required to provide on-chip isolation => between dedicated PLL power/ground and all other power/ground Use good power and ground source on board
AVSS18D	External	
AVDD18A	External	
AVSS18A	External	
VABB	External	
FIN	External	Do not place noisy, high frequency and high power consuming circuitry pads near the FIN. Use proper low jitter reference clock
FOUT	External/Internal	Do not place noisy, high frequency and high power consuming circuitry pads near the FOUT. Internal routing path should be short. This will minimize loading effect. FOUT signals should not be crossed by any signals and should not run next to digital signals. This will minimize capacitive coupling between the two signals.
FILTER	External	Do not place noisy, high frequency and high power consuming circuitry pads near the FILTER. Ground shielding is needed for internal routing path. FILTER routing path should not be crossed by any signals and should not run next to digital signals. External loop filter pin should be placed between analog power and ground to avoid stray coupling outside the chip and magnetic coupling via bond wires. Loop filter components should be placed as close as possible.
PWD	Internal/External	
M[7] ~ M[0]	Internal/External	
P[5] ~ P[0]	Internal/External	
S[1] ~ S[0]	Internal/External	

FEEDBACK REQUEST

Thank you for having an interest in our products. Please fill out this form, especially the items which you want to request.

Parameter		Customer	SEC	Unit
Process			0.18um CMOS	
Supply voltage (VDD)			1.8 ± 0.15	V
Input frequency (FIN)			4 ~ 40	MHz
Output frequency (FOUT)			20 ~ 300	MHz
Cycle to cycle jitter (TJCC)	20M ~ 100M		± 300	psec (pk-pk)
	100M ~ 200M		± 200	
	200M ~ 300M		± 120	
Period jitter (TJP)	20M ~ 100M		± 300	psec (pk-pk)
	100M ~ 200M		± 200	
	200M ~ 300M		± 120	
Output duty ratio (TOD)			45 ~ 55	%
Lock up time (TLT)			150	usec
Dynamic current			< 3m	A
Stand by current			< 220μ	A
Filter capacitor			Internal	–

1. How many PLLs are embedded in your system?
2. Do you need synchronization between input clock and output clock?
3. Do you need another spec of jitter?

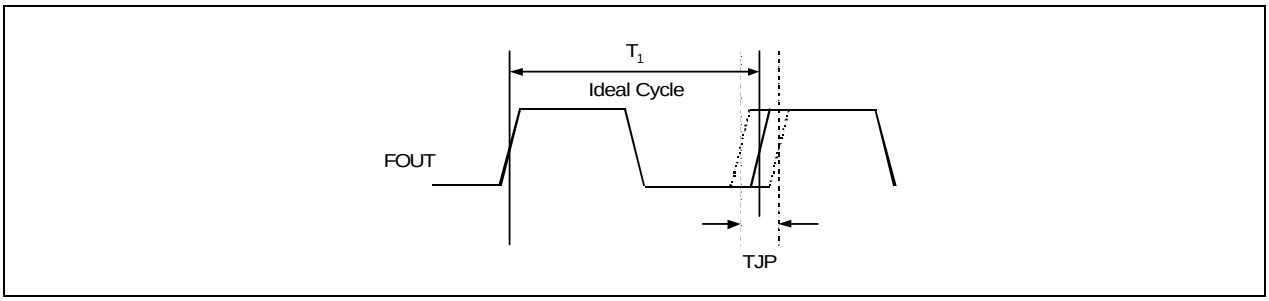
Parameter	Customer	Unit
Long-term Jitter (TJLT)		psec (pk-pk)
Tracking Jitter (TJT)		psec (pk-pk)

If you have another special request, please describe below.

JITTER DEFINITION

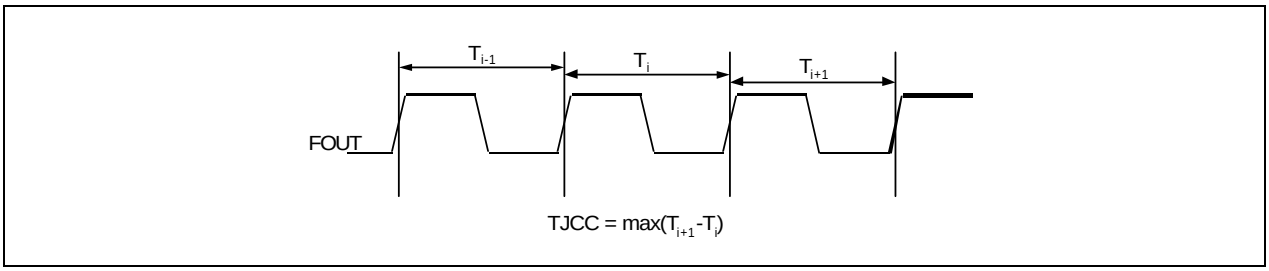
Period Jitter

Period jitter is the maximum deviation of output clock's transition from its ideal position.



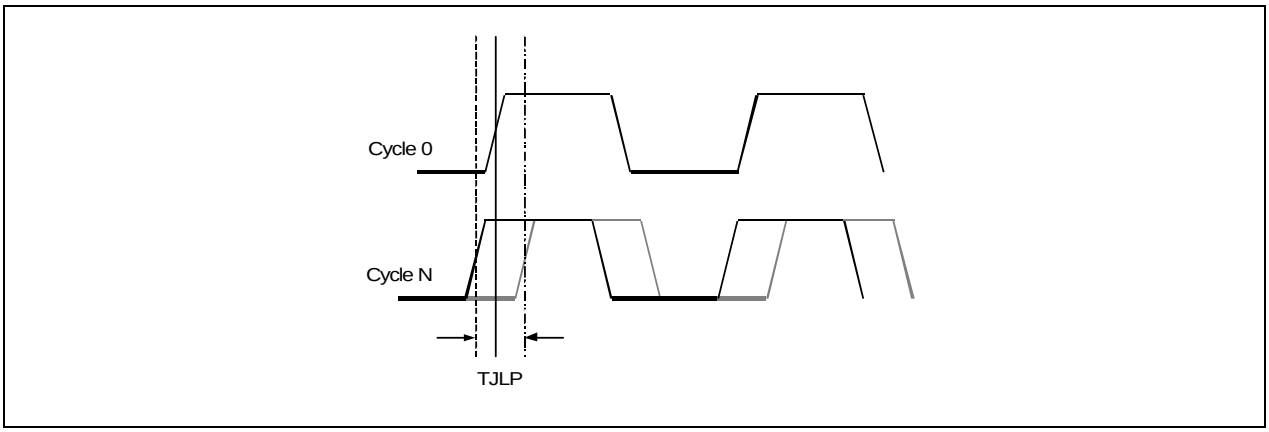
Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the maximum deviation of output clock's transition from its corresponding position of the previous cycle.



Long-Term Jitter

Long-term jitter is the maximum deviation of output clock's transition from its ideal position, after many cycles. The term "many" depends on the application and the frequency.



Tracking Jitter

Tracking jitter is the maximum deviation of output clock(FOUT)'s transition from input clock (FIN) position.