SOLOMON SYSTECH
SEMICONDUCTOR TECHNICAL DATA

SSD1301

Advance Information

OLED/PLED Segment/Common Driver with Controller
CMOS

SSD1301 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SSD1301 consists of 132 high voltage/current driving output pins for driving 132 segments and 64 commons plus 1 icon line driving common. This IC is designed for Common Cathode type OLED panel.

SSD1301 displays data directly from its internal 132x65 bit Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through a pin selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface or I^{2}C Interface.

SSD1301 embeds a contrast control function and an on-chip oscillator for reducing the number of external components.

FEATURES

Support max. 132 x (64+1) matrix panel
Power supply to logic system, 2.4V-3.5V
Power supply to OLED system, 7.0V-16.5V
Segment output maximum current: 400uA
Common sink maximum current: 50mA
Half range and full range current mode selection
Low current sleep mode (<5.0uA)
External current reference control by external resistor
256 steps contrast control on monochrome passive OLED panel
On-Chip Oscillator
Programmable Frame Rate
Solomon Systech Limited's Proprietary OLED Driving Scheme
8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface and I^{2}C Interface
Embedded 132 x 65 bit SRAM display buffer
Row re-mapping and Column re-mapping
Vertical scrolling
Support Partial display
Wide range of operating temperatures: -30 to 85 °C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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● SOLOMON

ORDERING INFORMATION

Ordering Part Number	Package Form
SSD1301TR1	TAB

BLOCK DIAGRAM
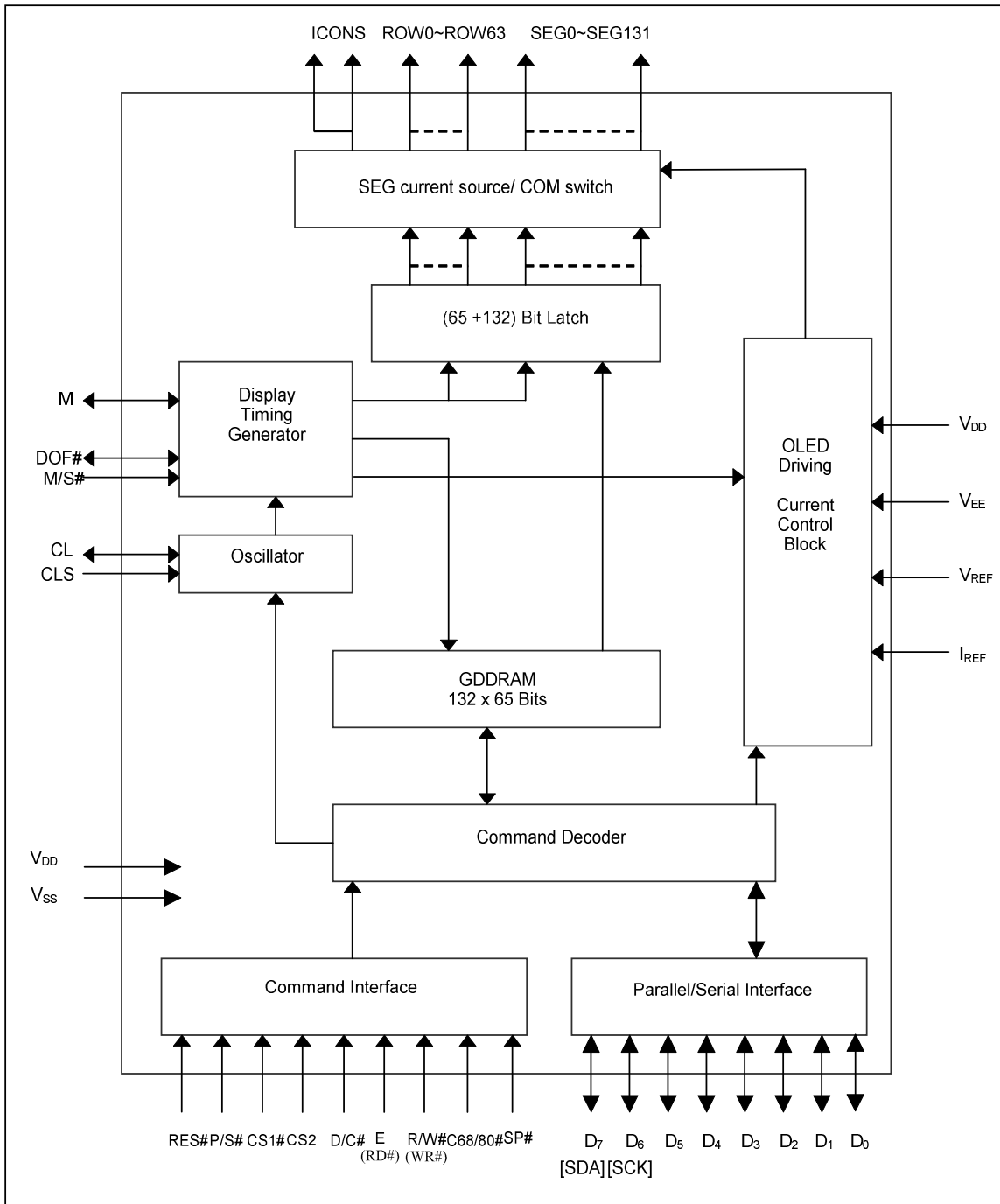
ICONS   ROW0~ROW63   SEG0~SEG131

SEG current source/ COM switch

(65 +132) Bit Latch

Display Timing Generator

M

DOF#
M/S#

Oscillator

CL
CLS

OLED Driving Current Control Block

V_{DD}

V_{EE}

V_{REF}

I_{REF}

GDDRAM
132 x 65 Bits

V_{DD}

V_{SS}

Command Decoder

Command Interface

Parallel/Serial Interface

RES#P/S# CS1#CS2   D/C# E   R/W#C68/80#SP#
                        (RD#) (WR#)

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
[SDA][SCK]

Figure 1 - Block Diagram

SSD1301TR1 PIN ASSIGNMENT

Figure 2 – SSD1301TR1 pin assignment (Copper View)

PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME	PIN NO	PIN NAME
1	NC	61	COM23	121	SEG84	181	SEG24	241	NC
2	VEE	62	COM21	122	SEG83	182	SEG23		
3	IREF	63	COM19	123	SEG82	183	SEG22		
4	VREF	64	COM17	124	SEG81	184	SEG21		
5	VSS	65	COM15	125	SEG80	185	SEG20		
6	VDD	66	COM13	126	SEG79	186	SEG19		
7	VSS	67	COM11	127	SEG78	187	SEG18		
8	SP#	68	COM9	128	SEG77	188	SEG17		
9	P/S#	69	COM7	129	SEG76	189	SEG16		
10	C68/80#	70	COM5	130	SEG75	190	SEG15		
11	VSS	71	COM3	131	SEG74	191	SEG14		
12	CLS	72	COM1	132	SEG73	192	SEG13		
13	M/S#	73	NC	133	SEG72	193	SEG12		
14	VDD	74	SEG131	134	SEG71	194	SEG11		
15	D7	75	SEG130	135	SEG70	195	SEG10		
16	D6	76	SEG129	136	SEG69	196	SEG9		
17	D5	77	SEG128	137	SEG68	197	SEG8		
18	D4	78	SEG127	138	SEG67	198	SEG7		
19	D3	79	SEG126	139	SEG66	199	SEG6		
20	D2	80	SEG125	140	SEG65	200	SEG5		
21	D1	81	SEG124	141	SEG64	201	SEG4		
22	D0	82	SEG123	142	SEG63	202	SEG3		
23	VDD	83	SEG122	143	SEG62	203	SEG2		
24	E(RD#)	84	SEG121	144	SEG61	204	SEG1		
25	R/W#	85	SEG120	145	SEG60	205	SEG0		
26	D/C#	86	SEG119	146	SEG59	206	ICONS		
27	RES#	87	SEG118	147	SEG58	207	COM0		
28	VDD	88	SEG117	148	SEG57	208	COM2		
29	CS2	89	SEG116	149	SEG56	209	COM4		
30	CS1#	90	SEG115	150	SEG55	210	COM6		
31	VSS	91	SEG114	151	SEG54	211	COM8		
32	DOF#	92	SEG113	152	SEG53	212	COM10		
33	CLS	93	SEG112	153	SEG52	213	COM12		
34	M	94	SEG111	154	SEG51	214	COM14		
35	VEE	95	SEG110	155	SEG50	215	COM16		
36	NC	96	SEG109	156	SEG49	216	COM18		
37	NC	97	SEG108	157	SEG48	217	COM20		
38	NC	98	SEG107	158	SEG47	218	COM22		
39	NC	99	SEG106	159	SEG46	219	COM24		
40	ICONS	100	SEG105	160	SEG45	220	COM26		
41	COM63	101	SEG104	161	SEG44	221	COM28		
42	COM61	102	SEG103	162	SEG43	222	COM30		
43	COM59	103	SEG102	163	SEG42	223	COM32		
44	COM57	104	SEG101	164	SEG41	224	COM34		
45	COM55	105	SEG100	165	SEG40	225	COM36		
46	COM53	106	SEG99	166	SEG39	226	COM38		
47	COM51	107	SEG98	167	SEG38	227	COM40		
48	COM49	108	SEG97	168	SEG37	228	COM42		
49	COM47	109	SEG96	169	SEG36	229	COM44		
50	COM45	110	SEG95	170	SEG35	230	COM46		
51	COM43	111	SEG94	171	SEG34	231	COM48		
52	COM41	112	SEG93	172	SEG33	232	COM50		
53	COM39	113	SEG92	173	SEG32	233	COM52		
54	COM37	114	SEG91	174	SEG31	234	COM54		
55	COM35	115	SEG90	175	SEG30	235	COM56		
56	COM33	116	SEG89	176	SEG29	236	COM58		
57	COM31	117	SEG88	177	SEG28	237	COM60		
58	COM29	118	SEG87	178	SEG27	238	COM62		
59	COM27	119	SEG86	179	SEG26	239	NC		
60	COM25	120	SEG85	180	SEG25	240	NC		

Table 1 : SSD1301TR1 pin assignment

PIN DESCRIPTION

M, DOF#

These pins are No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

CL

This pin is the system clock input. When internal clock is enabled, this pin should be left open. Nothing should be connected to this pin. When internal oscillator is disabled, this pin receives display clock signal from external clock source.

CS1#, CS2

These pins are the chip select inputs. The chip is enabled for MCU communication only when CS1# is pulled low and CS2 is pulled high.

RES#

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

D/C#

This pin is Data/Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as display data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

R/W#(WR#)

This pin is MCU interface input. When interfacing to an 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.

E (RD#)

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.

D_7-D_0

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D_7 will be the serial data input SDA and D_6 will be the serial clock input SCK.

When I^2C mode is selected, D_4 will be the clock signal (SCL) and D_5 will be the salve address (SA0). If read register status and write data are necessary, D_0 should be connected with D_1 as SDA bus. If only write data is necessary, D_1 will be SDA bus and D_0 should be left open.

V_{DD}

Power Supply pin. This is also the reference for the OLED driving voltages. It must be connected to external source.

V_{DD1}

Internally connected to V_{DD} for pull high purpose.

V_{DD2}

Internally connected to V_{DD}.

V_{SS}

Ground. It also acts as a reference for the logic pins. It must be connected to external ground.

V_{SS1}

Internally connected to V_{SS} for pull low purpose.

V_{EE}

This is the most negative voltage supply pin of the chip. It is supplied externally.

M/S#

This pin is the selection input. This pin must be pulled high to enable the chip function.

CLS

This pin is internal clock enable. When this pin is pulled high, internal clock is enabled.

The internal clock will be disabled when it is pulled low, an external clock source must be connected to CL pin for normal operation.

C68/80#

This pin is MCU parallel interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin is pulled low, 8080 series interface is selected.

If Serial Interface is selected (P/S# and SP# pulled low), the setting of this pin is ignored, but must be connected to a known logic (either high or low).

P/S#

This pin is parallel interface selection input. When this pin is pulled high, parallel interface mode is selected. When this pin and SP# pins are pulled low, serial interface is selected.

Note: Read data operation is only available in parallel mode.

ROW0-ROW63

These pins provide the Common switch signals to the OLED panel.

SEG0-SEG131

These pins provide the OLED segment driving signals. The output voltage level of these pins is in high impedance stage when display is off.

ICONS

There are two ICONS pin on the chip. They are the common pin for the icon row. Both pins output exactly the same signal. The reason for duplicating the pin is to enhance the flexibility of the OLED layout.

V$_{REF}$

This pin is the reference for OLED driving voltages. It is supplied externally.

I$_{REF}$

This pin is current reference pin. A resistor should be connected between this pin and V$_{EE}$.

SP#

This pin is serial interface selection input. When this pin and P/S# pulled low, serial interface mode is selected.

TESTIN, TESTOUT

They are reserved pins. TESTIN must be connected to V$_{SS}$ and TESTOUT must be left open.

Note: Refer to Appendix I for the configuration of I^{2}C Interface.

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D_7-D_0 is interpreted as a Command and it will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/W#(WR#), D/C#, E (RD#), CS1# and CS2. R/W#(WR#) input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. RW#/ (WR#) input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C# input. The E (RD#) input serves as data latch signal (clock) when high provided that CS1# and CS2 are low and high respectively. Refer to Figure 8 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below.
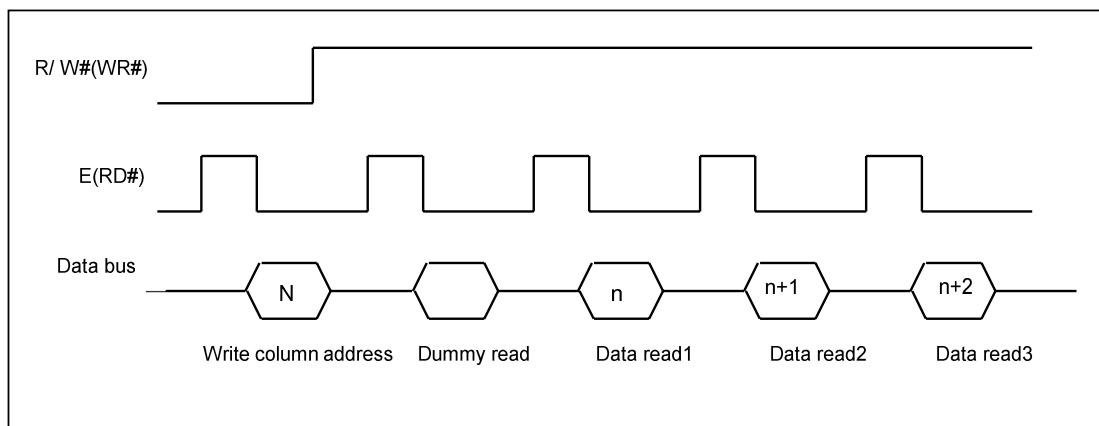
Figure 3 : Display Data Read Back Procedure - Insertion of Dummy Read

MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), E (RD#), R/W#(WR#), D/C#, CS1# and CS2. The E (RD#) input serves as data read latch signal (clock) when low, provided that CS1# and CS2 are low and high respectively. Display data or status register read is controlled by D/C#.

R/W# (WR#) input serves as data write latch signal (clock) when high provided that CS1# and CS2 are low and high respectively. Display data or command register write is controlled by D/C#. Refer to Figure 8 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial Interface

The serial interface consists of serial clock SCK, serial data SDA, D/C#, CS1# and CS2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D_7, D_6, ... D_0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The oscillator generates the clock for the Display Timing Generator.
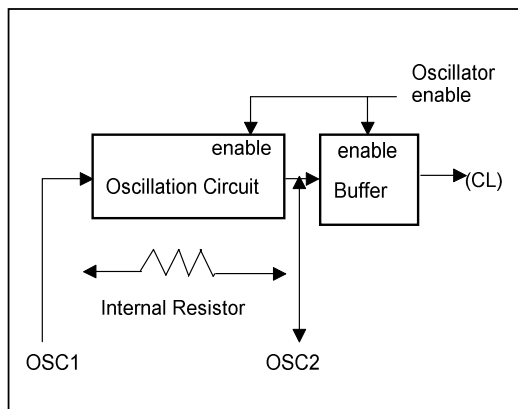

Figure 4 : Oscillator Circuit

OLED Driving Current Control Block

This block is used to divide the incoming power sources into the different levels of internal use voltage and current. V_{EE} and V_{DD} are external power supplies. V_{REF} is reference voltage, which is used to deliver a reference voltage for Seg Cells. I_{REF} is a reference current source for Seg Cells current drivers.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 65 = 8580 bits. Figure 5 on page 12 is a description of the GDDRAM address map.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display. Figure 5 on page 12 shows the case in which the display start line register is set to 38h.

For those GDDRAM out of the display common range, they could still be accessed, for either preparation of vertical scrolling data or even for the system usage.

Reset Circuit

When RES# input is low, the chip is initialized with the following status:
1. Display is OFF
2. 132x64 [Not included ICONS line] Display Mode
3. Normal segment and display data column address mapping(SEG0 mapped to address 00H)
4. Read-modify-write mode is OFF
5. Shift register data clear in serial interface
6. Display start line is set at display RAM address 0
7. Column address counter is set at 0
8. Page address is set at 0
9. Normal scan direction of the COM outputs
10. Contrast control register is set at 20H
11. Test mode is OFF
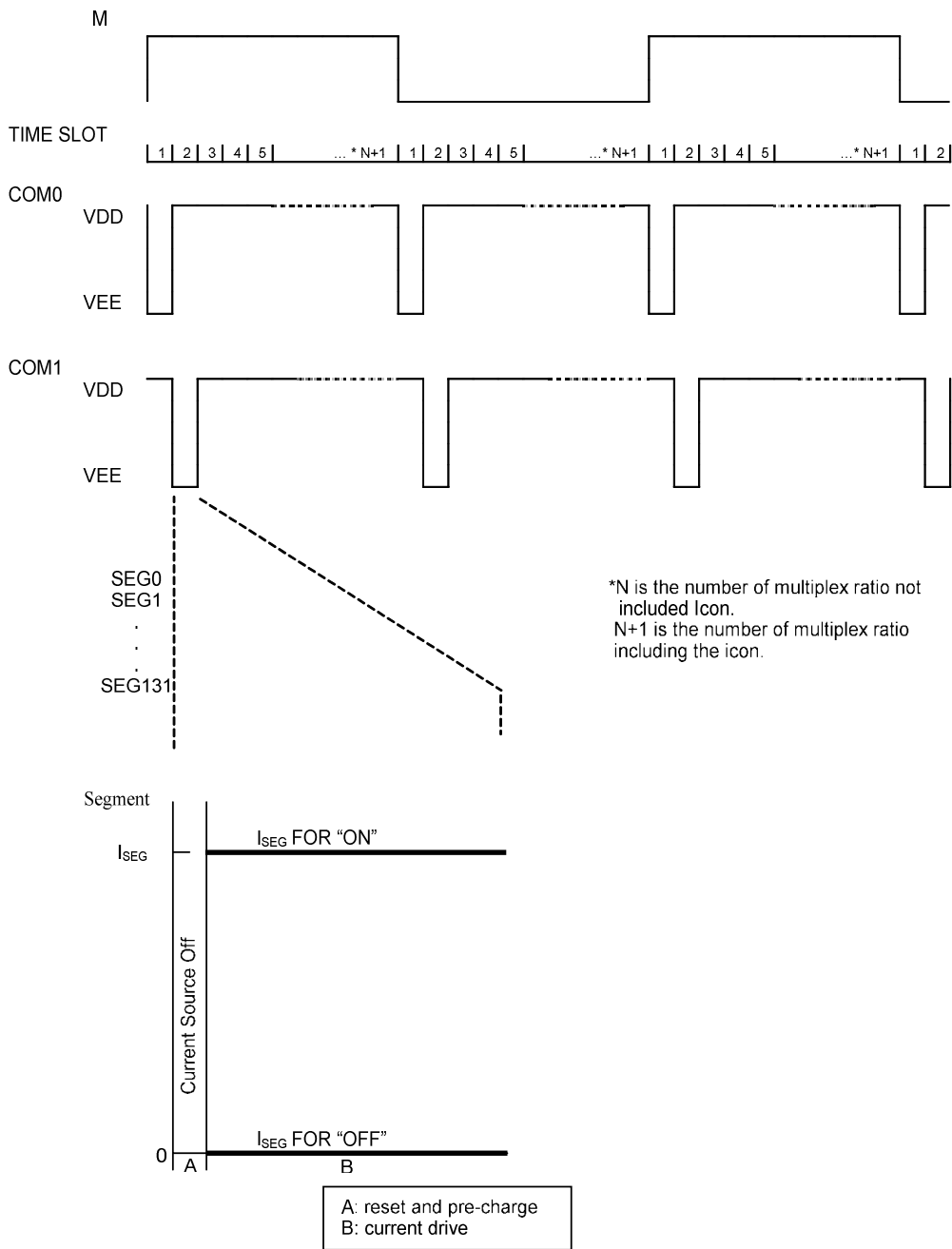12. Current mode is set to half range current mode

197 Bit Latch

A register carries the display signal information. In 132x65 display mode, data will be fed to the Seg/Com Cell and output to the required voltage/current level respectively.

Seg/Com Cell

Seg current source drivers deliver 132 current sources to drive OLED panel. It uses current source to drive the SegCell where the driving current can be adjusted from 0 to 400 uA with 256 steps. Com cell is the voltage scanning pulse as shown in Figure 6.

Figure 5 : Graphic Display Data RAM (GDDRAM) Address Map with Display Start Line set to 38h.

M

TIME SLOT

| 1 | 2 | 3 | 4 | 5 | ... * N+1 | 1 | 2 | 3 | 4 | 5 | ...* N+1 | 1 | 2 | 3 | 4 | 5 | ...* N+1 | 1 | 2 |

COM0
VDD

VEE

COM1
VDD

VEE

SEG0
SEG1
.
.
.
SEG131

*N is the number of multiplex ratio not
 included Icon.
N+1 is the number of multiplex ratio
including the icon.

Segment

I_{SEG}

I_{SEG} FOR "ON"

Current Source Off

I_{SEG} FOR "OFF"

0

A

B

A: reset and pre-charge
B: current drive

Figure 6 : OLED Driving Waveform

COMMAND TABLE

Table 2 : Command Table (D/C# =0, R/W#(WR#)=0, E (RD#)=1)

Bit Pattern	Command	Description
$0000X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
$0001X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after POR.
$01X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 during POR.
10000001 $X_7X_6X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Double byte command to select 1 out of 256 contrast steps. Contrast increases as $X_7X_6X_5X_4X_3X_2X_1X_0$ is increased from 00000000b to 11111111b. $X_7X_6X_5X_4X_3X_2X_1X_0$ =10000000b after POR
$1010000X_0$	Set Segment Re-map	X_0=0: column address 00H is mapped to SEG0 (POR) X_0=1: column address 83H is mapped to SEG0
$1010010X_0$	Set Entire Display On/Off	X_0=0: normal display (POR) X_0=1: entire display on
$1010011X_0$	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
$1010111X_0$	Set Display On/Off	X_0=0: turns off OLED panel (POR) X_0=1: turns on OLED panel
$1011X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0~8) for read/write using $X_3X_2X_1X_0$
$1100X_3$ * * *	Set COM Output Scan Direction	X_3=0: normal mode (POR) X_3=1: remapped mode. COM0 to COM[N-1] becomes COM[N-1] to COM0 in Multiplex ratio is equal to N. See Fig.5 as an example for N equal to 64.
11100000	Set Read-Modify-Write Mode	Read-Modify-Write mode will be entered in which the column address will not be increased during display data read. After POR, Read-modify-write mode is turned OFF
11100010	Software Reset	Initialize internal status registers
11101110	Set End of Read-Modify-Write Mode	Exit Read-Modify-Write mode. RAM Column address before entering the mode will be restored. After POR, Read-modify-write mode is OFF.
11100011	NOP	Command for No Operation
1111 * * * *	Set Test Mode	Reserved for IC testing. Do NOT use.
* * * * * * * *	Set Power Save Mode	Sleep mode will be entered with compound commands

Bit Pattern	Command	Description
10101000 **$X_5X_4X_3X_2X_1X_0$	Set Multiplex Ratio	To select multiplex ratio N from 2 to the maximum multiplex ratio (POR value) (including icon line). Max. mux ratio: 65 N= $X_5X_4X_3X_2X_1X_0$+2, e.g. N=001111b+2=17
10101010 *10$X_4X_3X_2X_1X_0$	Set Frame Frequency	$X_4X_3X_2X_1X_0$ =00001: $\dfrac{F_{osc}}{4 \times 65}$ $X_4X_3X_2X_1X_0$ =11111: $\dfrac{F_{osc}}{6 \times 65}$ (POR) $X_4X_3X_2X_1X_0$ =00011: $\dfrac{F_{osc}}{8 \times 65}$
1101000X_0	Set Icon Mode	X_0=0: icon mode off (POR) X_0=1: icon mode on
11011010 ***1**$X_1$0	Set Current Mode	X_1=0: Select half range current mode (POR) X_1=1: Select full range current mode

Note: Remark "*" stands for "Don't Care"

Table 3 : Read Command Table (D/C#=0, R/W#(WR#)=1, E(RD#)=1 for 6800 or E(RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read	D_7=0: indicates the driver is ready for command. D_7=1: indicates the driver is Busy. D_6=0: indicates reverse segment mapping with column address D_6=1: indicates normal segment mapping with column address D_5=0: indicates the display is ON D_5=1: indicates the display is OFF D_4=0: initialization is not in progress D_4=1: initialization is in progress after RES# or software reset

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

Data Read / Write

To read data from the GDDRAM, input High to R/W#(WR#) pin and D/C# pin for 6800-series parallel mode, Low to E (RD#) pin and High to D/ C# pin for 8080-series parallel mode. No data read is provided for serial mode.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read. However, no automatic increase will be performed in read-modify-write mode.

Also, a dummy read is required before the first data read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/W#(WR#) pin and High to D/C# pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

It should be noted that, after the automatic column address increment, the pointer will NOT wrap round to 0 when overflow (>131). The increment of the pointer will stop at 131. Therefore, there is a need to re-initialize the pointer when progresses to another page address.

Address Increment Table (Automatic)

D/C#	R/W#(WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes*1

*1. If read-data command is issued in read-modify-write mode, address increase is not applied.

COMMAND DESCRIPTIONS

Set Lower Column Address
  This command specifies the lower nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Higher Column Address
  This command specifies the higher nibble of the 8-bit column address of the display data RAM. The column address will be incremented by each data access after it is pre-set by the MCU.

Set Display Start Line
  This command is to set **Display Start Line** register to determine starting address of display RAM to be displayed by selecting a value from 0 to 63. With value equals to 0, D_0 of Page 0 is mapped to COM0. With value equals to 1, D_1 of Page0 is mapped to COM0. The display start line values of 0 to 63 are assigned to Page 0 to 7.

Set Contrast Control Register
  This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increase with the increase of contrast step. See Fig 7a below. From Fig 7b, it shows that the output uniformity is better at highest contrast setting. Therefore, for both full range current mode and half range current mode, it is recommended choosing a higher contrast setting if possible.
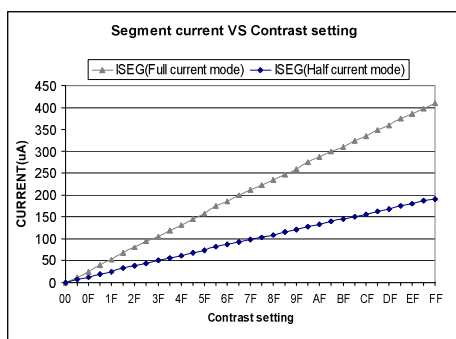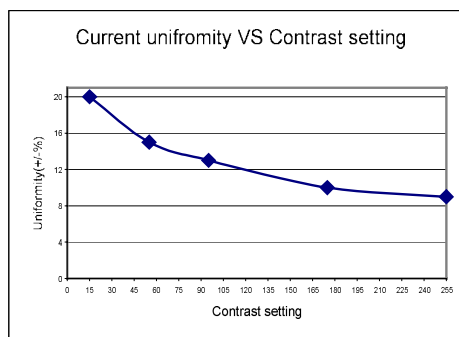

Figure 7a : Segment current vs Contrast setting

Figure 7b : Current uniformity vs Contrast setting

Set Segment Re-map
  This command changes the mapping between the display data column address and segment driver. It allows flexibility in layout during OLED module assembly. Refer to Table 2.

Set Entire Display On/Off
  This command forces the entire display, including the icon row, to be "ON" regardless of the contents of the display data RAM. This command has priority over normal/reverse display. This command will be used with "Set Display ON/OFF" command to form a compound command for entering power save mode. See "Set Power Save Mode".

Set Normal/Reverse Display
  This command sets the display to be either normal/reverse. In normal display, a RAM data of 1 indicates an "ON" pixel while in reverse display, a RAM data of 0 indicates an "ON" pixel. In icon mode, the icon line is not reversed by this command.

Set Display On/Off
  This command alternatively turns the display on and off. When display off is issued with entire display on, power save mode will be entered. See "Set Power Save Mode" for details.

Set Page Address
  This command positions the page address to 0 to 8 possible positions in GDDRAM. Refer to Table 2.

Set COM Output Scan Direction
  This command sets the scan direction of the COM output allowing layout flexibility in OLED module assembly. See Figure 5 on Page 12 for the relationship between turning on or off of this feature.
  In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

Set Read-Modify-Write Mode
  This command puts the chip in read-modify-write mode in which:
  1. The column address is saved before entering the mode
  2. The column address is incremented by display data write but not by display data read

Table 4 : ROW pins assignment for COM signals in Programmable Multiplex Ratio

Die Pad Name	64 Mux Com Signal Output	54 Mux Com Signal Output	53 Mux Com Signal Output	49 Mux Com Signal Output	48 Mux Com Signal Output	33 Mux Com Signal Output	32 Mux Com Signal Output	16 Mux Com Signal Output
ROW0	COM0	COM0	COM0	COM0	COM0	COM0	COM0	COM0
ROW1	COM1	COM1	COM1	COM1	COM1	COM1	COM1	COM1
ROW2	COM2	COM2	COM2	COM2	COM2	COM2	COM2	COM2
ROW3	COM3	COM3	COM3	COM3	COM3	COM3	COM3	COM3
ROW4	COM4	COM4	COM4	COM4	COM4	COM4	COM4	COM4
ROW5	COM5	COM5	COM5	COM5	COM5	COM5	COM5	COM5
ROW6	COM6	COM6	COM6	COM6	COM6	COM6	COM6	COM6
ROW7	COM7	COM7	COM7	COM7	COM7	COM7	COM7	COM7
ROW8	COM8	COM8	COM8	COM8	COM8	COM8	COM8	COM8
ROW9	COM9	COM9	COM9	COM9	COM9	COM9	COM9	COM9
ROW10	COM10	COM10	COM10	COM10	COM10	COM10	COM10	COM10
ROW11	COM11	COM11	COM11	COM11	COM11	COM11	COM11	COM11
ROW12	COM12	COM12	COM12	COM12	COM12	COM12	COM12	COM12
ROW13	COM13	COM13	COM13	COM13	COM13	COM13	COM13	COM13
ROW14	COM14	COM14	COM14	COM14	COM14	COM14	COM14	COM14
ROW15	COM15	COM15	COM15	COM15	COM15	COM15	COM15	COM15
ROW16	COM16	COM16	COM16	COM16	COM16	COM16	COM16	NON-SELECT*
ROW17	COM17	COM17	COM17	COM17	COM17	COM17	COM17	NON-SELECT*
ROW18	COM18	COM18	COM18	COM18	COM18	COM18	COM18	NON-SELECT*
ROW19	COM19	COM19	COM19	COM19	COM19	COM19	COM19	NON-SELECT*
ROW20	COM20	COM20	COM20	COM20	COM20	COM20	COM20	NON-SELECT*
ROW21	COM21	COM21	COM21	COM21	COM21	COM21	COM21	NON-SELECT*
ROW22	COM22	COM22	COM22	COM22	COM22	COM22	COM22	NON-SELECT*
ROW23	COM23	COM23	COM23	COM23	COM23	COM23	COM23	NON-SELECT*
ROW24	COM24	COM24	COM24	COM24	COM24	COM24	COM24	NON-SELECT*
ROW25	COM25	COM25	COM25	COM25	COM25	COM25	COM25	NON-SELECT*
ROW26	COM26	COM26	COM26	COM26	COM26	COM26	COM26	NON-SELECT*
ROW27	COM27	COM27	COM27	COM27	COM27	COM27	COM27	NON-SELECT*
ROW28	COM28	COM28	COM28	COM28	COM28	COM28	COM28	NON-SELECT*
ROW29	COM29	COM29	COM29	COM29	COM29	COM29	COM29	NON-SELECT*
ROW30	COM30	COM30	COM30	COM30	COM30	COM30	COM30	NON-SELECT*
ROW31	COM31	COM31	COM31	COM31	COM31	COM31	COM31	NON-SELECT*
ROW32	COM32	COM32	COM32	COM32	COM32	COM32	NON-SELECT*	NON-SELECT*
ROW33	COM33	COM33	COM33	COM33	COM33	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW34	COM34	COM34	COM34	COM34	COM34	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW35	COM35	COM35	COM35	COM35	COM35	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW36	COM36	COM36	COM36	COM36	COM36	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW37	COM37	COM37	COM37	COM37	COM37	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW38	COM38	COM38	COM38	COM38	COM38	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW39	COM39	COM39	COM39	COM39	COM39	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW40	COM40	COM40	COM40	COM40	COM40	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW41	COM41	COM41	COM41	COM41	COM41	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW42	COM42	COM42	COM42	COM42	COM42	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW43	COM43	COM43	COM43	COM43	COM43	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW44	COM44	COM44	COM44	COM44	COM44	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW45	COM45	COM45	COM45	COM45	COM45	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW46	COM46	COM46	COM46	COM46	COM46	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW47	COM47	COM47	COM47	COM47	COM47	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW48	COM48	COM48	COM48	COM48	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW49	COM49	COM49	COM49	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW50	COM50	COM50	COM50	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW51	COM51	COM51	COM51	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW52	COM52	COM52	COM52	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW53	COM53	COM53	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW54	COM54	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW55	COM55	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW56	COM56	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW57	COM57	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW58	COM58	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW59	COM59	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW60	COM60	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW61	COM61	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW62	COM62	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*
ROW63	COM63	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*	NON-SELECT*

Remark:
*The ROW will output a Non-Select COM signal.

Software Reset
     This command causes some of the internal status of the chip to be initialized:
     1.   Read-Modify-Write mode is off
     2.   Display start line register is set to 0
     3.   Column address counter is set to 0
     4.   Page address is set to 0
     5.   Normal scan direction of the COM outputs

Set End of Read-Modify-Write Mode
     This command relieves the chip from read-modify-write mode. The column address saved before entering read-modify-write mode will be restored.

NOP
     No Operation Command

Set Test Mode
     This command forces the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use this command.

Set Power Save Mode
     To enter Sleep Mode, it should be done by using a double byte command composed of "Set Display ON/OFF" and "Set Entire Display ON/OFF" commands. When "Set Entire Display ON" is issued during display is OFF, Sleep Mode will be entered.
     For Sleep mode:
     1.   Internal oscillator and OLED power supply circuits are stopped
     2.   Segment and Common drivers output high impedance level
     3.   The display data and operation mode before sleep are held
     4.   Internal display RAM can still be accessed
     5.   Sleep Mode can be exited by the issue of a new software command or by pulling Low at hardware pin RES#.

Status register Read
     This command is issued by setting D/C# Low during a data read (refer to Figure 8 and Figure 9 parallel interface waveform). It allows the MCU to monitor the internal status of the chip. No status read is provided for serial mode.

Set Multiplex Ratio
     This command switches default 65 multiplex mode to any multiplex mode from 2 to 65. The output pads ROW0-ROW63 will be switched to corresponding COM signal. (See Table 4)

Set Frame Frequency
     This command is used to select Frame Frequency. In SSD1301, there are three choices for frame frequency.

Set Icon Mode
     This command enables or disables the icon mode. The default setting (POR) disables the icon mode.

Set Current Mode
     This command is used to select half range current mode or full range current mode. In POR, half range current mode is default.

MAXIMUM RATINGS

Table 5 : Maximum Ratings (Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4	V
V_{EE}		0 to V_{DD}-16.5	V
V_{in}	Input voltage	Vss-0.3 to Vdd+0.3	V
T_A	Operating Temperature	-30 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

DC CHARACTERISTICS

Table 6 : DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25ºC)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{EE}	Operating Voltage		-13.0	-9	-4.6	V
V_{DD}	Logic Supply Voltage		2.4	2.7	3.5	V
V_{OH}	High Logic Output Level	Iout =100uA, 3.3MHz	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	Iout =100uA, 3.3MHz	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	Iout =100uA, 3.3MHz	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	Iout =100uA, 3.3MHz	0	-	0.2*V_{DD}	V
I_{SLEEP}	Sleep mode Current	VDD=2.7V, IREF=8uA, Display On, no panel attached	-	0.2	5	uA
I_{EE}	V_{EE} Supply Current	Contrast = FF	-680	-580		uA
	VDD=2.7V, VEE=-9V, IREF=8uA, Frame rate = 85Hz, Contrast = FF, All one pattern, Display on, no loading	Contrast = AF		-480		
I_{DD}	V_{DD} Supply Current VDD=2.7V, VEE=-9V, IREF=8uA, Frame rate = 85Hz, Contrast = FF, All one pattern, Display on, no loading	Contrast = FF	-	600	700	uA
	Power Consumption = (I_{DD}+I_{EE}) V_{DD} - (V_{DD}-V_{EE}) I_{EE}	Contrast = AF		500		
I_{SEG}	Full Range Current Mode VDD=2.7V, VEE=-9V, IREF=8uA, All one pattern, Display on, Segment pin under test is connected with a 20KΩ resistive load to VEE.	Contrast = FF	350	400	450	uA
		Contrast = AF	220	270	320	
		Contrast = 5F	110	145	180	
		Contrast = 0F	0	25	50	
	Half Range Current Mode VDD=2.7V, VEE=-9V, IREF=8uA, All one pattern, Display on, Segment pin under test is connected with a 20KΩ resistive load to VEE.	Contrast = FF	157.5	180	202.5	uA
		Contrast = AF	99	121.5	144	
		Contrast = 5F	49.5	65.25	81	
		Contrast = 0F	0	11.25	22.5	
Dev	Segment output current uniformity	Dev = (I_{SEG} − I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG}[0:131] = Segment current at contrast = FF	-	-	±9	%
		Contrast = 5F	-	-	±13	
R_{ON_C}	Common Output On Resistance	VDD - VEE=11.7V, Iout=30mA;	-	23	33	Ω

AC CHARACTERISTICS

Table 7 : AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.5V, T_A = 25°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display Timing Generator	Vdd = 2.7V, IREF = 8uA	35	40	42	kHz
F_{FRM}	Frame Frequency for 65 MUX Mode	132x64 Graphic Display Mode, Display ON, Internal Oscillator Enabled		$\dfrac{F_{osc}}{6x65}$		Hz
		132x64 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., F_{ext}, feeding to CL pin.		$\dfrac{F_{ext}}{6x65}$		Hz

Table 8 : 6800-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 8 : 6800-series MPU Parallel Interface Characteristics

Table 9 : 8080-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 9 : 8080-series MPU Parallel Interface Characteristics

Table 10 : Serial Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.5V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
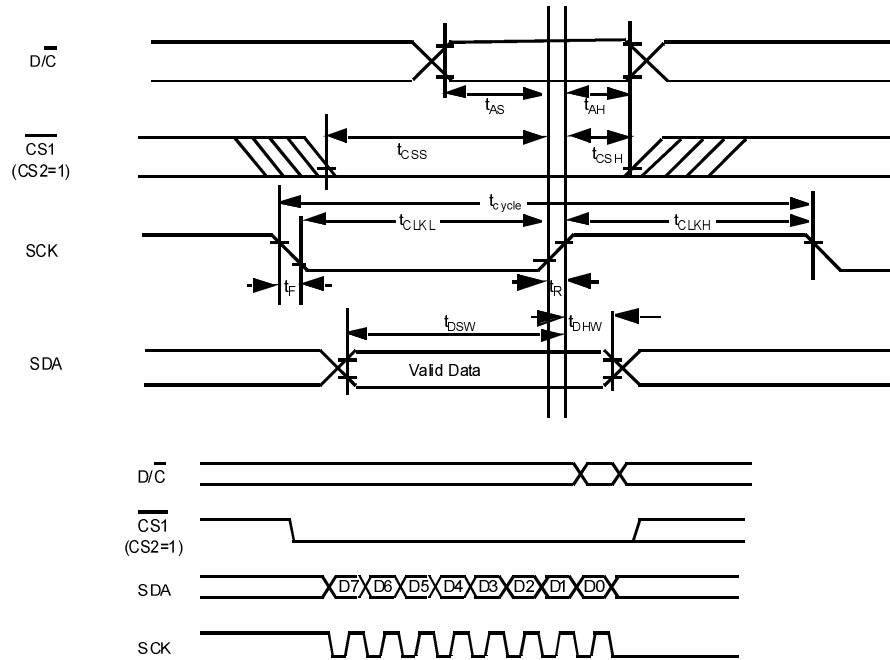
Figure 10 : Serial Interface Characteristics

* When SP# is high, please refer to APPENDIX I for timing characteristics for Solomon Systech Limited internal use only.

Application Example

The configuration for serial mode interface is shown in the following diagram:

DISPLAY PANEL SIZE
132X64+ICON LINE

COM0 ICONS SEG0 . . . . SEG131 COM1

COM44
COM46
.
COM60
COM62

SSD1301

COM47
COM49
.
COM63
ICONS

VEE IREF VREF VDD   VSS   CS1# D7 D6 D/C# RES# VEE

VDD   R1   C2   VDD   C3 VDD
C1

VEE   VREF VDD   VSS[GND]   CS1# SDA SCK D/C# RES# VEE
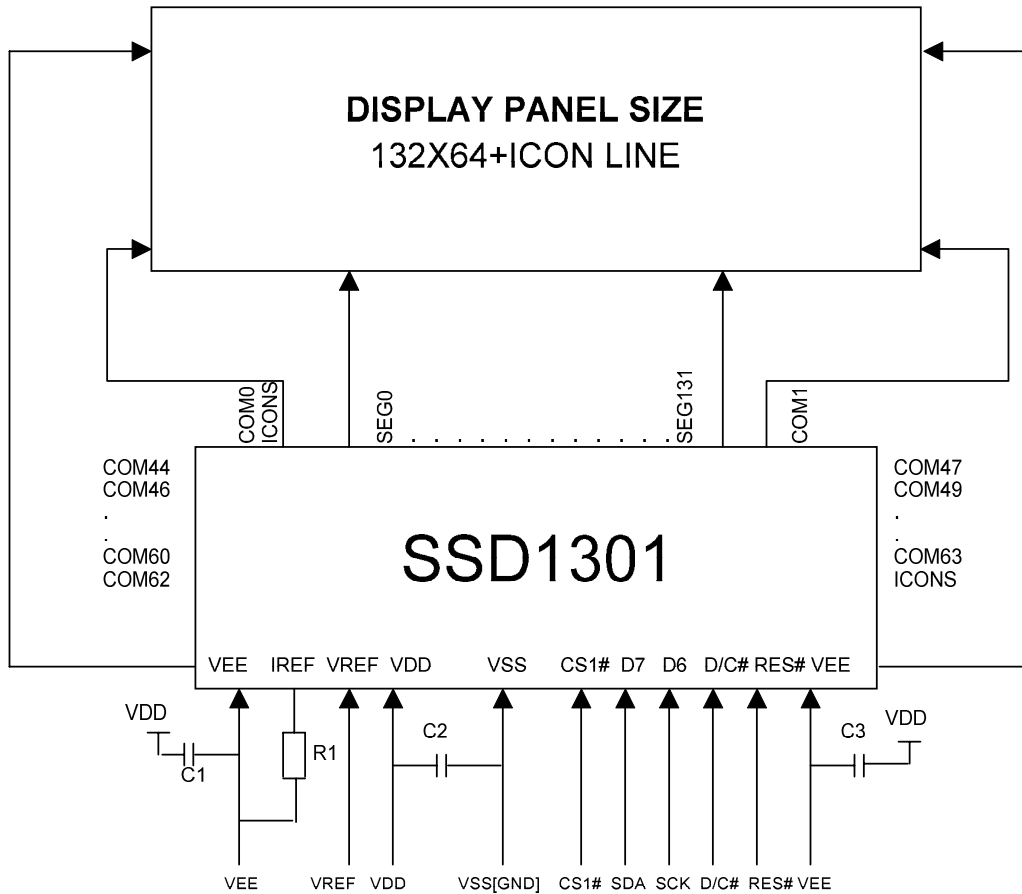
D0-D7: To MCU interface
VREF: External voltage reference for pre-charge signal (VEE<VREF<VDD)
IREF: Connect a 1% resistor to V_{EE} and keep the current across the resistor at 8.0uA
M/S#: Need to tie high for standalone system, refer to Pin Description
M, CL, DOF# –NC for standalone
CS2 – CS2 tied to high for serial bus
R/W#, E, D0 – D5 – NC for serial bus interface
CLS – pull high for internal oscillator

C1, C2, C3: 4.7uF
R1: Value=~1.2MΩ to set IREF to 8.0uA

	C68/80#	P/S#	SP#
6800 parallel interface	1	1	X
8080 parallel interface	0	1	X
Serial interface	X	0	0
I²C interface	*Refer to Appendix I		

Note: X stands for don't care.

SSD1301TR1 TAB PACKAGE DIMENSION
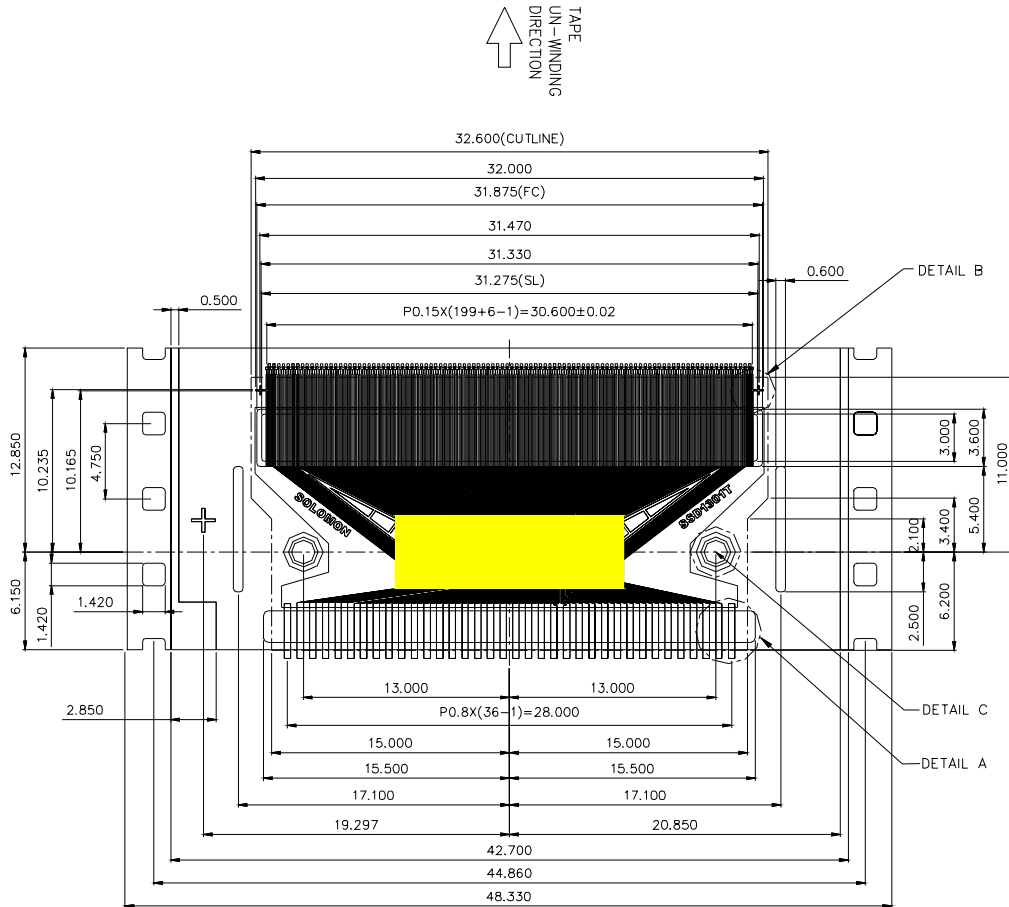
Note:

1. All dimensions are in mm unless specific

2. General Tolerance : +/-0.05mm

3. Cu Thickness : 25um

4. SN Plating : 0.35um

0.800

0.400

DETAIL A

2.000

0.663

0.070

0.075

0.150

0.070

0.600

DETAIL B

R0.740

R0.940

R1.240
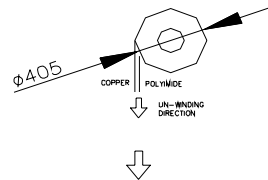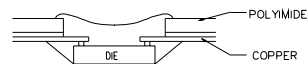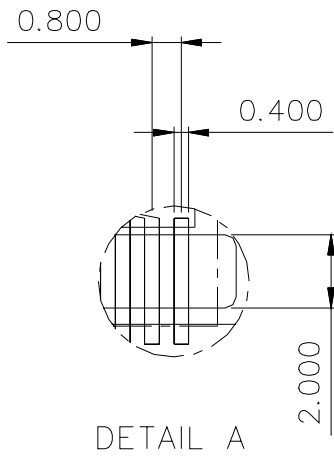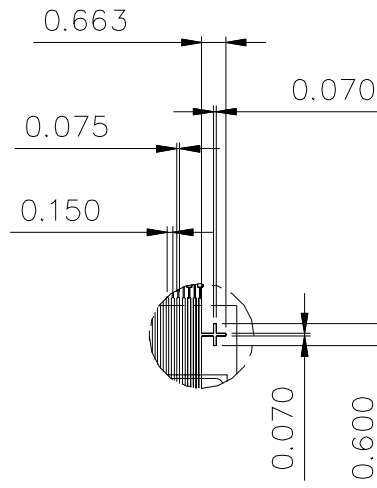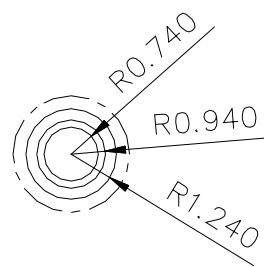
DETAIL C

APPENDIX I   IIC TIMING DIAGRAM AND PIN CONNECTION

PIN DESCRIPTION

SP#
This pin is serial interface selection input. When this pin and P/S# are pulled low, serial interface mode is selected. When it is pulled high and P/S# pin is pulled low, I^2C interface mode is selected.

FUNCTIONAL BLOCK DESCRIPTION

MPU I^2C Interface

The I^2C communication interface consists of slave address bit SA0 (D_5), I^2C-bus data signal SDA (D_0 for output and D_1 for input) and I^2C-bus clock signal SCL (D_4). Both the data and clock signals must be connected to pull-up resistors. There are also five input signals including, RES#, CS1#, P/S#, CS2, SP#, which is used for the initialization of device.

   a)   Slave address bit (SA0)
       SSD1301 have to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will responds to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

       b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
       0 1 1   1 1 0 SA0 R/W#

       "SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1301.
       "R/W#" bit determines the I^2C-bus interface is operating at either write mode or read status mode.

   b) I^2C-bus data signal (SDA)
       SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA. If SDA in is connected to the "SDA out", the device becomes fully IIC bus compatible.
       It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
       The "SDA out" pin may be disconnected from the "SDA in" pin. With such arrangement, the acknowledgement signal will be ignored in the I^2C-bus.

   c) I^2C-bus clock signal (SCL)
       The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

Command Decoder

Input is directed to the command decoder based on the input of control byte which consists of a D/C# bit and a R/W# bit. For further information about the control byte, please refer to the section "I^2C-bus Write data and read register status". If both the D/C# bit and the R/W# bit are low, the input signal is interpreted as a Command. It will be decoded and written to the corresponding command register. If the D/C# bit is high and the R/W# bit is low, input signal is written to Graphic Display Data RAM (GDDRAM).

I²C-bus Write data and read register status

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 11 for the write mode of I²C-bus in chronological order.
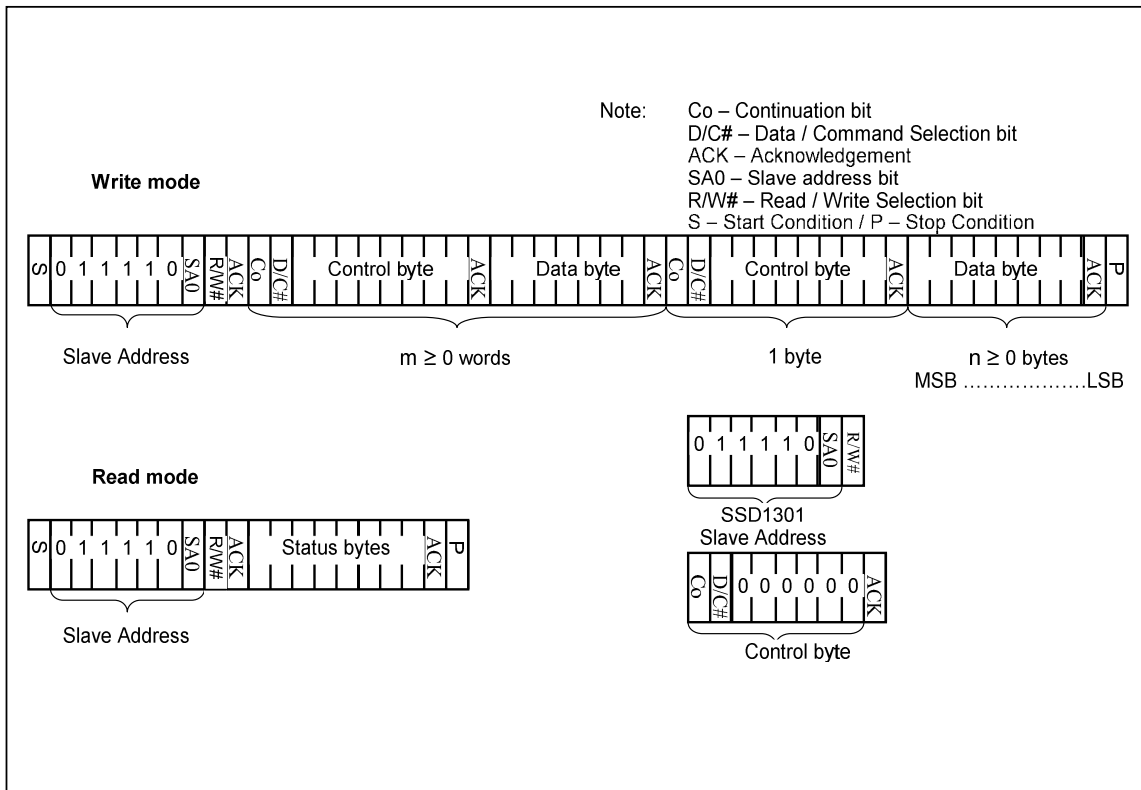

Figure 11 : I²C-bus data format

Write mode
1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 12. The start condition is established by pulling the SDA from high to low while the SCL stays high.
2) The slave address is following the start condition for recognition use. For the SSD1301, the slave address is either "b0111100" or "b0111101" by changing the SA0 to high or low.
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 13 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the high period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
   a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
   b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.

7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 12. The stop condition is established by pulling the "SDA in" from low to high while the "SCL" stays high.
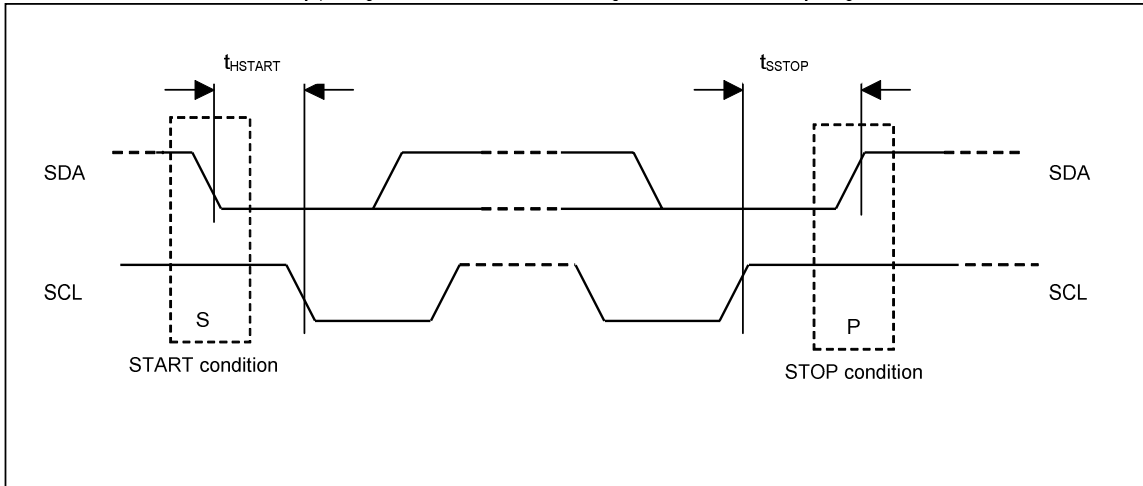

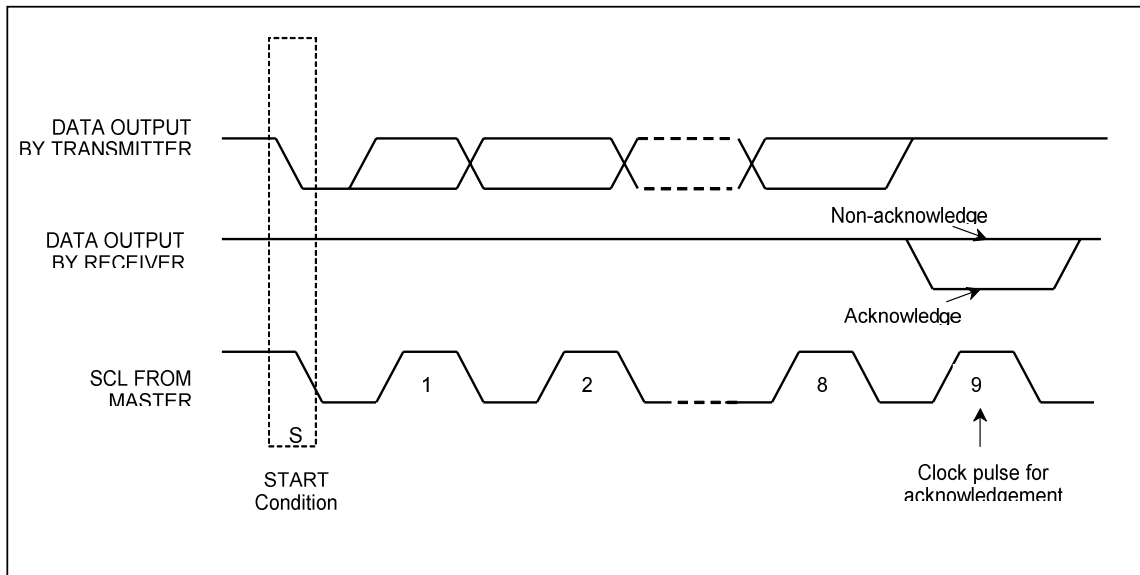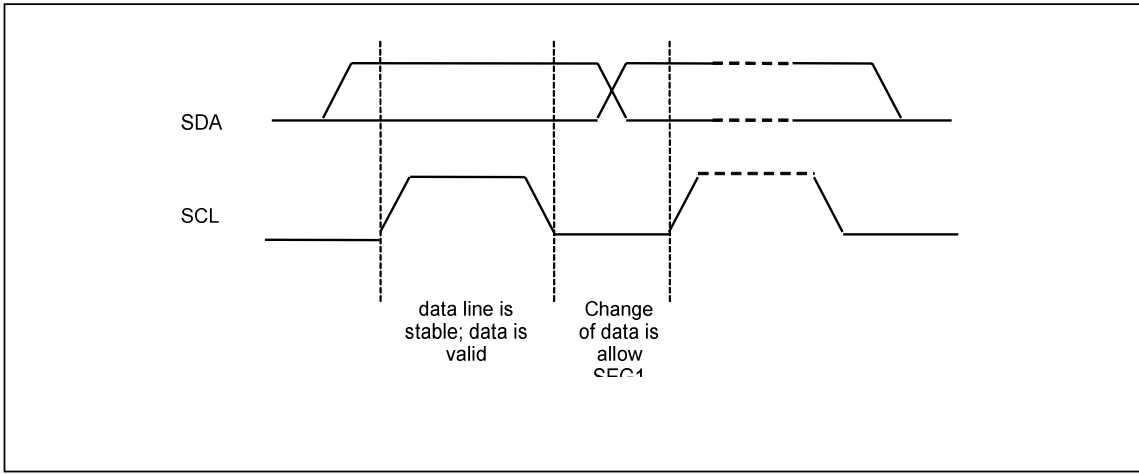**Figure 12 : Definition of the start and stop condition**

Figure 13 : Definition of the acknowledgement condition

Please be noted that the transmission of the data bit has some limitations.

      1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "high" period of the clock pulse. Please refer to the Figure 14 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is low.

      2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 14 : Definition of the data transfer condition

Read mode (Read status register)

1) The master device firstly initiates the data communication by a start condition. The definition of the start condition is shown in Figure 12.

2) The slave address is following the start condition for recognition use. For the SSD1301, the slave address is either "b0111100" or "b0111101".

3) The read mode is established by setting R/W# bit to logic "1". The read mode allows the MCU to monitor the internal status of the chip.

4) An acknowledgement signal will be generated after sending one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 13 for the graphical representation of the acknowledge signal.

5) The status of the register will be read at the next status byte. Please refer to the Read Command Table on page 15 for the explanation of the status byte.

6) The read mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 12.

Table 11 : I²C Interface Timing Characteristics (V$_{DD}$-V$_{SS}$=2.4 to 3.5V, T$_A$=-30 to 85° C)

Symbol	Parameter	Min	Typ	Max	Unit
t$_{cycle}$	Clock Cycle Time	2.5	-	-	us
t$_{HSTART}$	Start condition Hold Time	0.6	-	-	us
t$_{HD}$	Data Hold Time	300	-	-	ns
t$_{SD}$	Data Setup Time	100	-	-	ns
t$_{SSTART}$	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t$_{SSTOP}$	Stop condition Setup Time	0.6	-	-	us
t$_R$	Rise Time for data and clock pin	-	-	300	ns
t$_F$	Fall Time for data and clock pin	-	-	300	ns
t$_{IDLE}$	Idle Time before a new transmission can start	1.3	-	-	us
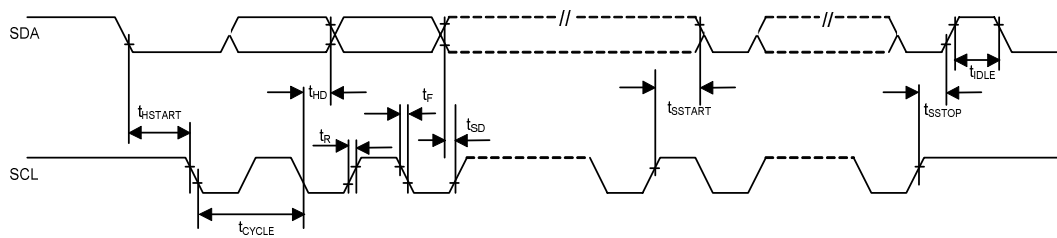
Figure 15 : I²C Interface Timing Characteristics