PhaseLink Corporation

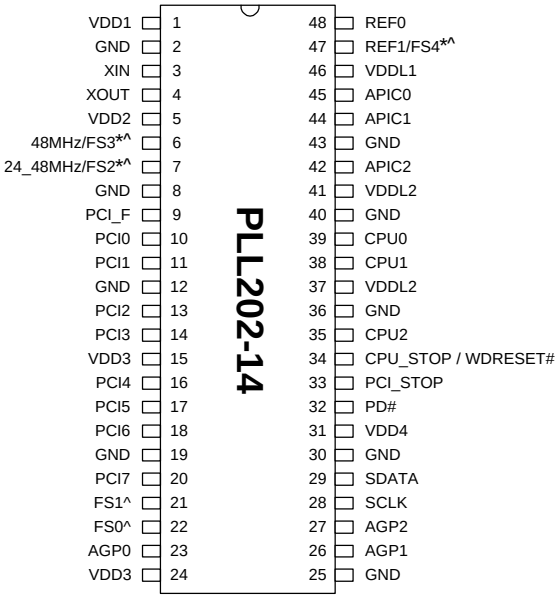
PLL202-14

Programmable Clock Generator for VIA Apollo Pro-266

FEATURES

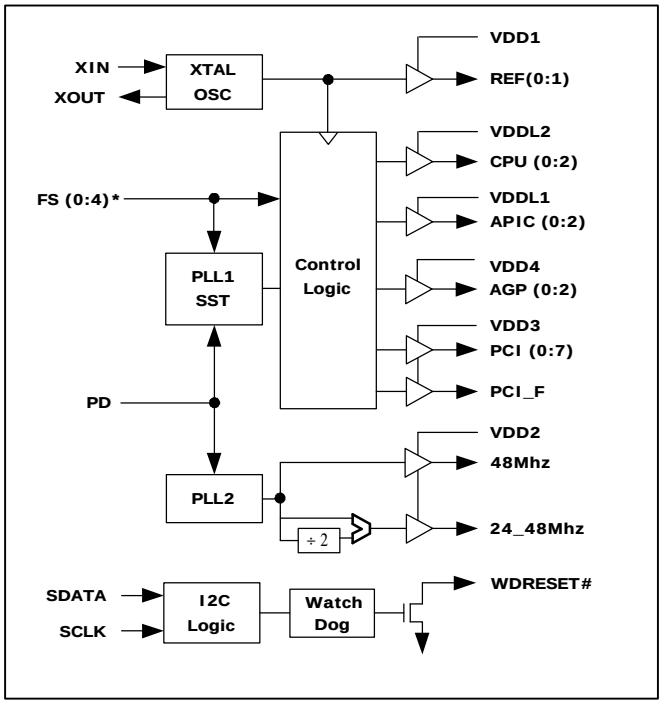
- Generates all clock frequencies for PentiumII/III system processor.
- Support 3 CPU clocks, 3 AGP and 9 PCI.
- Enhanced PCI Output Drive selectable by I2C.
- One 48MHz clock (or 24_48MHz clock via I2C).
- Three 2.5V APIC and two 14.318MHz ref. Clocks.
- Power management control to stop CPU, PCI, AGP, and APIC clocks.
- Supports 2-wire I2C serial bus interface with readback.
- Single byte micro-step linear Frequency Programming via I2C with glitch free smooth switching.
- Built-in programmable watchdog timer up to 63 seconds with 1-second interval. It will generate a low reset output when timer expired.
- Spread Spectrum ±0.25% center, ±0.5% center, ±0.75% center, and 0 to –0.5% downspread .
- 50% duty cycle with low jitter.
- Available in 300 mil 48 pin SSOP.

PIN CONFIGURATION



Note: ^: Pull up **#:** Active low
*: Bi-directional up latched at power-up

BLOCK DIAGRAM



POWER GROUP

- VDD1: REF(0:1), XIN, XOUT, PLL CORE
- VDD2: 48MHz or 24_48MHz
- VDD3: PCI(0:7), PCI_F
- VDD4: AGP(0:2)
- VDDL1: APIC(0:2)
- VDDL2: CPU(0:2)

KEY SPECIFICATIONS

- CPU Cycle to Cycle jitter: 250ps.
- PCI Cycle to Cycle jitter: 500ps.
- PCI to PCI skew: 500ps.
- CPU to CPU skew 175ps.
- CPU to PCI skew (CPU lead): typical 2ns.
- AGP to AGP skew: 250ps.

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PIN DESCRIPTIONS

Name	Number	Type	Description
VDD1	1	P	Power supply for REF(0:1), crystal oscillator and PLL core.
VDD2	5	P	Power supply for 48MHz or 24_48MHz.
VDD3	15,24	P	Power supply for PCI(0:7), PCI_F.
VDD4	31	P	Power supply for AGP(0:2).
VDDL1	46	P	Power supply for APIC(0:2) (2.5V).
VDDL2	37,41	P	Power supply for CPU(0:2) (2.5V).
GND	2,8,12,19,25,30, 36,40,43	P	Ground.
XIN	3	I	14.318MHz crystal input to be connected to one end of the crystal.
XOUT	4	O	14.318MHz crystal output.
PD#	32	I	PD is Asynchronous active low input used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped.
PCI_STOP	33	I	When input is LOW, PCI_STOP will stop PCI(0:7) except PCI_F.
CPU_STOP/ WDRESET#	34	B	When input is LOW, CPU_STOP will stop CPU(0:2). The enable of the watchdog timer masks the CPU_STOP action.
PCI_F, PCI(0:7)	9,10,11,13,14, 16,17,18,20	O	PCI clocks with frequencies defined by Frequency Table. These pins except PCI_F will be LOW when PCI_STOP is LOW.
CPU(0:2)	39,38,35	O	CPU clocks with frequencies defined by Frequency Table. These pins are LOW when CPU_STOP is LOW.
AGP(0:2)	23,26,27	O	AGP clocks outputs defined as 2x PCI.
SDATA	29	B	Serial data input for serial interface port.
SCLK	28	I	
REF1/FS4* 48MHz/FS3* 24_48MHz/FS2*	47,6,7	B	At power up, these pins are input pins and will determine the CPU clock frequency. After input sampling, these pins will generate output clocks. They all have internal pull up.
FS1,FS0	21,22	I	At power up, these pins will determine the CPU clock frequency.
APIC(0:2)	45,44,42	O	2.5V APIC clock output running synchronous with PCI/2 clock output. It is controlled by I2C byte 5 and byte 1.
REF0	48	O	3.3V 14.318MHz clock output.

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POWER MANAGEMENT

CPU_STOP	PCI_SOTP	CPU(0:1)	PCI	PCI_F	XTAL,VCO
1	1	Running	Running	Running	Running
0	1	Low	Running	Running	Running
1	0	Running	Low	Running	Running

FREQUENCY (MHz) SELECTION TABLE

FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	APIC	Spread Spectrum
0	0	0	0	0	200.0	100.0	50.0	25.0	± 0.25%
0	0	0	0	1	190.0	95.0	47.5	23.8	± 0.25%
0	0	0	1	0	180.0	90.0	45.0	22.5	± 0.25%
0	0	0	1	1	170.0	85.0	42.5	21.3	± 0.25%
0	0	1	0	0	166.0	83.4	41.5	20.8	± 0.25%
0	0	1	0	1	160.0	80.0	40.0	20.0	± 0.25%
0	0	1	1	0	150.0	75.0	37.5	18.7	± 0.25%
0	0	1	1	1	145.0	72.5	36.2	18.1	± 0.25%
0	1	0	0	0	140.0	70.0	35.0	17.5	± 0.25%
0	1	0	0	1	136.0	68.0	34.0	17.0	± 0.25%
0	1	0	1	0	130.0	65.0	32.5	16.2	± 0.25%
0	1	0	1	1	124.0	62.0	31.0	15.5	± 0.25%
0	1	1	0	0	66.8	66.8	33.4	16.7	± 0.75%
0	1	1	0	1	100.2	66.8	33.4	16.7	± 0.75%
0	1	1	1	0	118.0	78.6	39.3	19.6	± 0.25%
0	1	1	1	1	133.4	66.7	33.3	16.6	± 0.75%
1	0	0	0	0	66.8	66.8	33.4	16.7	± 0.25%
1	0	0	0	1	100.2	66.8	33.4	16.7	± 0.25%
1	0	0	1	0	115.0	76.6	38.3	19.1	± 0.25%
1	0	0	1	1	133.4	66.7	33.3	16.6	± 0.25%
1	0	1	0	0	66.8	66.8	33.4	16.7	± 0.5%
1	0	1	0	1	100.2	66.8	33.4	16.7	± 0.5%
1	0	1	1	0	110.0	73.3	36.6	18.3	± 0.25%
1	0	1	1	1	133.4	66.7	33.3	16.6	± 0.5%
1	1	0	0	0	105.0	70.0	35.0	17.5	± 0.25%
1	1	0	0	1	90.0	60.0	30.0	15.0	± 0.25%
1	1	0	1	0	85.0	56.6	28.3	14.1	± 0.25%
1	1	0	1	1	78.0	78.0	39.0	19.5	± 0.25%
1	1	1	0	0	66.6	66.6	33.3	16.6	0 to- 0.5%
1	1	1	0	1	100.0	66.6	33.3	16.6	0 to- 0.5%
1	1	1	1	0	75.0	75.0	37.5	18.7	± 0.25%
1	1	1	1	1	133.3	66.6	33.3	16.6	0 to- 0.5%

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FREQUENCY (MHz) SELECTION TABLE BY GROUP TIMING

Divider Ratio (CPU:AGP)	FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	APIC	Spread Spectrum
A (1 : 1)	1	1	1	0	0	66.6	66.6	33.3	16.6	0 to- 0.5%
	0	1	1	0	0	66.8	66.8	33.4	16.7	± 0.75%
	1	0	0	0	0	66.8	66.8	33.4	16.7	± 0.25%
	1	0	1	0	0	66.8	66.8	33.4	16.7	± 0.5%
	1	1	1	1	0	75.0	75.0	37.5	18.7	± 0.25%
	1	1	0	1	1	78.0	78.0	39.0	19.5	± 0.25%
B (1.5 : 1)	1	1	0	1	0	85.0	56.6	28.3	14.1	± 0.25%
	1	1	0	0	1	90.0	60.0	30.0	15.0	± 0.25%
	1	1	1	0	1	100.0	66.6	33.3	16.6	0 to- 0.5%
	0	1	1	0	1	100.2	66.8	33.4	16.7	± 0.75%
	1	0	0	0	1	100.2	66.8	33.4	16.7	± 0.25%
	1	0	1	0	1	100.2	66.8	33.4	16.7	± 0.5%
	1	1	0	0	0	105.0	70.0	35.0	17.5	± 0.25%
	1	0	1	1	0	110.0	73.3	36.6	18.3	± 0.25%
	1	0	0	1	0	115.0	76.6	38.3	19.1	± 0.25%
	0	1	1	1	0	118.0	78.6	39.3	19.6	± 0.25%
C (2 : 1)	0	1	0	1	1	124.0	62.0	31.0	15.5	± 0.25%
	0	1	0	1	0	130.0	65.0	32.5	16.2	± 0.25%
	1	1	1	1	1	133.3	66.6	33.3	16.6	0 to- 0.5%
	0	1	1	1	1	133.4	66.7	33.3	16.6	± 0.75%
	1	0	0	1	1	133.4	66.7	33.3	16.6	± 0.25%
	1	0	1	1	1	133.4	66.7	33.3	16.6	± 0.5%
	0	1	0	0	1	136.0	68.0	34.0	17.0	± 0.25%
	0	1	0	0	0	140.0	70.0	35.0	17.5	± 0.25%
	0	0	1	1	1	145.0	72.5	36.2	18.1	± 0.25%
	0	0	1	1	0	150.0	75.0	37.5	18.7	± 0.25%
D (2.5 : 1)	0	0	1	0	1	160.0	80.0	40.0	20.0	± 0.25%
	0	0	1	0	0	166.0	83.0	41.5	20.8	± 0.25%
	0	0	0	1	1	170.0	85.0	42.5	21.3	± 0.25%
	0	0	0	1	0	180.0	90.0	45.0	22.5	± 0.25%
	0	0	0	0	1	190.0	95.0	47.5	23.8	± 0.25%
	0	0	0	0	0	200.0	100.0	50.0	25.0	± 0.25%

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I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Serial Bits Reading	The serial bits will be read or sent by the clock driver in the following order Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in **Write Mode:** the **Command Byte** and **Byte Count Byte must be sent by the master** but ignored by the slave, in **Read Mode:** the **Byte Count Byte** will be **read by the master** then all other **Data Byte**.							

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	6	0	FS3 (see Frequency selection Table)
Bit 6	7	0	FS2 (see Frequency selection Table)
Bit 5	21	0	FS1 (see Frequency selection Table)
Bit 4	22	0	FS0 (see Frequency selection Table)
Bit 3	-	0	Frequency selection control bit 1=Via I2C, 0=Via External jumper
Bit 2	47	0	FS4 (see Frequency selection Table)
Bit 1	-	1	0 = OFF, 1 = Spread Spectrum Enable
Bit 0	-	0	0 = Normal, 1 = Tristate Mode for all outputs

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2. BYTE 1: CPU Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS2 value(Read) / WDT Fall-back Frequency selection for FS2
Bit 6	-	X	Inverted Power-up latched FS1 value(Read) / WDT Fall-back Frequency selection for FS1
Bit 5	-	1	1 = Normal, 0 = PCI Drive Enhanced 25%
Bit 4	-	X	Inverted Power-up latched FS0 value(Read) / WDT Fall-back Frequency selection for FS0
Bit 3	35	1	CPU2 (Active/Inactive)
Bit 2	38	1	CPU1 (Active/Inactive)
Bit 1	39	1	CPU0 (Active/Inactive)
Bit 0	42	1	APIC2 (Active/Inactive)

3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	20	1	PCI7 (Active/Inactive)
Bit 6	18	1	PCI6 (Active/Inactive)
Bit 5	17	1	PCI5 (Active/Inactive)
Bit 4	16	1	PCI4 (Active/Inactive)
Bit 3	14	1	PCI3 (Active/Inactive)
Bit 2	13	1	PCI2 (Active/Inactive)
Bit 1	11	1	PCI1 (Active/Inactive)
Bit 0	10	1	PCI0 (Active/Inactive)

4. BYTE 3: AGP Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS3 value(Read) / WDT Fall-back Frequency selection for FS3
Bit 6	-	0	0=24MHz, 1=48MHz
Bit 5	6	1	48MHz (Active/Inactive)
Bit 4	7	1	24_48MHz (Active/Inactive)
Bit 3	9	1	PCI_F (Active/Inactive)
Bit 2	27	1	AGP2 (Active/Inactive)
Bit 1	26	1	AGP1 (Active/Inactive)
Bit 0	23	1	AGP0 (Active/Inactive)

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5. BYTE 4: Linear Programming Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Linear programming sign bit (0 is "+", 1 is "–")
Bit 6	-	0	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0	Linear programming magnitude bit 5
Bit 4	-	0	Linear programming magnitude bit 4
Bit 3	-	0	Linear programming magnitude bit 3
Bit 2	-	0	Linear programming magnitude bit 2
Bit 1	-	0	Linear programming magnitude bit 1
Bit 0	-	0	Linear programming magnitude bit 0 (LSB)

6. BYTE 5: Peripheral Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS4 value(Read) / WDT Fall-back Frequency selection for FS4
Bit 6	-	1	Reserved (Active/Inactive)
Bit 5	44	1	APIC1 (Active/Inactive)
Bit 4	45	1	APIC0 (Active/Inactive)
Bit 3	-	1	Reserved (Active/Inactive)
Bit 2	-	1	Reserved (Active/Inactive)
Bit 1	47	1	REF1 (Active/Inactive)
Bit 0	48	1	REF0 (Active/Inactive)

7. BYTE 6: Reserved Register (For PLL103-02 DDR)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

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8. BYTE 7: Reserved Register (For PLL103-02 DDR)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

9. BYTE 8: Watchdog Timer / Revision ID and Vendor ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description	
Bit 7	-	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable	
Bit 6	-	0	Revision ID Bit 2*	
Bit 5	-	0	Watchdog Time Interval Bit 5 (MSB)	Revision ID Bit 1*
Bit 4	-	0	Watchdog Time Interval Bit 4	Revision ID Bit 0*
Bit 3	-	0	Watchdog Time Interval Bit 3	Vendor ID Bit 3*
Bit 2	-	0	Watchdog Time Interval Bit 2	Vendor ID Bit 2*
Bit 1	-	1	Watchdog Time Interval Bit 1	Vendor ID Bit 1*
Bit 0	-	1	Watchdog Time Interval Bit 0 (LSB)	Vendor ID Bit 0*

Note: ***:** Default value at power-up. Don't write into this register, writing into this register can cause malfunction.

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PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL202-14 device incorporates SMART-BYTE ™ technology with a single byte programming via I2C to better optimize clock jitter and spread spectrum performance. Detail of PLL202-14's dual mode frequency programming method is described below:

1. ROM-table Frequency Programming:

The pre-defined 32 frequencies found in Frequency table can be accessed either through 5 external jumpers or by setting internal I2C register in BYTE0.

2. Fine-step Linear Frequency Programming:

CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around current selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency change. The formula is as follow:

$$F_{CPU} = F_{CPU\text{-}ROM\text{-}table} \pm \alpha\ (=0.22,\ 0.15 \text{ or } 0.11) * M$$

Where:
1. M is magnitude factor defined in I2C Byte4.bit (0:6)
2. ± (sign bit) of M is defined in I2C Byte4.bit 7
3. α is a constant but related to CPU's three Timing groups definition
   α = 0.11 (for Group A), α = 0.15 (for Group B, C) or α = 0.22 (for Group D)

FREQUENCY PROGRAMMING EXAMPLE:

1. Procedures to program target CPU frequency to 122.0 Mhz in Group B timing:

A. Locate the closest CPU frequency from Frequency from Frequency-ROM table: 118.0
B. α = 0.15 for Group B
C. Solve M (Linear Magnitude factor) in integer:

$$M = (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha$$
$$= (122 - 118) / 0.15$$
$$= 27$$

D. Program I2C register:

7	6	5	4	3	2	1	0
1	1	1	0	1	0	0	0
FS3	FS2	FS1	FS0	CTR	FS4		

Setting of I2C.BYTE0

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	1
Sign	M6	M5	M4	M3	M2	M1	M0

Setting of M = +27 in I2C.BYTE4

F_{CPU} = 118.0 + (0.15) * 27 = 122.05 (% of frequency increased = 0.04%)
F_{AGP} = 78.6 * (1 + 0.04%) = 78.63
F_{PCI} = 39.3 * (1 + 0.04%) = 39.32

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BUILT-IN WATCHDOG TIMER (WDT)

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into "Hang-up" state within a reasonable period of time (or Watchdog time interval). The watchdog time interval can be programmed between 0 and 63 seconds with increment of 1 second by setting the value of I2C.Byte8.Bit(5:0). Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL202-14 will start from predefined Fall-back Frequency (the value of I2C Byte1.Bit(4,6,7), Byte3.Bit7, Byte5.Bit7). If system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

Example usage:

1. System power-up at CPU= 66.8MHz (Group A) where external jumpers are used.

2A. Switch to target CPU=100.2MHz frequency (Group B) with following I2C register setting:

7	6	5	4	3	2	1	0	
1	1	0	1	**1**	0	0	0	FSEL Setting in I2C.BYTE0
FS3	FS2	FS1	FS0	CTR	FS4			

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	M =0 Setting in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0	

7	6	5	4	3	2	1	0	
1	0	0	0	1	1	1	1	WD-Timer = 15s Setting in I2C.BYTE8
ENB		T5	T4	T3	T2	T1	T0	

7	6	5	4	3	2	1	0	
0	0	0	0	1	1	0	1	FBSEL Setting in I2C.BYTE1, 3, 5
			FB4	FB3	FB2	FB1	FB0	

The fall-back frequency is set to the same location as that of FSEL since frequency switching between different timing groups will cause system to hang up. After WD timer expired or 15 seconds, the system will restart properly at target 100.2MHz if CPU is capable; otherwise WDT will perform another reset action to restart the system from 66.8 MHz

2B. Switch to target CPU=79MHz within the same timing Group

The fall-back frequency is recommended to set at the most safe and comfortable level to ensure a successful reboot such as 75.0 if system is unable to switch to 79Mhz.

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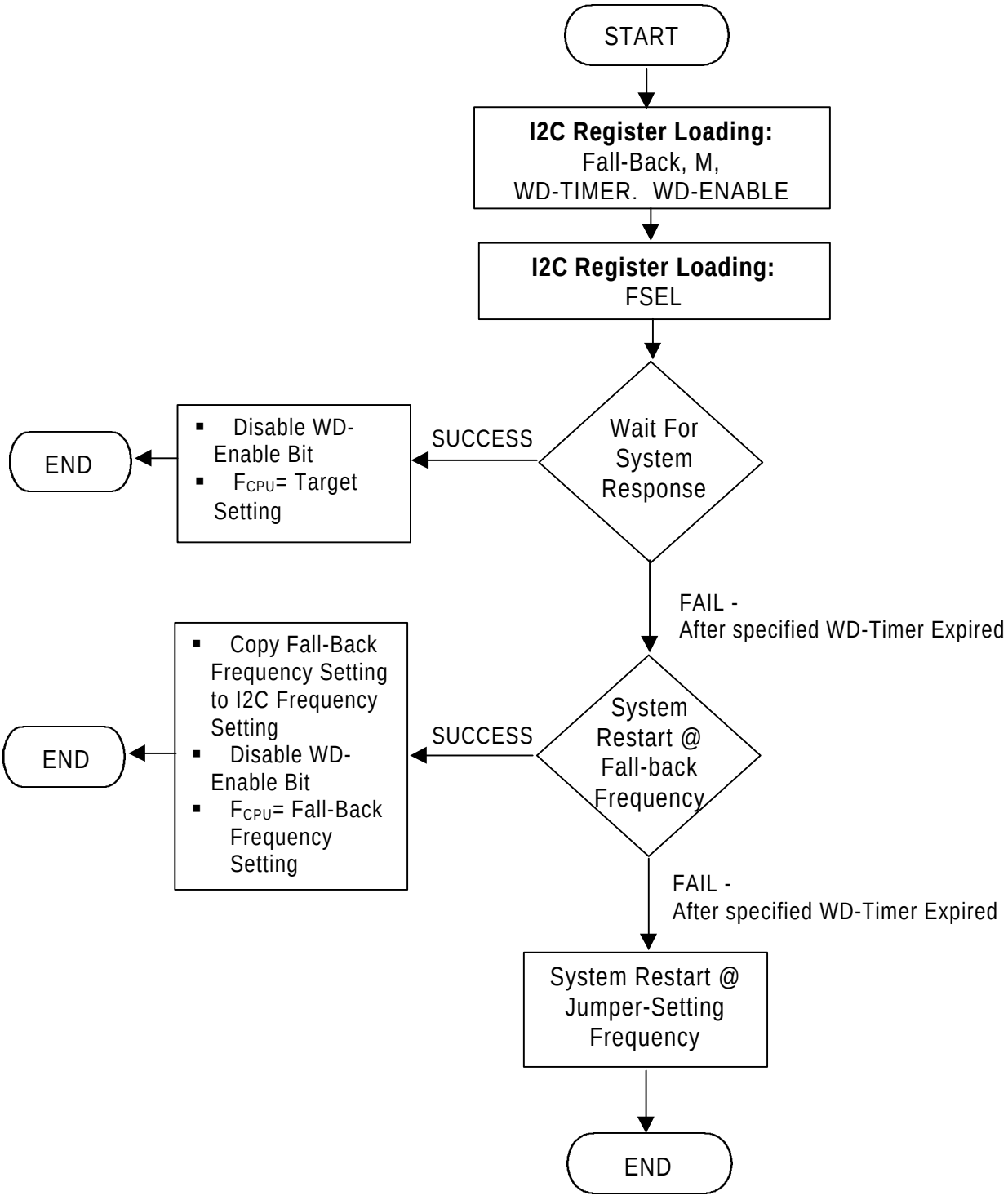
WDT OPERATIONAL FLOW CHART



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ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC/AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	uA
Input Low Current	I_{IL1}	V_{IN}=0 with no pull-up resistor	-5			uA
Input Low Current	I_{IL2}	V_{IN}=0 with pull-up resistor	-200			
Supply Current	I_{DD}	C_L=0 pF@66MHz, 3.3V±5%			180	mA
	I_{DDL}	C_L=0 pF@133MHz, 3.3V±5%				
	I_{DD}	C_L=0 pF@66MHz, 2.5V±5%			72	
	I_{DDL}	C_L=0 pF@133MHz, 2.5V±5%			100	
Transition Time	T_{trans}	To 1st crossing of target Freq.			3	ms
Pull-up resistor	R_{Pu}	Pin 6,7,21,22,47		120		kohm
Input frequency	F_I	V_{DD} = 3.3V	12	14.318	16	MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	XIN & XOUT pins	27	28	45	pF

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2. DC/AC Electrical Specifications (continued)

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU	Measured @ 0.4V ~ 2.0V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 0.4V ~ 2.4V, C_L=10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 0.4V ~ 2.4V, C_L=10-30pf			2	
Output Fall time	T_{OF}	CPU	Measured @ 2.0 ~ 0.4V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 2.4V ~ 0.4V, C_L=10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 2.4V ~ 0.4V, C_L=10-30pf			2	
Duty Cycle	D_T	CPU,APIC,REF, 48MHz,24MHz	Measured @ 1.5V C_L=20pf	45	50	55	%
		PCI, AGP	Measured @ 1.5V, C_L=20~30pf	40		55	
Clock Skew	T_{SKEW}	CPU	Rising edge @ 1.25V, C_L=20pf			175	ps
		PCI	Rising edge @ 1.5V, C_L=30pf			500	
		AGP	Rising edge @ 1.5V, C_L=30pf			250	
Jitter(Cycle to Cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		PCI, AGP	Measured @ 1.5V			500	
Frequency Stabilization Time	T_{FST}	CPU,PCI_F,PCI, APIC,AGP,REF, 48MHz,24MHz	Assumes full supply voltage reached within 1ms from power-up. Short cycle exist prior to frequency stabilization.			3	ms
AC output impedance	Z_0	CPU	V_{DD}=3.3V(2.5V)±5%		20		ohm
		PCI,AGP	V_{DD}=3.3V±5%		30		
		REF,48MHz,24MHz	V_{DD}=3.3V±5%		40		

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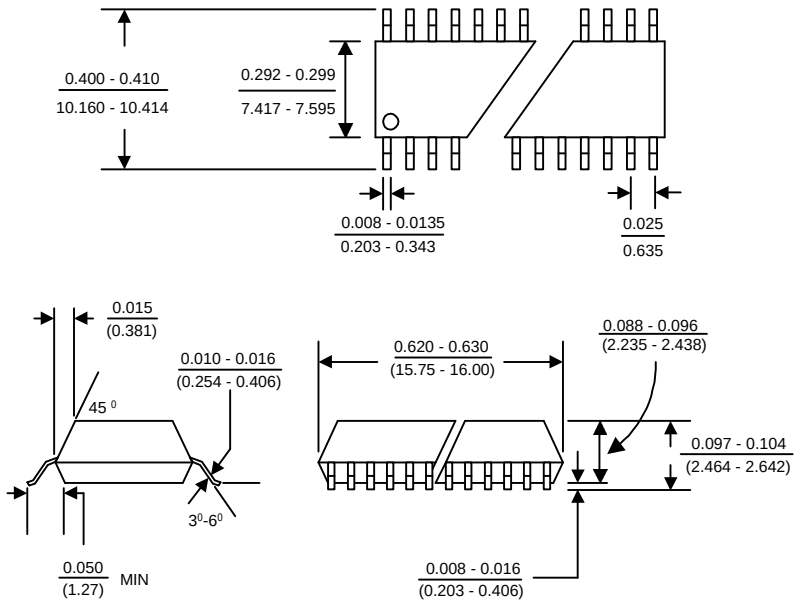
PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL202-14 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP

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