PL-2528 (Chip Rev 3A)
Advanced Hi-Speed USB Flash Disk Controller
Product Datasheet

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Prolific Technology Inc.

7F, No. 48, Sec. 3, Nan Kang Rd.
Nan Kang, Taipei 115, Taiwan, R.O.C.
Tel: 886-2-2654-6363
Fax: 886-2-2654-6161
Email: sales@prolific.com.tw
URL: http://www.prolific.com.tw

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1.0 Overview

PL-2528 is an advanced Hi-Speed USB Flash Disk controller that allows data transfer between USB-equipped hosts (such as PC, PDA, MP3 Player) and NAND Flash Memory through USB port interface at transfer rate of 480Mbps. Advanced mode design allows for PL-2528 USB Flash devices to reach enhanced R/W performances of 34MByte/sec and 24MByte/sec respectively. It also allows interface of up to 8 NAND Flash Memory. The PL-2528 is the best solution for low power, high performance and compatibility, plug-and-play portable storage media.

The available NAND flash memories on board can generally be used as a normal single disk or partitioned into a standard/open mass storage device and a secured mass storage device. The sizes of the partitions can be easily configured and adjusted by end-users using the USB Flash Disk (UFD) utility program. To access the secured mass storage device or disk, users must first enter the correct password using the UFD utility program.

Two new features of the PL-2528 is the Read-Only and Hidden Partition (Optional). The PL-2528 allows vendors to create a read-only partition for preloading their software driver and application program to save on driver CD cost and enhance user-friendliness. If a secured partition and password is set, this Read-Only partition will toggle with the Secured partition disk after the password is confirmed. When you plug-in the device, the Read-Only partition and the open partition will first appear and after the end-user enters the password, the Read-Only partition will be removed and the Secured partition will appear (refer to the partition configuration table on the succeeding page). The Hidden partition allows vendors to put their own private application programs and using a special utility to access it. This Hidden partition is not accessible and cannot be seen by end-users. Prolific provides a vendor manufacturing kit utility to customize and preset these special partitions.

To take advantage of Plug and Play, the mass storage device is implemented according to the USB mass storage device class. Since the default driver is included within most of the current OS, no extra driver is needed for Linux, Mac OS, Windows Vista, Windows® ME/2000/XP/2003 Server and above. Prolific provides a separate Windows 98 driver and supports driver and utility customization. PL-2528 also supports Vista ReadyBoost requirements for both SLC and MLC NAND flash configurations.

The PL-2528 also provides options to customize this chip in showing the vendor identity. Users could modify the Vendor ID, Product ID, Language ID, manufacturer string, and product string of the final product. Production configuration and test tool utilities are also provided by Prolific.

2.0 Features

- **USB Interface**
  - Supports standard USB (Universal Serial Bus) interface
  - Fully USB 2.0 bus powered compliant
  - Fully compatible with USB 1.1 and 2.0
  - Hi-Speed USB-IF Logo Compliant with TID 40000222
  - Integrated USB 2.0 Transceiver Macrocell Interface and Serial Interface Engine
  - Supports Hi-Speed (480 Mbps), Full Speed (12 Mbps), Low Speed (1.5 Mbps) transfer
  - 4 End points support Control, Interrupt, Bulk-In, and Bulk-Out
  - Dual 512-Byte FIFO for Bulk In and Bulk Out Data Transfer
  - USB power saving support
  - Built-in USB mass storage driver support in Windows® Vista, XP, 2003 Server, 2000, and ME (Prolific provides Windows 98 driver support), Linux Kernel 2.4.18 and above, MAC OS 9.x and above (Apple provides Mac OS 8.6 driver support).
  - Windows Vista Logo and ReadyBoost Compliant

- **Error Correction Logic**
  - Error Correction of 4 bits random error per 512 Bytes of data
  - Automatic on-the-fly, in-buffer error correction

- **Flash Memory Control**
  - Flash Sequencer Logic to support all the control signals to execute read/write/erase operation automatically
  - Flash Write Protect control support
  - Supports Samsung/Toshiba/Hynix/ST/Infineon/Micron SLC NAND type flash memories
  - Supports Samsung/Hynix/Sandisk/Toshiba MLC flash memories
  - 8/16-bit Flash Data I/O
  - Dual-channel mode support for SLC and MLC NAND flash memories
  - Universal flash memory support
  - In-System Programming to upgrade firmware easily
  - Supports up to 8 NAND flash memories
  - Non-Stop Writing® (NSW) Technology (Gain 20% Write Performance)
  - Wear-Leveling algorithm to prolong the life and write endurance of NAND Flash

- **Miscellaneous:**
  - No extra Regulator needed
  - 3.3V Single Power Required
  - 12MHz external clock
  - Integrated RISC micro-controller
  - Small form factor- 0.18um process LQFP64 (7 x 7 mm) and TQFP (7 x7 mm) package
  - Configurable Vendor ID/Product ID
  - LED indicator to show access status
  - Software support includes Disk partitions and password check for security disk, PC boot-up as USB Zip Disk and USB Hard Disk, and CD-ROM type emulation.

3.0 Functional Block Diagram

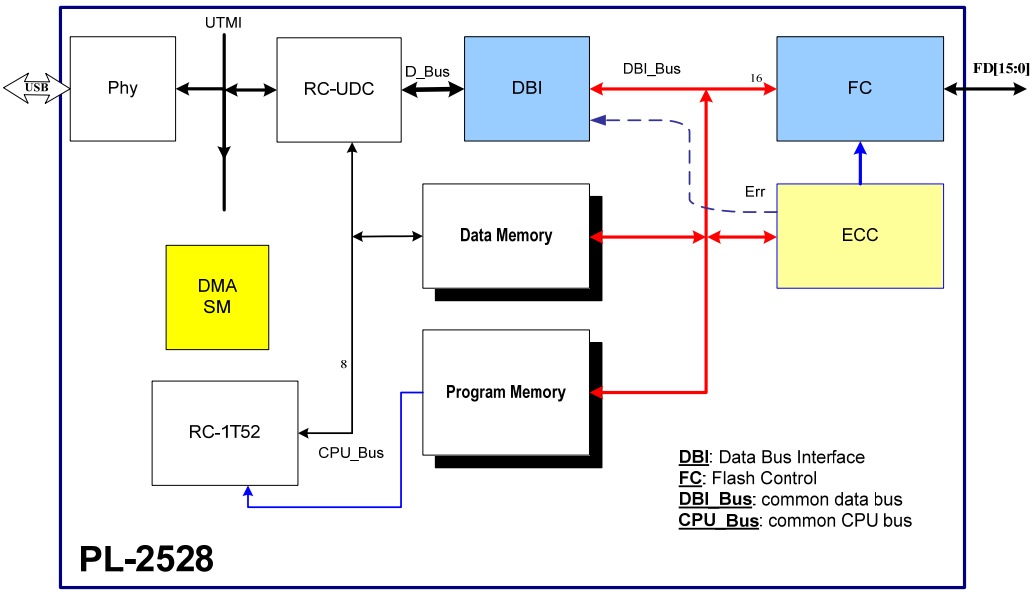


Figure 3-1 Block Diagram of PL-2528

4.0 Pin Assignment and Description

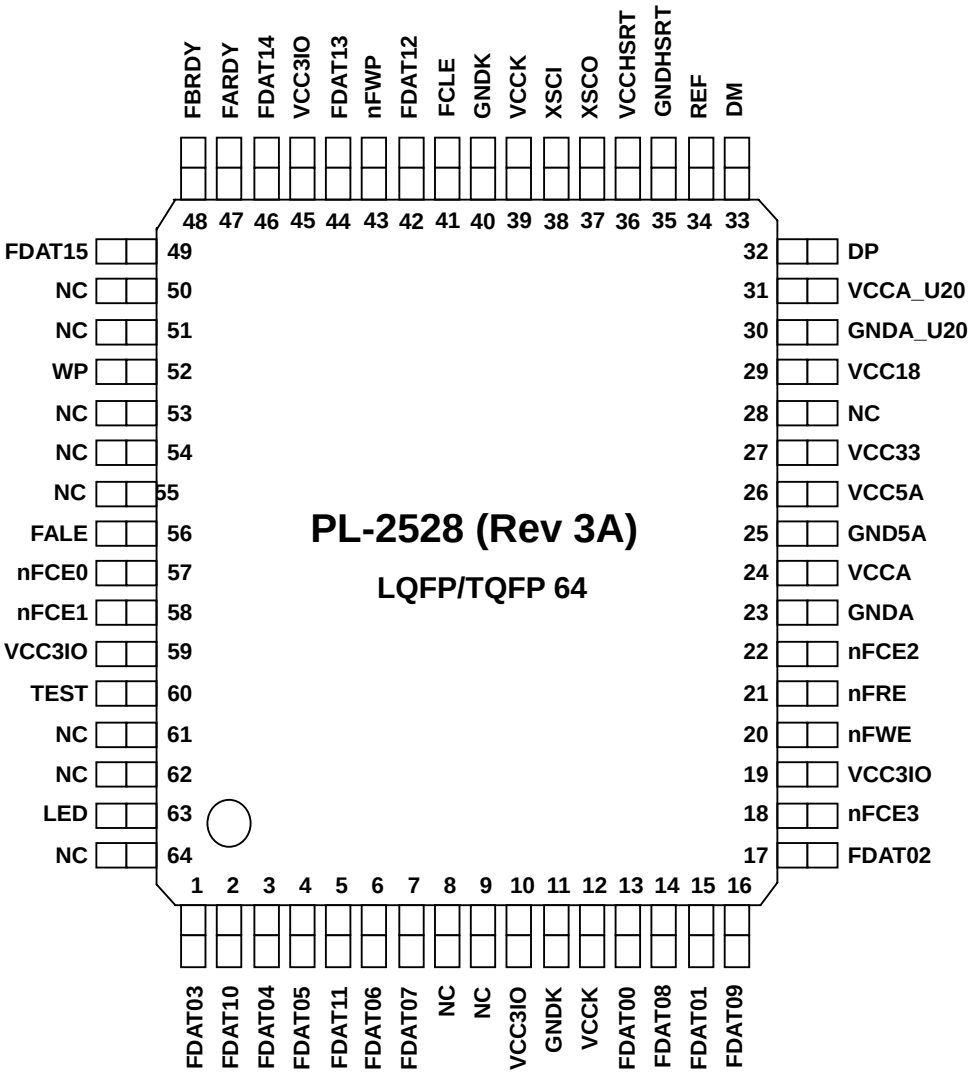


Figure 4-1 Pin Assignment of PL-2528 (Rev 3A) LQFP/TQFP64

Table 4-1 Pin Descriptions of PL-2528 (Rev 3A) 64-Pin

Pin No.	Pin Name	Pin Description	Notes
1	FDAT03	Flash Data Bus 3	
2	FDAT10	Flash Data Bus 10	
3	FDAT04	Flash Data Bus 4	
4	FDAT05	Flash Data Bus 5	
5	FDAT11	Flash Data Bus 11	
6	FDAT06	Flash Data Bus 6	
7	FDAT07	Flash Data Bus 7	
8	NC	No Connection	
9	NC	No Connection	
10	VCC3IO	VCC I/O	
11	GNDK	Ground	
12	VCCK	VCC	1.8V only
13	FDAT00	Flash Data Bus 0	
14	FDAT08	Flash Data Bus 8	
15	FDAT01	Flash Data Bus 1	
16	FDAT09	Flash Data Bus 9	
17	FDAT02	Flash Data Bus 2	
18	nFCE3	Flash Chip Select 3	
19	VCC3IO	VCC I/O	
20	nFWE	Flash Write Enable	
21	nFRE	Flash Read Enable	
22	nFCE2	Flash Chip Select 2	
23	GNDA	Analog Ground	
24	VCCA	Analog Power Supply	
25	GND5A	Ground	
26	VCC5A	Regulator 5V input	
27	VCC33	Regulator 3.3V output	
28	NC	No Connection	
29	VCC18	Regulator 1.8V output	
30	GNDA_U20	Analog Ground	
31	VCCA_U20	Analog Power Supply	3.3V
32	DP	USB Data Positive Pin	
33	DM	USB Data Negative Pin	
34	REF	Connect External Reference Register to Analog Ground	12KΩ +/- 1%
35	GNDHSRT	Analog Ground	
36	VCCHSRT	Analog Power Supply	3.3V
37	XSCO	Crystal Oscillator Output	12MHz
38	XSCI	Crystal Oscillator input	12MHz
39	VCCK	VCC	1.8V only
40	GNDK	Ground	
41	FCLE	Flash Command Latch Enable	
42	FDAT12	Flash Data Bus 12	

Table 4-1 Pin Descriptions of PL-2528 64-Pin (cont…)

Pin No.	Pin Name	Pin Description	Notes
43	nFWP	Flash Write Protect	
44	FDAT13	Flash Data Bus 13	
45	VCC3IO	VCC I/O	
46	FDAT14	Flash Data Bus 14	
47	FARDY	Flash A Busy/Ready	
48	FBRDY	Flash B Busy/Ready	
49	FDAT15	Flash Data Bus 15	
50	NC	No Connection	
51	NC	No Connection	
52	WP	GPIO1	For Write Protect
53	NC	No Connection	
54	NC	No Connection	
55	NC	No Connection	
56	FALE	Flash Address Latch Enable	
57	nFCE0	Flash Chip Select 0	
58	nFCE1	Flash Chip Select 1	
59	VCC3IO	VCC I/O	
60	TEST	Test Mode Enable	
61	NC	No Connection	
62	NC	No Connection	
63	LED	GPIO0	For LED Indicator
64	NC	No Connection	

5.0 DC Characteristics

5.1 Recommended Operation Conditions

Table 5-1 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCCK	Core Power Supply	1.65	1.8	1.95	V
VCC3IO	Power Supply	3.0	3.3	3.6	V
T_j	Commercial Junction operation Temperature	-40	25	125	^oC

5.2 General DC Characteristics

Table 5-2 General DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{in}	Input leakage current	Vin= VCC3V or 0	-10	± 1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
V_{IL}	Input low voltage	LVTTL			0.8	V
V_{IH}	Input high voltage	LVTTL	2.0			V
V_{OL}	Output low voltage	Iol=2~16mA			0.4	V
V_{OH}	Output high voltage	Iol=2~16mA	2.4			V
R_I	Input pull up/down resistance	Vin=VCC3V(up) Vin=0(down)	40	75	190	kΩ

Note: Multi-voltage I/O buffers operating under 3.3V

6.0 AC Characteristics

6.1 Flash Read/Write Timing

6.1.1 Tc = 36 ns

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		36		ns
$Ts_{(FW)}$	FD set up time of FWE#	15			ns
$Th_{(FW)}$	FD hold time of FWE#	10			ns
$Ts_{(FR)}$	FD set up time of FRD#	5			ns
$Th_{(FR)}$	FD hold time of FRD#	-			ns

6.1.2 Tc = 54 ns

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		54		ns
$Ts_{(FW)}$	FD set up time of FWE#	20			ns
$Th_{(FW)}$	FD hold time of FWE#	20			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

6.1.3 Tc = 72 ns

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		72		ns
$Ts_{(FW)}$	FD set up time of FWE#	35			ns
$Th_{(FW)}$	FD hold time of FWE#	30			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

6.1.4 Tc = 108 ns

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		108		ns
$Ts_{(FW)}$	FD set up time of FWE#	60			ns
$Th_{(FW)}$	FD hold time of FWE#	40			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

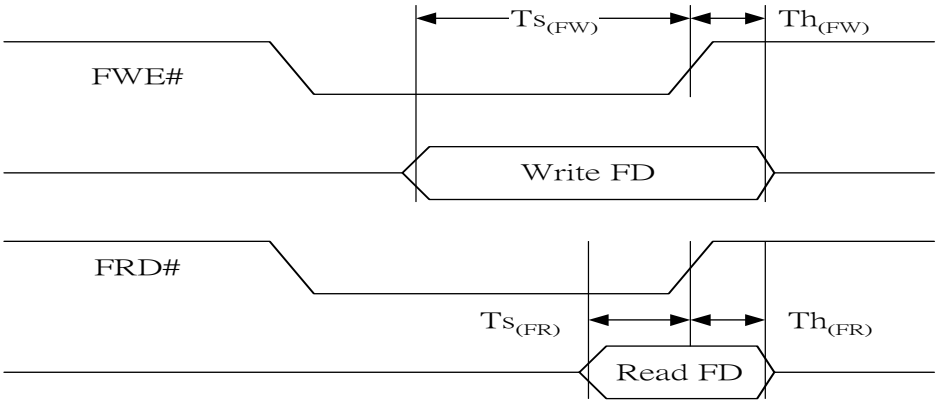


Figure 6-1 Flash Read/Write Timing Diagram

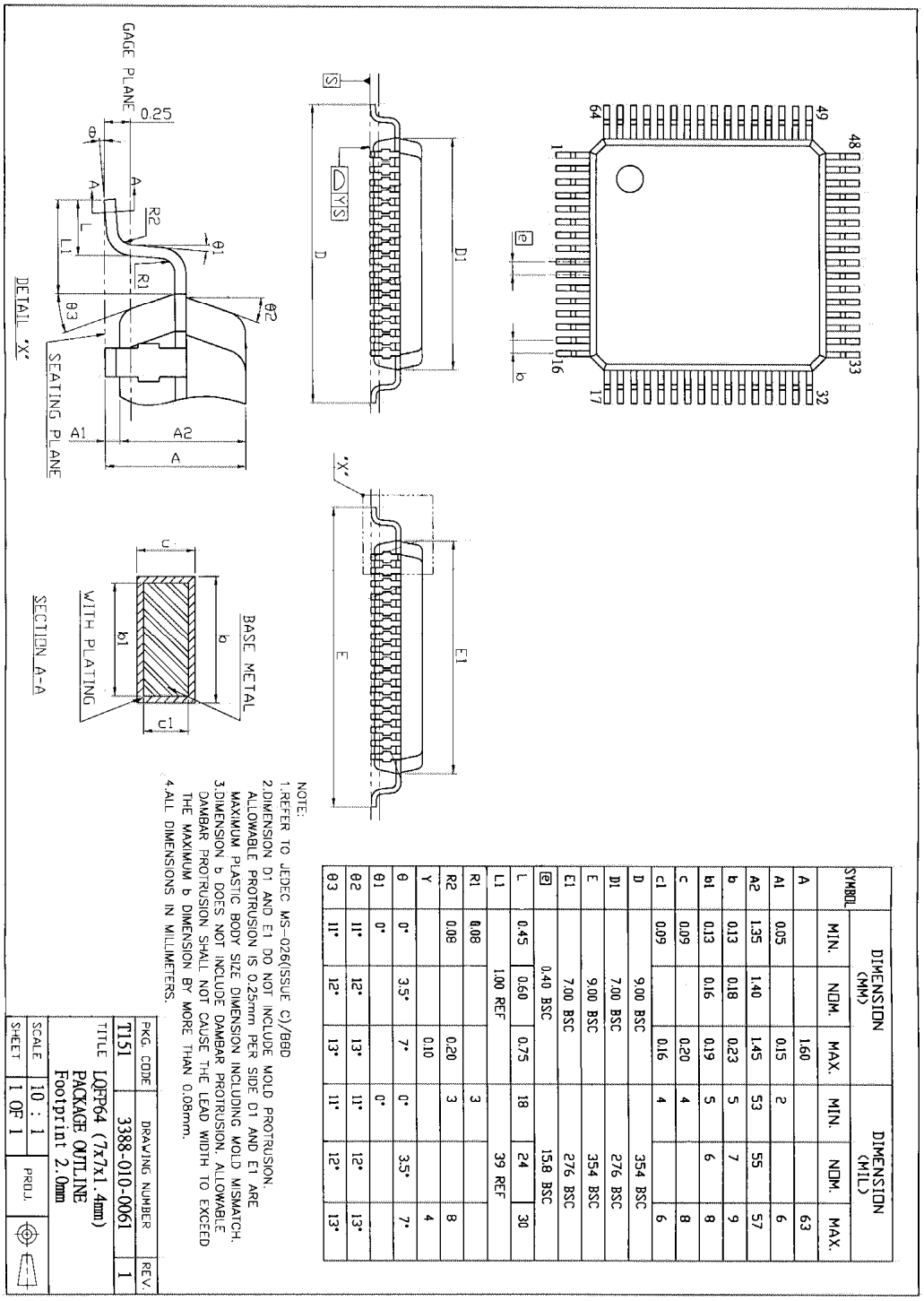
7.0 Ordering Information

Table 7-1 Ordering Information

Part Number	Package Type
PL-2528 LQFP	64-pin LQFP (7x7mm) Lead-Free or Pb-Free
PL-2528 TQFP	64-pin TQFP (7x7mm) Lead-Free or Pb-Free

8.0 Outline Diagram

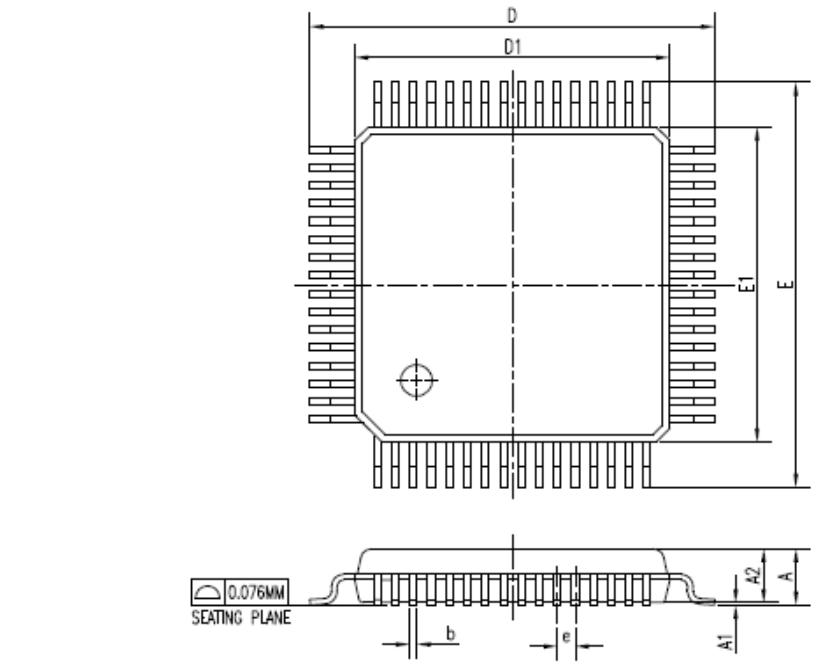
8.1 PL-2528 LQFP64pin (7mm x 7mm) Outline Diagram

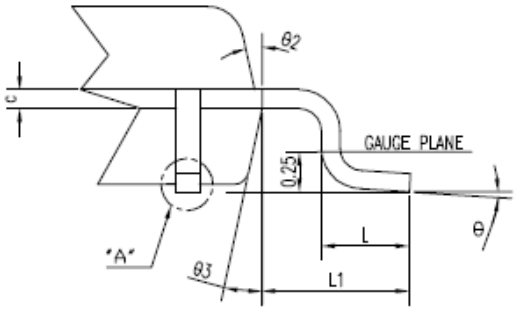


SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
e		0.40 BSC			15.8 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

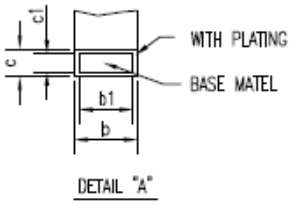
Figure 8-1 Outline Diagram of PL-2528 LQFP64 (7x7mm)

8.2 PL-2528 TQFP64pin (7mm x 7mm) Outline Diagram





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.156			0.046
A1	0.05		0.15	0.002		0.006
A2	0.94	1.00	1.06	0.037	0.039	0.042
c	0.119		0.185	0.005		0.007
c1	0.127 TYP.			0.005 TYP.		
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.95	7.00	7.05	0.273	0.276	0.278
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.95	7.00	7.05	0.273	0.276	0.278
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	1.5	3.5	5.5	1.5	3.5	5.5
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13



	MIN.	NOM.	MAX.	NOM.	MIN.	MAX.	NOM.	MIN.	MAX.
b	0.34		0.45	0.15		0.26	0.15		0.26
b1	0.34	0.37	0.40	0.15	0.18	0.21	0.15	0.18	0.21
e	0.80BSC.			0.50BSC.			0.40BSC.		
N	32			48			64		
JEDEC	MS-026 ABA			MS-026 ABC			MS-026 ABD		

Figure 8-2 Outline Diagram of PL-2528 TQFP64 (7x7mm)

9.0 Document Revision History

Revision	Description	Date
1.5	➢ Section 2: Added Wear Leveling Algorithm Feature	March 28, 2008
1.4	➢ Added TQFP64 (7x7 mm) package information	December 13, 2007
1.3B	➢ Correct Vista Basic Logo on cover page	April 4, 2007
1.3	➢ Section 2: Added Dual Channel Mode Support for both SLC and MLC NAND Flash ➢ Cover Page and Section 2: Added Windows Vista x64 Basic Logo Submission Compliance	December 25, 2006
1.2	➢ Section 2: Added USB-IF Logo Compliant TID ➢ Section 4: Correct Pin Name for Pin 52 (PORT1_1 to WP) and Pin 63 (PORT1_0 to LED).	November 1, 2006
1.1	➢ Revised Datasheet based on Chip Rev 3A	September 14, 2006
1.0	➢ Product Datasheet (Chip Rev A) – Initial Release	December 9, 2005