PL-2520 (Chip Rev A)
Advanced Hi-Speed USB Flash Disk Controller
Product Datasheet

Document Revision: 1.1
Document Release: December 25, 2008

Prolific Technology Inc.

7F, No. 48, Sec. 3, Nan Kang Rd.
Nan Kang, Taipei 115, Taiwan, R.O.C.
Tel: 886-2-2654-6363
Fax: 886-2-2654-6161
Email: sales@prolific.com.tw
URL: http://www.prolific.com.tw

Disclaimer

All the information in this document is subject to change without prior notice. Prolific Technology Inc. does not make any representations or any warranties (implied or otherwise) regarding the accuracy and completeness of this document and shall in no event be liable for any loss of profit or any other commercial damage, including but not limited to special, incidental, consequential, or other damages.

Trademarks

The Prolific logo is a registered trademark of Prolific Technology Inc. All brand names and product names used in this document are trademarks or registered trademarks of their respective holders.

Copyrights

Table of Contents

List of Figures

List of Tables

1.0 Overview

PL-2520 is an advanced Hi-Speed USB Flash Disk controller that allows fast data transfer between USB-equipped hosts (such as PC, PDA, MP3 Player) and NAND Flash Memory through USB port interface at transfer rate of 480Mbps. Advanced mode design allows for PL-2520 USB Flash devices to reach enhanced Read/Write performances of 34MByte/sec and 24MByte/sec respectively. It also allows interface of up to 8 NAND Flash Memory.

The available NAND flash memories on board can generally be used as a normal single disk or partitioned into a standard/open mass storage device and a secured mass storage device. The sizes of the partitions can be easily configured and adjusted by end-users using the USB Flash Disk (UFD) utility program. To access the secured mass storage device or disk, users must first enter the correct password using the UFD utility program.

Other features of PL-2520 are the Read-Only and Hidden Partition (Optional). The PL-2520 allows vendors to create a read-only partition for preloading their software driver and application program to save on driver CD cost and enhance user-friendliness. If a secured partition and password is set, this Read-Only partition will toggle with the Secured partition disk after the password is confirmed. When you plug-in the device, the Read-Only partition and the open partition will first appear and after the end-user enters the password, the Read-Only partition will be removed and the Secured partition will appear. The Hidden partition allows vendors to put their own private application programs and using a special utility to access it. This Hidden partition is not accessible and cannot be seen by end-users. Prolific provides a vendor manufacturing kit utility to customize and preset these special partitions.

To take advantage of Plug and Play, the mass storage device is implemented according to the USB mass storage device class. Since the standard USB mass storage driver is included within the OS, no extra driver is needed for Linux, Mac OS, Windows Vista, and Windows ME/2000/XP/2003 Server. Prolific provides a separate Windows 98 driver and supports driver and utility customization. PL-2520 also supports Vista ReadyBoost requirements for both SLC and MLC NAND flash configurations.

PL-2520 also provides options to customize the chip in showing the vendor identity. Vendors could modify the Vendor ID, Product ID, Language ID, manufacturer string, and product string of the final product for their customization needs. Production configuration and test tool utilities are also provided by Prolific. PL-2520 is the best solution for securer, low power, high performance and compatibility, plug-and-play portable flash storage media.

2.0 Features

- **USB Interface**
  - Supports standard USB (Universal Serial Bus) interface
  - Fully USB 2.0 bus powered compliant and fully compatible with USB 1.1 and 2.0
  - Hi-Speed USB-IF Logo Compliant with TID 40000402
  - Integrated USB 2.0 Transceiver Macrocell Interface and Serial Interface Engine
  - Supports Hi-Speed (480 Mbps), Full Speed (12 Mbps), Low Speed (1.5 Mbps) transfer
  - 4 End points support Control, Interrupt, Bulk-In, and Bulk-Out
  - Multiple 512-Byte FIFO for Bulk In and Bulk Out Data Transfer
  - Optional Embedded hub technology to implement USB compound device application
  - USB power saving support
  - Built-in USB mass storage driver support in Windows® Vista, XP, 2003 Server, 2000, and ME (Prolific provides Windows 98 driver support), Linux Kernel 2.4.18 and above, MAC OS 9.x and above (Apple website provides Mac OS 8.6 driver support).
  - Supports Windows Vista ReadyBoost requirements for both SLC and MLC

- **Error Correction Logic**
  - Error Correction of 4 bits random error per 512 Bytes of data
  - Automatic on-the-fly, in-buffer error correction

- **Flash Memory Control**
  - Flash Sequencer Logic to support all the control signals to execute read/write/erase operation automatically
  - Flash Write Protect control support
  - Supports Samsung/Toshiba/Hynix/ST/Infineon/Micron SLC NAND type flash memories
  - Supports Samsung/Hynix/Sandisk/Toshiba MLC flash memories
  - 8/16-bit Flash Data I/O
  - Dual-channel mode support for SLC and MLC NAND flash memories
  - Universal flash memory support
  - In-System Programming to upgrade firmware easily
  - Supports up to 8 NAND flash memories in 64 pin package
  - Supports up to 8 NAND flash memories in 48 pin package
  - Non-Stop Writing® (NSW) Technology (Gain 20% Write Performance)

- **Miscellaneous:**
  - Built-in multi-voltage regulator for 5V/3.3V/1.8V (No extra regulator needed)
  - 12MHz external clock
  - Integrated RISC micro-controller
  - Small form factor- LQFP64, LQFP48, and TQFP48 package (7x7 mm)
  - Configurable Vendor ID/Product ID
  - LED indicator to show access status
  - Software support includes Disk partitions and password check for security disk, PC boot-up as USB Zip Disk and USB Hard Disk, and CD-ROM type emulation.
  - Certified for Windows Vista logo compliant

3.0 Functional Block Diagram

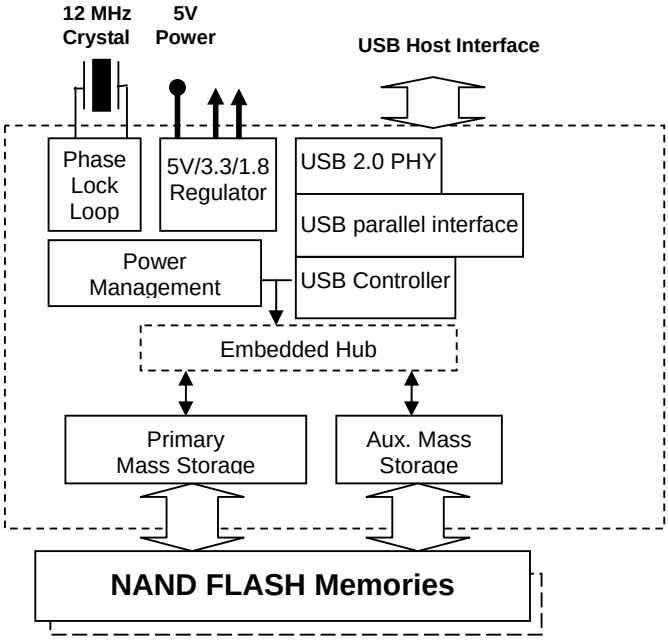


Figure 3-1 Block Diagram of PL-2520

4.0 Pin Assignment and Description

4.1 64-Pin Package

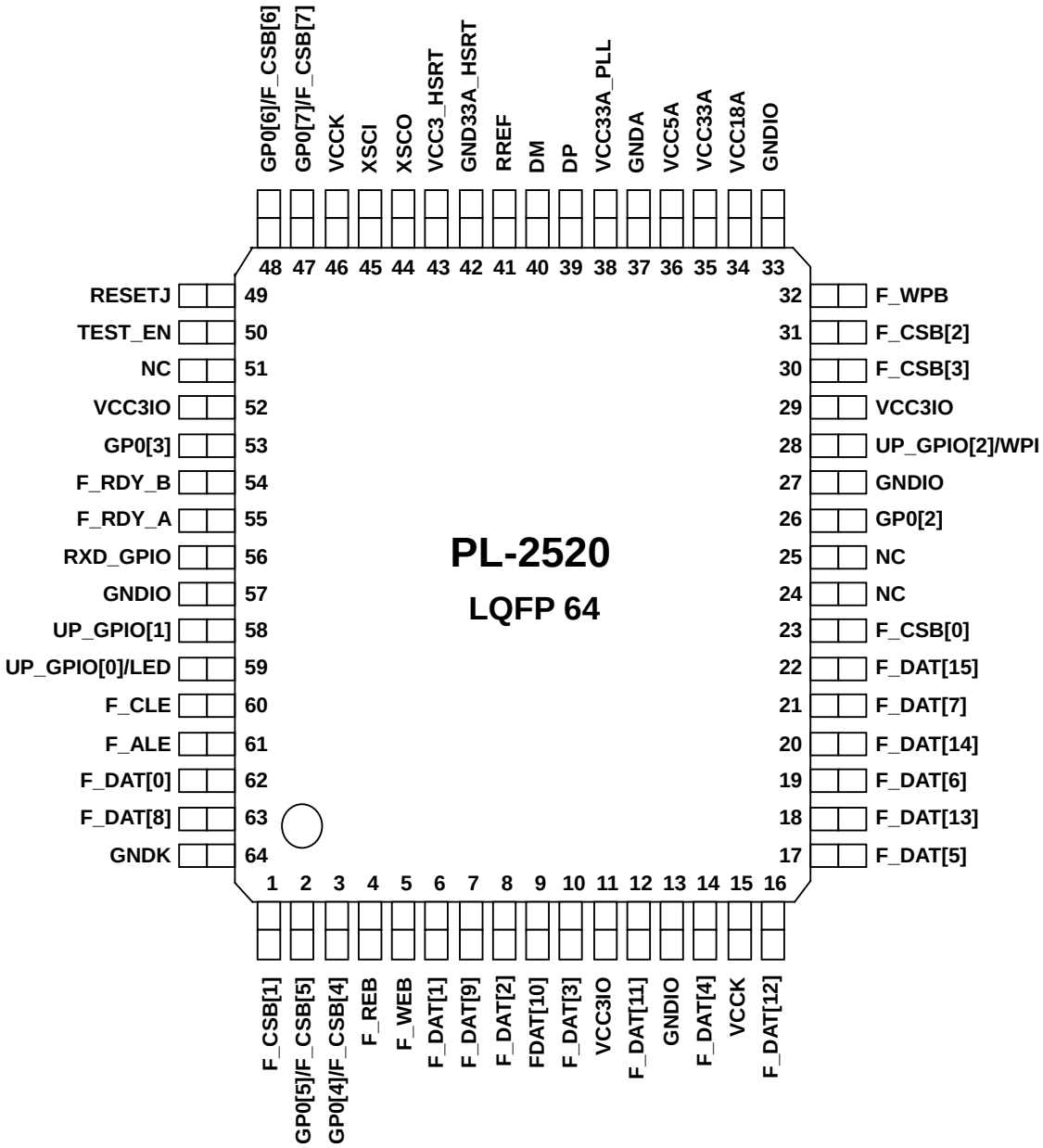


Figure 4-1 Pin Assignment of PL-2520 LQFP64

Table 4-1 Pin Descriptions of PL-2520 LQFP64

Pin No.	Pin Name	Pin Description	Notes
1	F_CSB[1]	Flash Chip Select 1	
2	GP0[5]/F_CSB[5]	GPIO/Flash Chip Select 5	
3	GP0[4]/F_CSB[4]	GPIO/Flash Chip Select 4	
4	F_REB	Flash Read Enable	
5	F_WEB	Flash Write Enable	
6	F_DAT[1]	Flash Data Bus 1	
7	F_DAT[9]	Flash Data Bus 9	
8	F_DAT[2]	Flash Data Bus 2	
9	F_DAT[10]	Flash Data Bus 10	
10	F_DAT[3]	Flash Data Bus 3	
11	VCC3IO	VCC I/O	3.3V
12	F_DAT[11]	Flash Data Bus 11	
13	GNDIO	Ground	
14	F_DAT[4]	Flash Data Bus 4	
15	VCCK	VCC core	1.8V only
16	F_DAT[12]	Flash Data Bus 12	
17	F_DAT[5]	Flash Data Bus 5	
18	F_DAT[13]	Flash Data Bus 13	
19	F_DAT[6]	Flash Data Bus 6	
20	F_DAT[14]	Flash Data Bus 14	
21	F_DAT[7]	Flash Data Bus 7	
22	F_DAT[15]	Flash Data Bus 15	
23	F_CSB[0]	Flash Chip Select 0	
24	NC		
25	NC		
26	GP0[2]	GPIO	
27	GNDIO	Ground	
28	UP_GPIO[2]/WPI	GPIO	For Write Protect switch input
29	VCC3IO	VCC I/O	
30	F_CSB[3]	Flash Chip Select 3	
31	F_CSB[2]	Flash Chip Select 2	
32	F_WPB	Flash Write Protect	
33	GNDIO	Ground	
34	VCC18A	Regulator 1.8V output	
35	VCC33A	Regulator 3.3V output	
36	VCC5A	Regulator 5V input	
37	GNDA	Analog Ground	
38	VCC33A_PLL	Analog Power Supply	3.3V
39	DP	USB Data Positive Pin	
40	DM	USB Data Negative Pin	
41	RREF	Connect External Reference Register to Analog Ground	12KΩ +/- 1%

(cont…)

Table 4-1 Pin Descriptions of PL-2520 LQFP64 (cont…)

Pin No.	Pin Name	Pin Description	Notes
42	GND33A_HSRT	Analog Ground	
43	VCC3_HSRT	Analog Power Supply	3.3V
44	XSCO	Crystal Oscillator Output	12MHz
45	XSCI	Crystal Oscillator input	12MHz
46	VCCK	VCC core	1.8V only
47	GP0[7]/F_CSB[7]	GPIO/Flash Chip Select 7	
48	GP0[6]/F_CSB[6]	GPIO/Flash Chip Select 6	
49	RESETJ	External Reset, low active	
50	TEST_EN	Test Mode Enable, high active	
51	NC	No Connection	
52	VCC3IO	VCC I/O	3.3V
53	GP0[3]	GPIO	
54	F_RDY_B	Flash B Busy/Ready	
55	F_RDY_A	Flash A Busy/Ready	
56	RXD_GPIO	Reserved	
57	GNDIO	Ground	
58	UP_GPIO[1]	GPIO	
59	UP_GPIO[0]/LED	GPIO	For LED Indicator
60	F_CLE	Flash Command Latch Enable	
61	F_ALE	Flash Address Latch Enable	
62	F_DAT[0]	Flash Data Bus 0	
63	F_DAT[8]	Flash Data Bus 8	
64	GNDK	Ground	

4.2 48-Pin Package

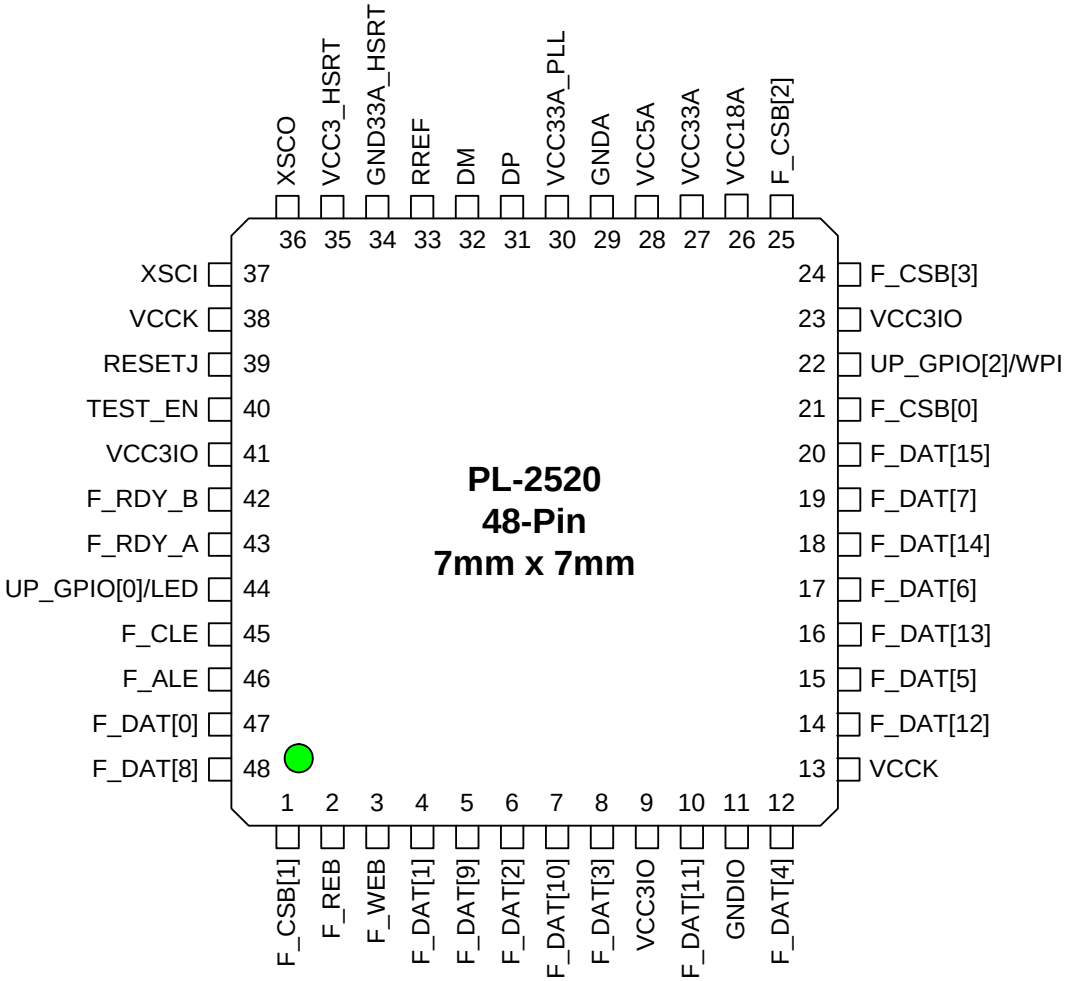


Figure 4-2 Pin Assignment of PL-2520 LQFP48 (TQFP48)

Table 4-2 Pin Descriptions of PL-2520 LQFP48/TQFP48

Pin No.	Pin Name	Pin Description	Notes
1	F_CSB[1]	Flash Chip Select 1	
2	F_REB	Flash Read Enable	
3	F_WEB	Flash Write Enable	
4	F_DAT[1]	Flash Data Bus 1	
5	F_DAT[9]	Flash Data Bus 9	
6	F_DAT[2]	Flash Data Bus 2	
7	F_DAT[10]	Flash Data Bus 10	
8	F_DAT[3]	Flash Data Bus 3	
9	VCC3IO	VCC I/O	3.3V
10	F_DAT[11]	Flash Data Bus 11	
11	GNDIO	Ground	
12	F_DAT[4]	Flash Data Bus 4	
13	VCCK	VCC core	1.8V only
14	F_DAT[12]	Flash Data Bus 12	
15	F_DAT[5]	Flash Data Bus 5	
16	F_DAT[13]	Flash Data Bus 13	
17	F_DAT[6]	Flash Data Bus 6	
18	F_DAT[14]	Flash Data Bus 14	
19	F_DAT[7]	Flash Data Bus 7	
20	F_DAT[15]	Flash Data Bus 15	
21	F_CSB[0]	Flash Chip Select 0	
22	UP_GPIO[2]/WPI	GPIO	For Write Protect switch input
23	VCC3IO	VCC I/O	3.3V
24	F_CSB[3]	Flash Chip Select 3	
25	F_CSB[2]	Flash Chip Select 2	
26	VCC18A	Regulator 1.8V output	
27	VCC33A	Regulator 3.3V output	
28	VCC5A	Regulator 5V input	
29	GNDA	Analog Ground	
30	VCC33A_PLL	Analog Power Supply	3.3V
31	DP	USB Data Positive Pin	
32	DM	USB Data Negative Pin	
33	RREF	Connect External Reference Register to Analog Ground	12KΩ +/- 1%
34	GND33A_HSRT	Analog Ground	
35	VCC3_HSRT	Analog Power Supply	3.3V
36	XSCO	Crystal Oscillator Output	12MHz
37	XSCI	Crystal Oscillator input	12MHz
38	VCCK	VCC core	1.8V only
39	RESETJ	External Reset, low active	
40	TEST_EN	Test Mode Enable, high active	

(cont…)

Table 4-2 Pin Descriptions of PL-2520 LQFP48/TQFP48 (cont…)

Pin No.	Pin Name	Pin Description	Notes
41	VCC3IO	VCC I/O	3.3V
42	F_RDY_B	Flash B Busy/Ready	
43	F_RDY_A	Flash A Busy/Ready	
44	UP_GPIO[0]/LED	GPIO	For LED Indicator
45	F_CLE	Flash Command Latch Enable	
46	F_ALE	Flash Address Latch Enable	
47	F_DAT[0]	Flash Data Bus 0	
48	F_DAT[8]	Flash Data Bus 8	

5.0 DC Characteristics

5.1 Recommended Operation Conditions

Table 5-1 Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCCK	Core Power Supply	1.65	1.8	1.95	V
VCC3IO	Power Supply	3.0	3.3	3.6	V

5.2 General DC Characteristics

Table 5-2 General DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{in}	Input leakage current	Vin= VCC3V or 0	-10	± 1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
V_{IL}	Input low voltage	LVTTL			0.8	V
V_{IH}	Input high voltage	LVTTL	2.0			V
V_{OL}	Output low voltage	Iol=2~16mA			0.4	V
V_{OH}	Output high voltage	Iol=2~16mA	2.4			V
R_I	Input pull up/down resistance	Vin=VCC3V(up) Vin=0(down)	40	75	190	kΩ

Note: Multi-voltage I/O buffers operating under 3.3V

6.0 AC Characteristics

6.1 Flash Read/Write Timing

6.1.1 Tc = 36 ns

Table 6-1 AC Characteristics (Tc=36ns)

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		36		ns
$Ts_{(FW)}$	FD set up time of FWE#	15			ns
$Th_{(FW)}$	FD hold time of FWE#	10			ns
$Ts_{(FR)}$	FD set up time of FRD#	5			ns
$Th_{(FR)}$	FD hold time of FRD#	-			ns

6.1.2 Tc = 54 ns

Table 6-2 AC Characteristics (Tc=54ns)

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		54		ns
$Ts_{(FW)}$	FD set up time of FWE#	20			ns
$Th_{(FW)}$	FD hold time of FWE#	20			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

6.1.3 Tc = 72 ns

Table 6-3 AC Characteristics (Tc=72ns)

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		72		ns
$Ts_{(FW)}$	FD set up time of FWE#	35			ns
$Th_{(FW)}$	FD hold time of FWE#	30			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

6.1.4 Tc = 108 ns

Table 6-4 AC Characteristics (Tc=108ns)

Symbol	Description	Min	Typ	Max	Units
$Tc_{(F)}$	Flash Read / Write cycle time		108		ns
$Ts_{(FW)}$	FD set up time of FWE#	60			ns
$Th_{(FW)}$	FD hold time of FWE#	40			ns
$Ts_{(FR)}$	FD set up time of FRD#	10			ns
$Th_{(FR)}$	FD hold time of FRD#	5			ns

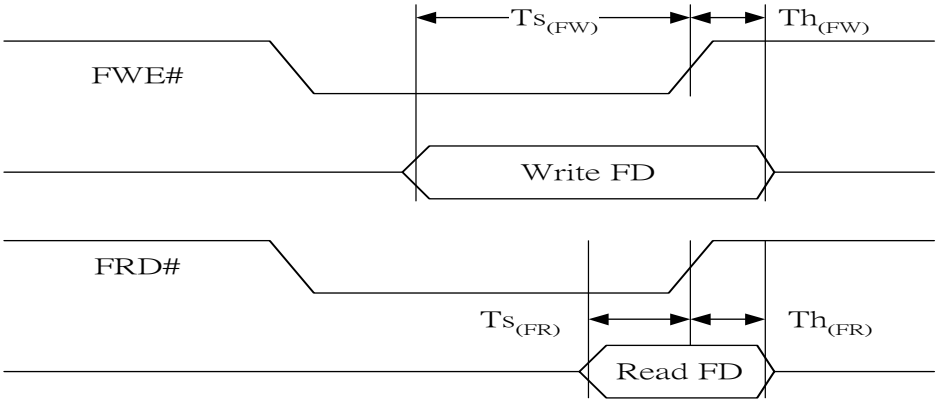


Figure 6-1 Flash Read/Write Timing Diagram

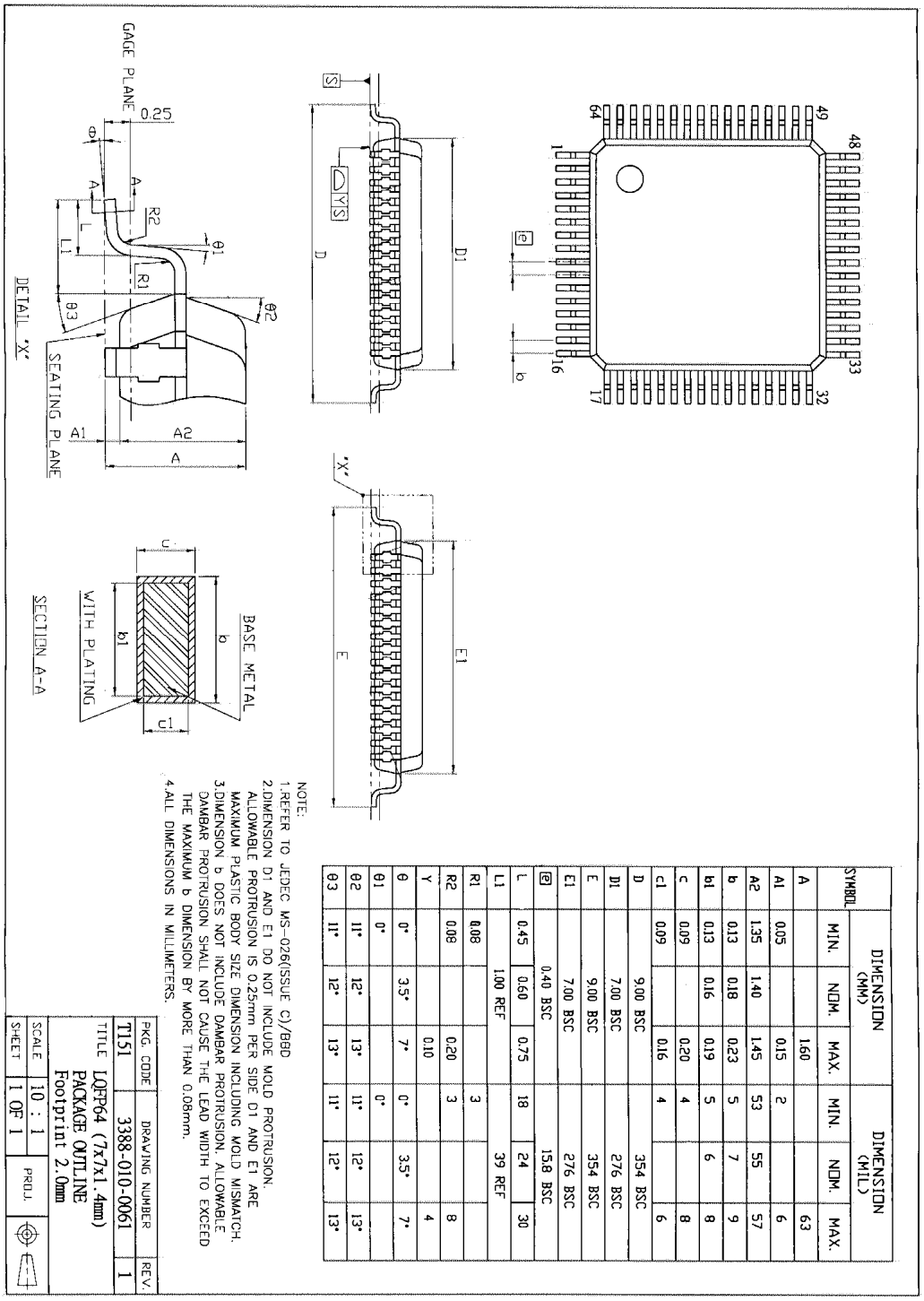
7.0 Ordering Information

Table 7-1 Ordering Information

Part Number	Package Type
PL-2520 LQFP64	64-pin LQFP (7x7mm) Lead-Free or Pb-Free
PL-2520 LQFP48	48-pin LQFP (7x7mm) Lead-Free or Pb-Free
PL-2520 TQFP48	48-pin TQFP (7x7mm) Lead-Free or Pb-Free

8.0 Outline Diagram

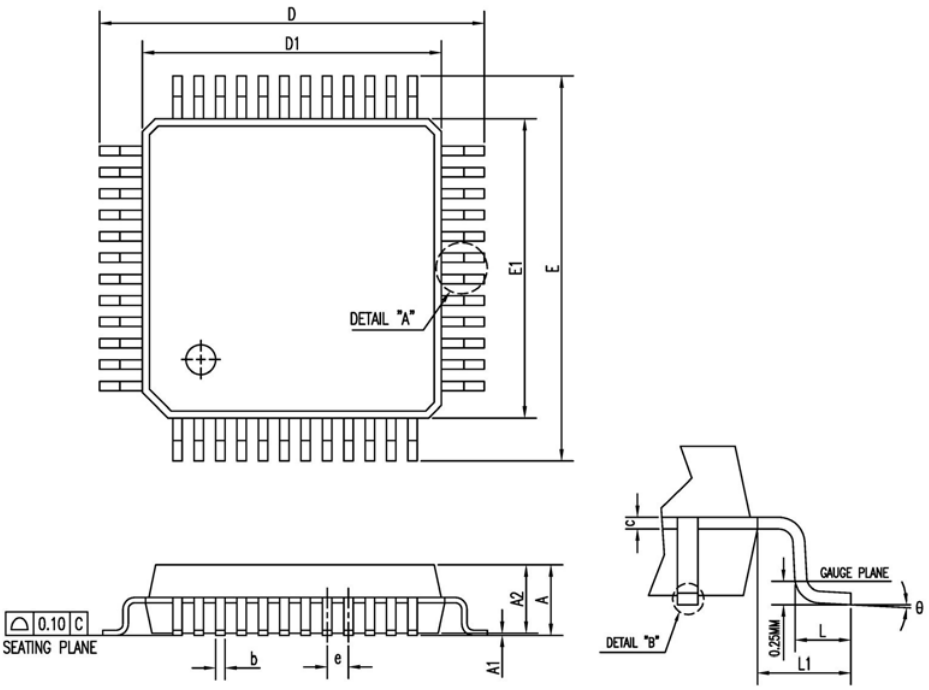
8.1 LQFP64pin (7mm x 7mm) Outline Diagram

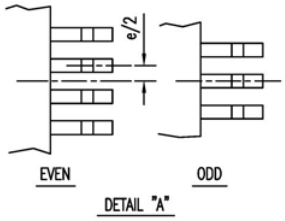


SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
e		0.40 BSC			15.8 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

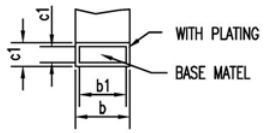
Figure 8-1 Outline Diagram of PL-2520 LQFP64 (7x7mm)

8.2 LQFP48pin (7mm x 7mm) Outline Diagram





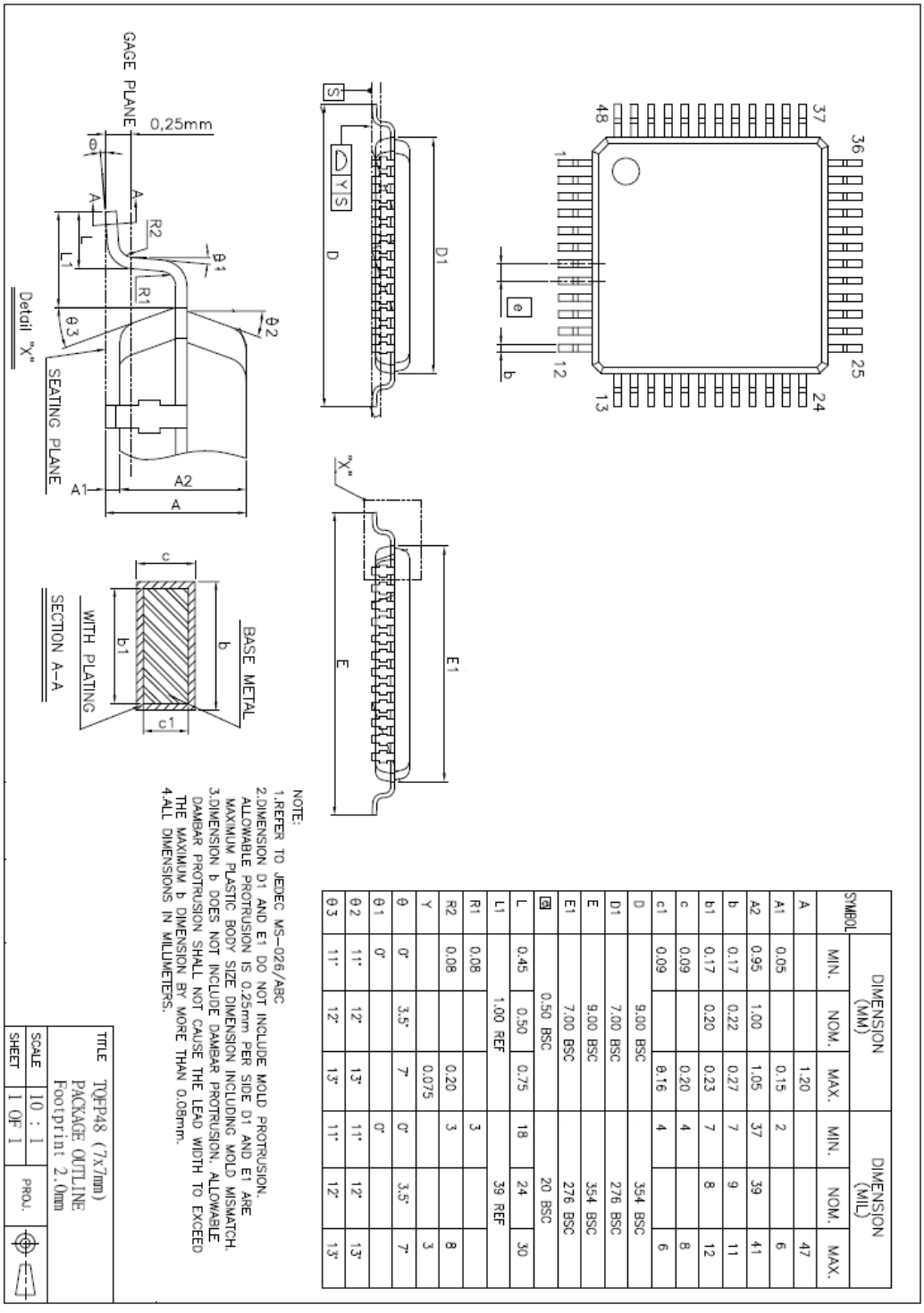
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.129 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						



	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			

Figure 8-2 Outline Diagram of PL-2520 LQFP48 (7x7mm)

8.3 TQFP48pin (7mm x 7mm) Outline Diagram



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.20			47
A1	0.05		0.15	2		6
A2	0.95	1.00	1.05	37	39	41
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.50 BSC			20 BSC		
L	0.45	0.50	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08		0.20	3		8
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

Figure 8-3 Outline Diagram of PL-2520 TQFP48 (7x7mm)

9.0 Document Revision History

Revision	Description	Date
1.1	➢ Modify LQFP64 supports up to 8 NAND Flash Memory	December 25, 2008
1.0	➢ PL-2520 Product Datasheet (Chip Rev A) – Formal Release	December 6, 2007