NEC Electronics Inc.

# μPD75P56/P66
# 4-Bit, Single-Chip, One-Time Programmable (OTP) CMOS Microcomputers With Comparator

## Description

The μPD75P56 and μPD75P66 are 1024 x 8-bit, on-chip, one-time programmable (OTP) ROM versions of the mask ROMs, μPD7556 and μPD7566. They have the same functions as, and are pin-compatible with, their mask ROMs. Because of their programming capabilities, the μPD75P56/P66 are suitable for evaluation and small lot production for system development. Their unique features will be described in this data sheet. For information about the base part μPD7556/66, please refer to its data sheet.

## Features

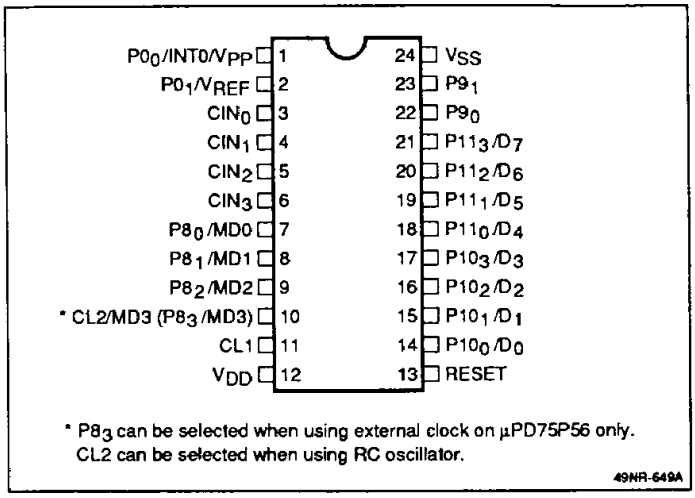
- 45 instructions (subset of μPD7500 set B)
- Instruction cycle:
  - — External clock (μPD75P56): 2.86 μs/700 kHz, 5 V
  - — RC oscillator (μPD75P56); 4 μs/500 kHz, 5 V
  - — Ceramic resonator (μPD75P66): 2.86 μs/700 kHz, 5 V
- Program memory (ROM) of 1024 x 8 bits
- Data memory (RAM) of 64 x 4 bits
- 8-bit timer/event counter
- 4-channel comparator
- I/O lines: 20-μPD75P56; 19-μPD75P66
- One-time programmable
  - — No mask option available
- Data memory retention at low supply voltage
- Standby (STOP/HALT) functions
- CMOS technology
- Low-power consumption
- Single power supply
  - — 4.5 to 6.0 V, normal operation

## Ordering Information

| Part Number | Package Type |
|---|---|
| μPD75P56CS-001 | 24-pin plastic shrink DIP (OTP) |
| μPD75P56CS-012 | |
| μPD75P66CS-001 | |
| μPD75P56G-511 | 24-pin plastic SOP (OTP) |
| μPD75P56G-512 | |
| μPD75P66G-511 | |

## Pin Configuration

***24-Pin Plastic Shrink DIP or SOP (OTP)***




* P83 can be selected when using external clock on μPD75P56 only.
CL2 can be selected when using RC oscillator.

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## Pin Identification

| Symbol | Function |
|---|---|
| $P0_0$/INT0/$V_{PP}$ | 2-bit input port 0/testable input pin/ programming voltage supply pin for program memory write/verify |
| $V_{REF}$ | Comparator reference voltage input pin |
| $CIN_0$<br>$CIN_1$<br>$CIN_2$<br>$CIN_3$ | 4-channel comparator inputs |
| $P8_0$-$P8_2$/$MD_0$-MD2<br>CL2/MD3<br>($P8_3$/MD3) | 4-bit output port 8/OTP operation mode/ connection for RC oscillator or ceramic resonator (No $P8_3$ on μPD75P66) (Note 1) |
| CL1 | Connection for ceramic resonator or RC oscillator |
| $V_{DD}$ | Power supply. 4.5 to 6.0 V (normal); 6.0 V (OTP) |
| RESET | Reset input pin |
| $P10_1$-$P10_3$/<br>$D_0$-$D_3$ | 4-bit I/O port 10/$D_0$-$D_3$ during programming write/verify |
| $P11_0$-$P11_3$/<br>$D_4$-$D_7$ | 4-bit I/O port 11/ $D_4$-$D_7$ during programming write/verify |
| $P9_0$-$P9_1$ | 2-bit output port 9 |
| $V_{SS}$ | Ground |

**Notes:**

(1) MD0-MD3 are used as mode selection pins during programming.

## PIN FUNCTIONS

### $P0_0$/INT0/$V_{PP}$, $V_{REF}$ (Port 0/Count clock input/Programming/ Comparator reference voltage input)

Two-bit input port 0/count clock input/programming/ comparator reference voltage input. INT0 is an edge-sensitive testable input pin that detects a signal at the rising edge. $V_{PP}$ is the programming supply pin for programming memory write/verify. $V_{REF}$ is the comparator reference voltage input pin. If $P0_0$/INT0/$V_{REF}$ is unused; connect it to ground. The port is in the input state at reset.

### $CIN_0$-$CIN_3$ (Comparator inputs)

Four-channel comparator inputs. Analog voltage input is compared with the reference voltage ($V_{REF}$). The comparison requires up to three machine cycles. To obtain the comparison result after changing the voltage applied to the $V_{REF}$ pin by port output (OPL), and connecting the A/D converter via the resistor ladder, execute the input instruction (IP1 or IPL, L = 1) after waiting three machine cycles following the execution of OPL.

### $P8_0$-$P8_2$/MD0-MD2, $P8_3$/MD3 or CL2/MD3 (Port 8/Clock input 2/Mode selection for OTP)

Four-bit output port 8. This port can sink 15 mA and interface 12 V. $P8_3$ is a output port on the μPD75P56. On the μPD75P56, CL2 is one of the pins to which a resistor for RC oscillation is connected. On the μPD75P66 CL2 is one of the pins to which a ceramic resonator is connected. If any of $P8_0$-$P8_2$ pins are unused, leave them open. The port is in the high impedance state at reset. MD0-MD3 are used for OTP program memory write and read mode selection. There is no $P8_3$ on μPD75P66.

### CL1 (Clock input 1)

On the μPD75P56, CL1 is one of the two pins to which a resistor for RC oscillation is connected. On the μPD75P66, CL1 is one of the two pins to which a ceramic resonator is connected.

### $V_{DD}$ (Power supply)

Positive power supply. 4.5 to 6.0 V for normal operation. 6.0 V for program memory write/verify.

### RESET (Reset)

System reset input pin (active high). This pin is not internally connected to a pull-down resistor.

### $P10_0$-$P10_3$/$D_0$-$D_3$ (Port 10/Data I/O)

Four-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or $V_{DD}$ in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset. $D_0$-$D_3$ are four-bit I/O pins for program memory write/verify.

### $P11_0$-$P11_3$/$D_4$-$D_7$ (Port 11/Data I/O)

Four-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or $V_{DD}$ in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset. $D_4$-$D_7$ are four-bit I/O pins for program memory write/verify.

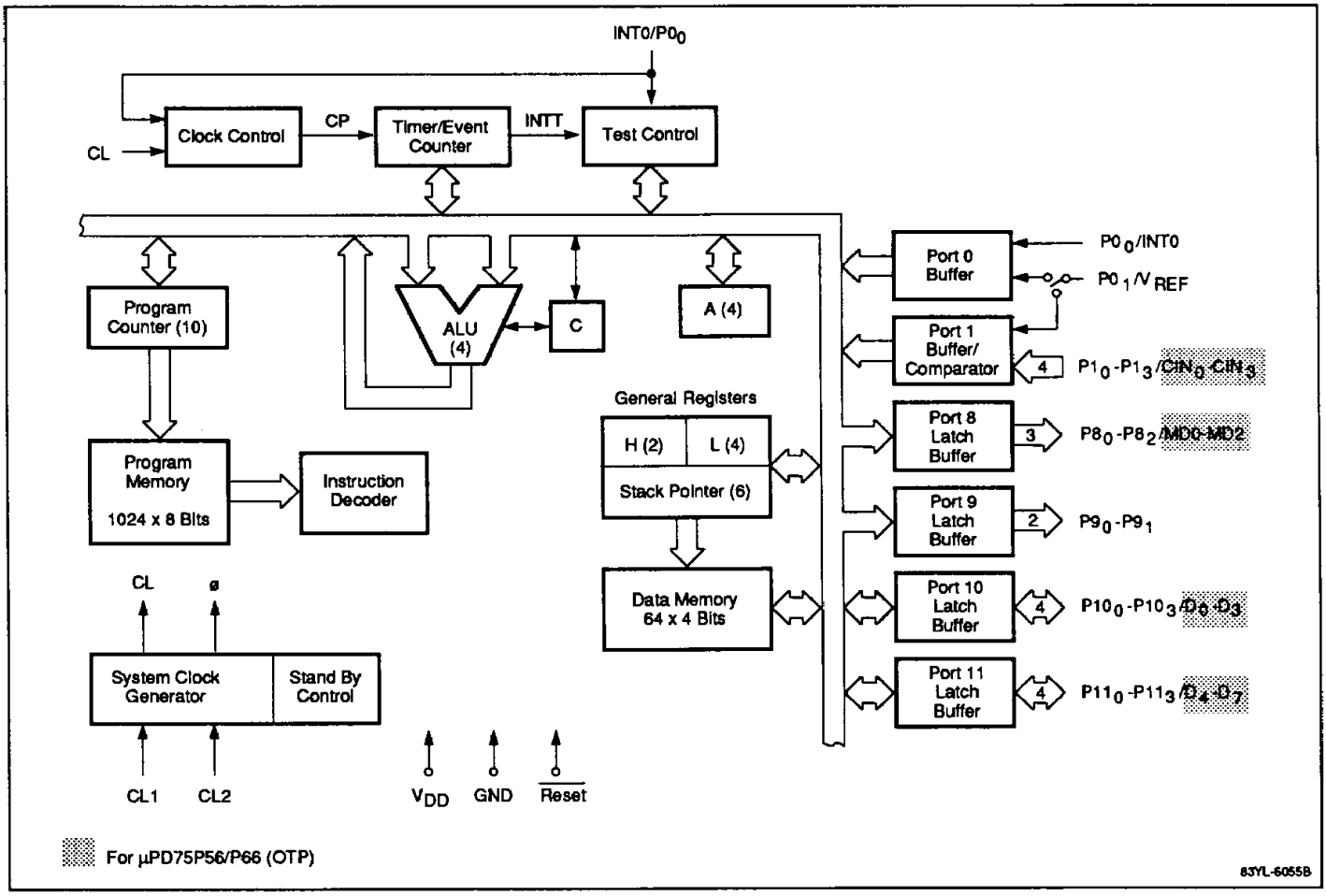
### $P9_0$-$P9_1$ (Port 9)

Two-bit output port. This port sinks 15 mA and can interface to 12 V. If either of these pins is unused, leave it open. The port is in the high impedance state at reset.

### $V_{SS}$ (Ground)

Ground.

### Block Diagram



## FUNCTIONAL DESCRIPTION

### I/O Ports

Figure 1 shows the internal circuits at the I/O ports.

***Figure 1. Interface at I/O Ports***

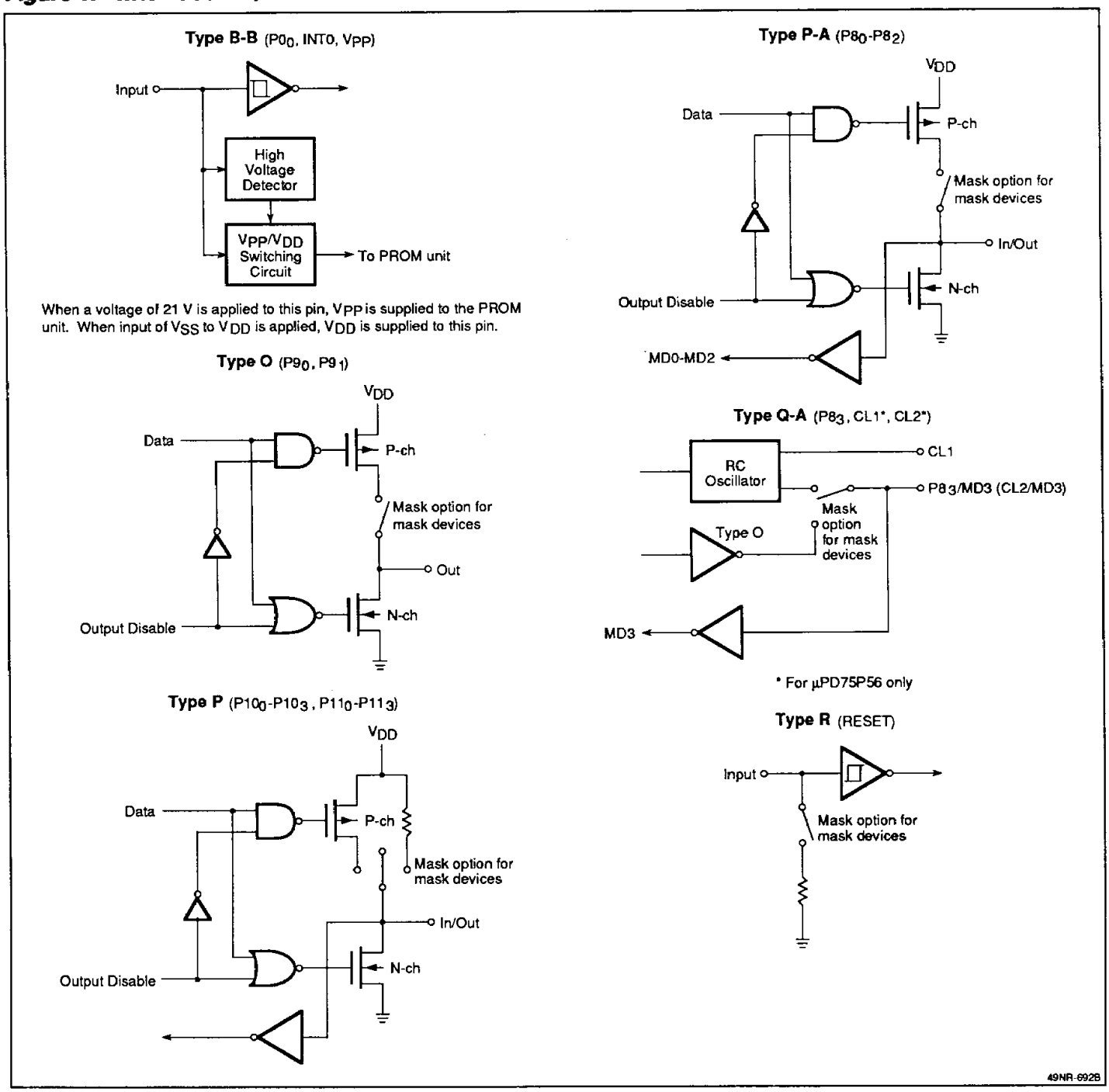
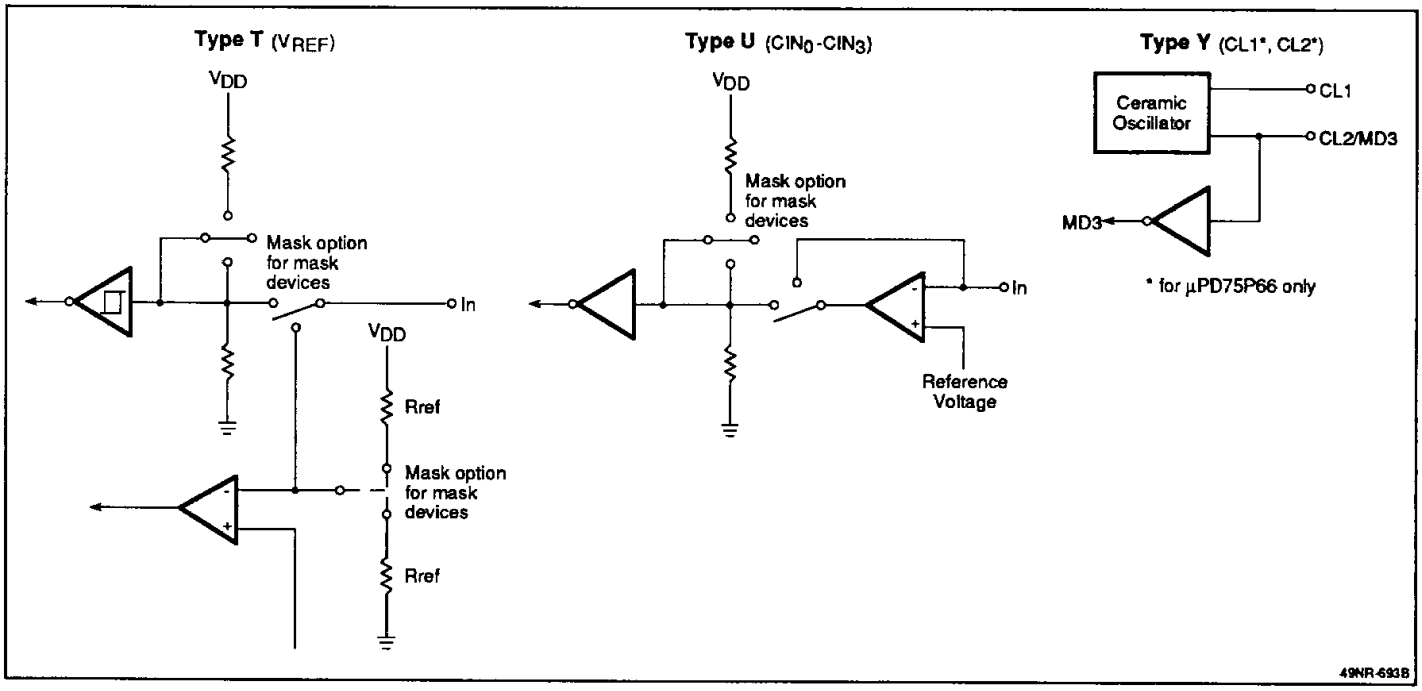


***Figure 1. Interface at I/O Ports (cont)***

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## μPD75P56/P66 and μPD7556/66 Comparisons

Table 1 compares the features of OTP μPD75P56/P66 and their mask ROMs, μPD7556/66.

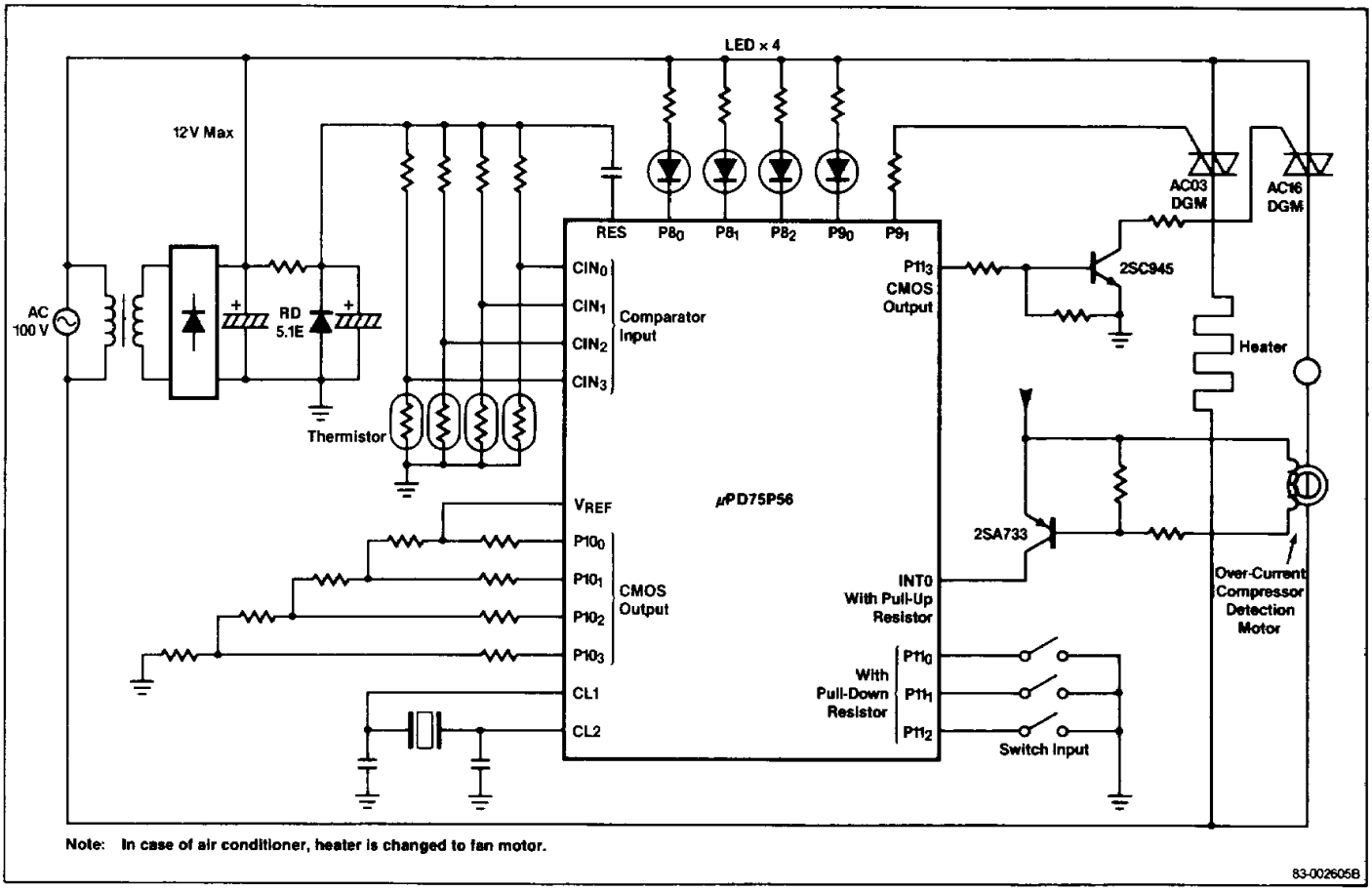
***Table 1. Product Comparisons, μPD75P56/P66 and μPD7556/66***

| Item | | μPD75P56 (OTP) | μPD75P66 (OTP) | μPD7556 | μPD7566 |
|---|---|---|---|---|---|
| Instruction cycle/system clock (5 V) | RC | 4 μs/500 kHz | | 4 μs/500 kHz | |
| | External | 2.86 μs/700 kHz | | 2.86 μs/700 kHz | |
| | Ceramic | | 2.86 μs/700 kHz | | 2.86 μs/700 kHz |
| Instruction set | | 45 (set B) | 45 (set B) | 45 (set B) | 45 (set B) |
| ROM | | 1024 x 8 | 1024 x 8 | 1024 x 8 | 1024 x 8 |
| RAM | | 64 x 4 | 64 x 4 | 64 x 4 | 64 x 4 |
| I/O port total | | 20 (max) | 19 | 20 (max) | 19 |
| Port 0 | | $P0_0$-$P0_1$ | $P0_0$-$P0_1$ | $P0_0$-$P0_1$ | $P0_0$-$P0_1$ |
| Port 1 | | $CIN_0$-$CIN_3$ | $CIN_0$-$CIN_3$ | $P1_0$-$P1_3$ | $P1_1$-$P1_3$ |
| Port 8 | | $P8_0$-$P8_2$/MD0-MD2<br>$P8_3$/MD3 | $P8_0$-$P8_2$/MD0-MD2<br>CL2/MD3 | $P8_0$-$P8_2$<br>$P8_3$/CL2 | $P8_0$-$P8_2$<br>$P8_2$/CL2 |
| Port 9 | | $P9_0$-$P9_1$ | $P9_0$-$P9_1$ | $P9_0$-$P9_1$ | $P9_0$-$P9_1$ |
| Port 10 | | $P10_0$-$P10_3$/$D_0$-$D_3$ | $P10_0$-$P10_3$/$D_0$-$D_3$ | $P10_0$-$P10_3$ | $P10_0$-$P10_3$ |
| Port 11 | | $P11_0$-$P11_3$/$D_4$-$D_7$ | $P11_0$-$P11_3$/$D_4$-$D_7$ | $P11_0$-$P11_3$ | $P11_0$-$P11_3$ |
| Timer/Event counter | | 8-bit | 8-bit | 8-bit | 8-bit |
| Output and I/O pins | | No on-chip resistor | No on-chip resistor | Mask options available | Mask options available |
| RESET | | No pull-down resistor | No pull-down resistor | Mask options available | Mask options available |
| Comparator | | 4-channel | 4-channel | 4-channel | 4-channel |
| Process | | CMOS | CMOS | CMOS | CMOS |
| Package | | 24-pin plastic SOP (OTP)<br>24-pin shrink DIP (OTP) | 20-pin plastic SOP (OTP)<br>20-pin shrink DIP (OTP) | 24-pin plastic SOP<br>24-pin shrink DIP | 24-pin plastic SOP<br>24-pin shrink DIP |

## μPD75P56 Application

Figure 2 gives an application example of a refrigerator or air conditioner circuitry.

***Figure 2 Refrigerator or Air Conditioner Circuitry***




Note: In case of air conditioner, heater is changed to fan motor.

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## OTP PROM (Program Memory Write and Verify)

The μPD75P56/P66 is a one-time programmable (OTP) PROM version of the μPD7556/66. The OTP is programmed by the pins and their functions listed in table 2. During OTP programming, addresses are updated by inputting clocks, instead of addresses, from the CL1 pin.

***Table 2. OTP Access***

| Pin | Function |
|---|---|
| $V_{PP}$ | OTP programming voltage pin (normally $V_{DD}$) |
| CL1 | Address update clock input during programming |
| MD0-MD3 | Mode selection during OTP programming |
| $D_0$-$D_7$ | 8-bit data I/O pins during OTP programming |
| $V_{DD}$ | Supply voltage pin: 4.5 to 6.0 V during normal operation; 6 V during OTP programming |

**Notes:**

The μPD75P56/P66 has no erasure window. The program memory data cannot be erased with ultraviolet light.

## OTP Operation Mode

The μPD75P56/P66 operates in the program memory write/verify mode when +6 V is applied to $V_{DD}$ and +21 V to $V_{PP}$. Mode pins MD0-MD3 select the operation modes shown in table 3.

***Table 3. OTP Operation Mode Selection (Note 1)***

$V_{PP}$ = +21 V; $V_{DD}$ = +6 V

| MD0 | MD1 | MD2 | MD3 | Operating Mode |
|---|---|---|---|---|
| H | L | H | L | Program memory address clear (Note 2) |
| L | H | H | H | Program memory write (Note 3) |
| L | L | H | H | Program memory verify (Note 4) |
| H | X | H | H | Program inhibit (Note 5) |

**Notes:**

(1) X = L or H.

(2) While HLHL is applied, the program counter is cleared.

(3) While LHHH is applied, data applied to $D_0$-$D_7$ is written to the OTP.

(4) While LLHH is applied, the OTP contents at the address which the program counter indicates output to $D_0$-$D_7$.

(5) While HXHH is applied, the OTP is nonaccessible, and $D_0$-$D_7$ are set to high impedance.

**Program Memory Write Procedure.** The program memory write procedure follows (Data can be written at high speeds.):

(1) Connect unused pins to $V_{SS}$ through a pull-down resistor. RESET is pulled up to $V_{DD}$ through a resistor. Set CL1 low.

(2) Supply 5 V to $V_{DD}$ and $V_{PP}$.

(3) Select the program memory address clear mode (HLHL).

(4) Change the voltage on $V_{DD}$ to 6 V, and on $V_{PP}$ to 21 V.

(5) Select the program inhibit mode (HXHH).

(6) Write data in the 1 ms write mode (LHHH).

(7) Select the program inhibit mode (HXHH).

(8) Select the verify mode (LLHH). After data is written, proceed to step 9; if data is not written, repeat steps 6-8.

(9) Perform one additional write.

(10) Select the program inhibit mode (HXHH).

(11) Increment the program memory address by one, by inputting four pulses to CL1.

(12) Repeat steps 6-11 until the end address occurs.

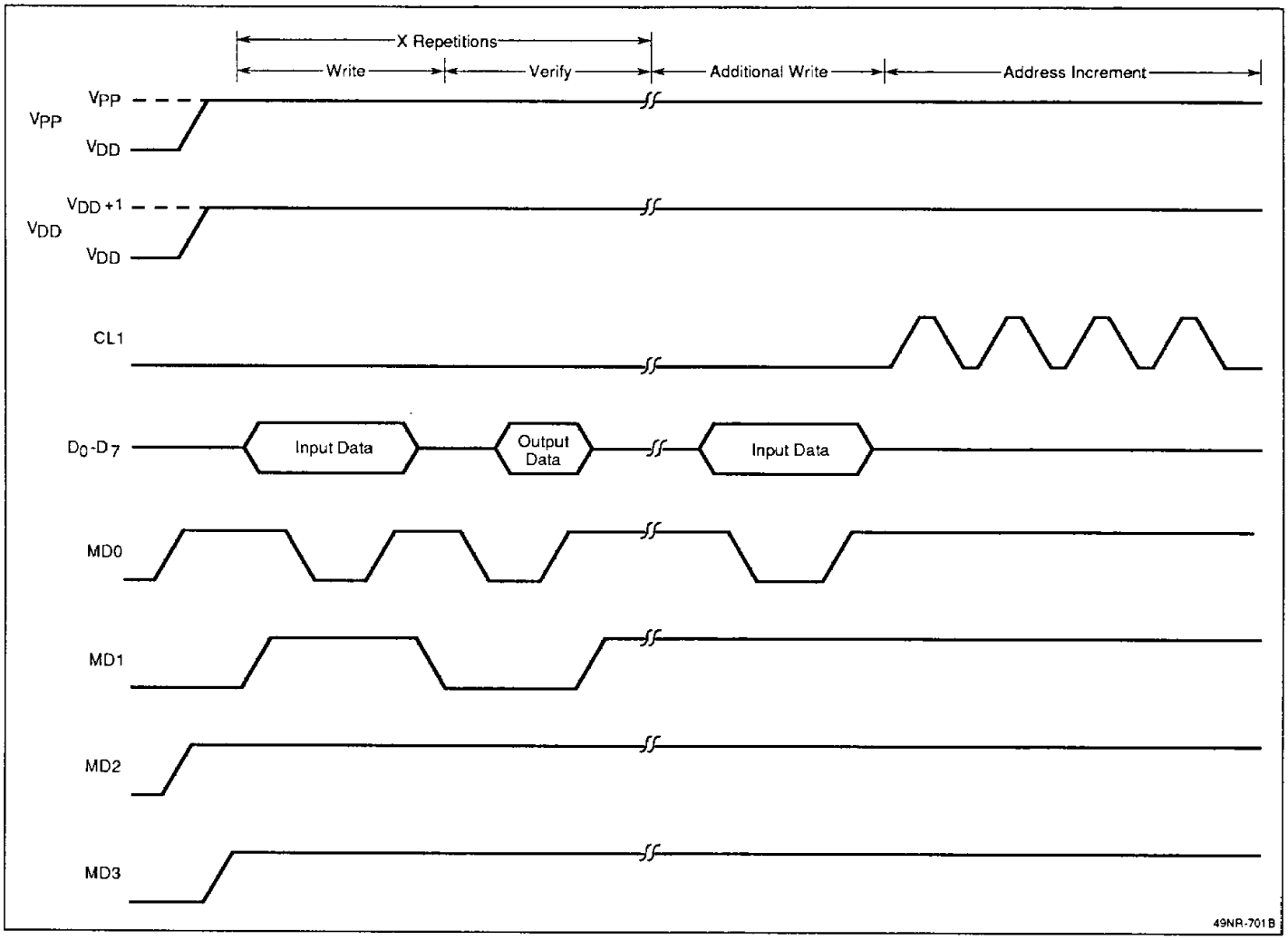
(13) Select the program memory address clear mode (HLHL).

(14) Change the voltage on $V_{DD}$ and $V_{PP}$ to 5 V.

(15) Turn off power.

The timing for steps 2-11 is shown in figure 3.

***Figure 3. Timing Diagram for OTP Program Memory Write***




**Program Memory Read Procedure.** The program memory read procedure follows:

(1) Connect unused pins to $V_{SS}$ through a pull-down resistor. RESET is pulled up to $V_{DD}$ through a resistor. Set CL1 low.

(2) Supply 5 V to $V_{DD}$ and $V_{PP}$.

(3) Select the program memory address clear mode (HLHL).

(4) Change the voltage on $V_{DD}$ to 6 V, and on $V_{PP}$ to 21 V.

(5) Select the program inhibit mode (HXHH).

(6) Select the verify mode (LLHH). Data is read from 000H. Each time four clock pulses are input to the X1 pin, data from one address is output.

(7) Pulse input to the CL1. Program memory address is updated at the rising edge of the third pulse. Address after updated one (+1) is updated every four pulses. Repeat update to last address.

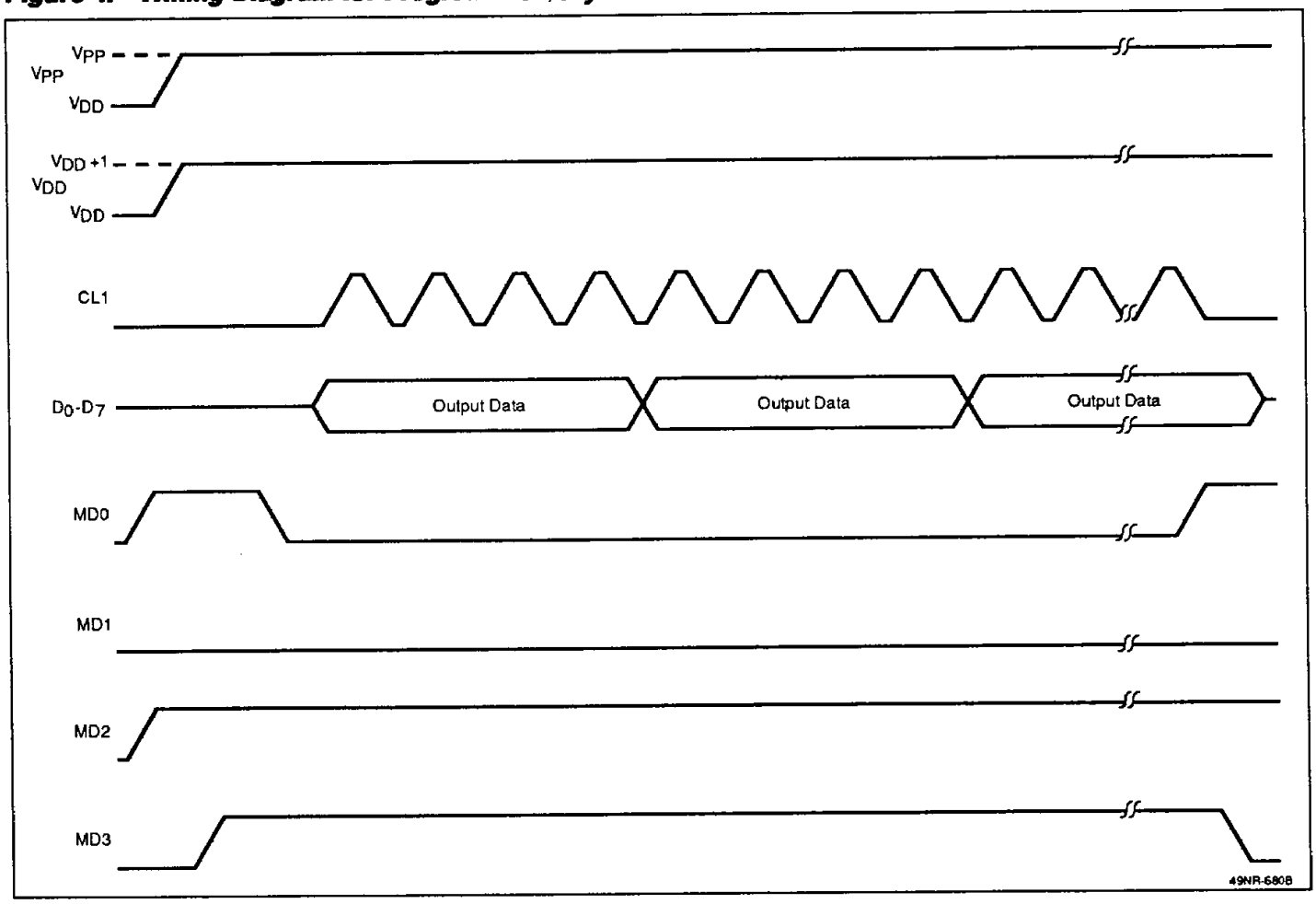
(8) Select the program memory address clear mode (HLHL).

(9) Change the voltage on $V_{DD}$ and $V_{PP}$ to 5 V.

(10) Turn off power.

The timing for steps 2-9 is shown in figure 4.

***Figure 4. Timing Diagram for Program Memory Read***



## ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

$T_A$ = 25°C

| | |
|---|---|
| Operating temperature, $T_{OPT}$ | −10 to +70°C |
| Storage temperature, $T_{STG}$ | −65 to +150°C |
| Power supply voltage, $V_{DD}$ | −0.3 to +7.0 V |
| Input voltage, $V_I$ | |
| Except ports 10, 11 | −0.3 to $V_{DD}$ +0.3 V |
| Ports 10, 11 (Note 1) | −0.3 to $V_{DD}$ +0.3 V |
| (Note 2) | −0.3 to +13 V |
| Output voltage, $V_O$ | |
| Except ports 10, 11 | −0.3 to $V_{DD}$ +0.3 V |
| Ports 10, 11 (Note 1) | −0.3 to $V_{DD}$ +0.3 V |
| (Note 2) | −0.3 to +13 V |
| Output current, high $I_{OH}$ | |
| One port | −5 mA |
| All output ports, total | −15 mA |
| Output current, low $I_{OL}$ | |
| Ports 8, 9 | 30 mA |
| Other ports | 15 mA |
| All ports, total | 100 mA |
| Power dissipation, $P_D$ ($T_A$ = +70°C) | |
| Shrink DIP | 480 mW |
| SOP | 250 mW |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Notes:**

(1) CMOS I/O or N-channel open drain + internal pull-up resistor.

(2) N-channel open drain I/O.

### Capacitance

$T_A$ = 25°C, $V_{DD}$ = $V_{SS}$ = 0 V; f = 1 MHz

Unmeasured pins returned to $V_{SS}$

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input capacitance | $C_I$ | | | 50 | pF | $P0_0$-$P0_1$; $P1_0$-$P1_3$ |
| | | | | 15 | | $CIN_0$-$CIN_3$ |
| Output capacitance | $C_O$ | | | 35 | pF | Ports 8, 9 |
| I/O capacitance | $C_{I/O}$ | | | 35 | pF | Ports 10, 11 |

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## DC Characteristics, Normal Operation; $V_{DD}$ = 4.5 to 6.0 V; $V_{SS}$ = 0 V

$T_A$ = −10 to +70°C

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input high voltage except CL1 | $V_{IH1}$ | 0.7 $V_{DD}$ | | $V_{DD}$ | V | |
| Input high voltage CL1 | $V_{IH2}$ | $V_{DD}$ − 0.5 | | $V_{DD}$ | V | |
| Input high voltage ports 10, 11 (Note 1) | $V_{IH3}$ | 0.7 $V_{DD}$ | | 12 | V | |
| Input low- and high-level voltage RESET | $V_{IHDR}$ | 0.9 $V_{DDDR}$ | | $V_{DDDR}$ + 0.2 | V | Data retention mode |
| Input low voltage except CL1 | $V_{IL1}$ | 0 | | 0.3 $V_{DD}$ | V | |
| Input low voltage CL1 | $V_{IL2}$ | 0 | | 0.5 | V | |
| Input leakage current except CL1 | $I_{LI1}$ | −3 | | 3 | μA | 0 V < $V_I$ < $V_{DD}$ |
| Input leakage current CL1 | $I_{LI2}$ | −10 | | 10 | μA | 0 V < $V_I$ < $V_{DD}$ |
| Input leakage current ports 10, 11 (Note 1) | $I_{LI3}$ | | | 10 | μA | $V_I$ = 12 V |
| Output voltage high $P0_1$, $P0_2$, ports 8-11 | $V_{OH}$ | $V_{DD}$ − 2.0 | | | V | $I_{OH}$ = −1 mA |
| Output voltage low ports 10, 11 | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | | | | 2.0 | V | $I_{OL}$ = 10 mA |
| Output voltage low ports 8, 9 | $V_{OL}$ | | | 2.0 | V | $I_{OL}$ = 15 mA |
| Output leakage current | $I_{LO1}$ | −3 | | 3 | μA | 0 V ≤ $V_O$ < $V_{DD}$ |
| Output leakage current, port 8-11 (Note 1) | $I_{LO2}$ | | | 10 | μA | $V_O$ = 12 V |
| Supply voltage, data retention mode | $V_{DDDR}$ | 2.0 | | 6.0 | V | |
| Supply current, normal operation | $I_{DD1}$ | | 400 | 1400 | μA | μPD75P56: $V_{DD}$ = 5 V ±10%; R = 56Ω ±2% |
| | | | 700 | 2300 | μA | μPD75P66: $V_{DD}$ = 5 V ±10%; $f_{CC}$ = 700 kHz |
| Supply current, HALT mode | $I_{DD2}$ | | 120 | 400 | μA | μPD75P56: $V_{DD}$ = 5 V ±0.5 V; R = 56Ω ±2% |
| | | | 450 | 1500 | μA | μPD75P66: $V_{DD}$ = 5 V ±10%; $f_{CC}$ = 700 kHz |
| Supply current, STOP mode | $I_{DD3}$ | | 0.1 | 10 | μA | $V_{DD}$ = 5 V ±10% |
| | | | 0.1 | 10 | μA | $V_{DD}$ = 5 V ±10% |
| Supply current, data retention mode | $I_{DDDR}$ | | 0.1 | 5 | μA | $V_{DDDR}$ = 2.0 V |

**Notes:**

(1) N-channel, open-drain I/O ports.

## DC Characteristics, Programming mode; $V_{DD}$ = 6.0 V ±0.25 V; $V_{PP}$ = 21 ±0.5 V; $V_{SS}$ = 0 V

$T_A$ = 25°C; (Notes 1 and 2)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input high voltage except CL1 | $V_{IH1}$ | 0.7 $V_{DD}$ | | $V_{DD}$ | V | |
| Input high voltage CL1 | $V_{IH2}$ | $V_{DD}$ – 0.5 | | $V_{DD}$ | V | |
| Input low voltage except CL1 | $V_{IL1}$ | 0 | | 0.3 $V_{DD}$ | V | |
| Input low voltage CL1 | $V_{IL2}$ | 0 | | 0.5 | V | |
| Input leakage current | $I_{LI}$ | | | 10 | μA | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| Output voltage high | $V_{OH}$ | $V_{DD}$ – 2.0 | | | V | $I_{OH}$ = –1 mA |
| Output voltage low | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6 mA |
| $V_{DD}$ supply current | $I_{DD}$ | | | 30 | mA | |
| $V_{PP}$ power current | $I_{PP}$ | | | 30 | mA | MD0 = $V_{IL}$, MD1 = $V_{IH}$ |

**Notes:**

(1) $V_{PP}$, including an overshoot, should not exceed +22 V.

(2) Apply $V_{DD}$ before $V_{PP}$, and cut off after $V_{PP}$.

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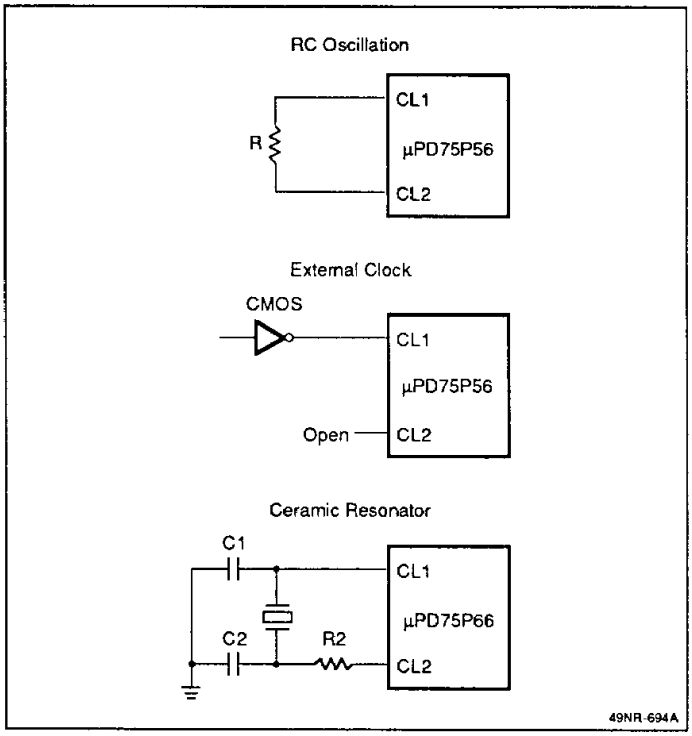
### *Figure 5. Recommended Circuits*



## Comparator

$T_A$ = −10 to +70°C; $V_{DD}$ = 4.5 to 6.0 V, $V_{SS}$ = 0 V

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{CIN}/V_{REF}$ | 0 | | $V_{DD}$ | V | |
| Response time | $T_{COMP}$ | 2 | | 4 | MC(Note 1) | |
| Input voltage resolution | $\Delta V_{CIN}$ | | 10 | 50 | mV | |
| Input leakage current | $I_{CIN}/I_{REF}$ | −3 | | 3 | μA | |
| $V_{REF}$ bias resistance | $R_{REF}$ | | 100 | | kΩ | |
| Comparator circuit current (Note 2) | $I_{DDCMP}$ | | 50 | | μA | $f_{CC}$ = 500 kHz |

**Notes:**

(1) Machine cycle.

(2) Excluding current through bias resistor.

## AC Characteristics, Normal Operation; $V_{DD}$ = 4.5 to 6.0 V; $V_{SS}$ = 0 V

$T_A$ = −10 to +70°C

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| System clock oscillation frequency CL1, CL2 | $f_{CC}$ | 400 | 500 | 600 | kHz | μPD75P56: R = 56 kΩ ±2% |
| | | 290 | | 710 | kHz | μPD75P66: ceramic resonator |
| System clock input frequency, CL1 | $f_C$ | 10 | | 710 | kHz | μPD75P56: 50% duty |
| Oscillation stabilization time | $t_{OS}$ | 20 | | | ms | OS stabilization after minimum of operating voltage reached. (Note 1) |
| System clock rise time, CL1 | $t_{CR}$ | | | 0.2 | μs | |
| System clock fall time, CL1 | $t_{CF}$ | | | 0.2 | μs | |
| System clock pulse width, CL1 | $t_{CH}$ | 0.7 | | 50 | μs | |
| System clock pulse width, CL1 | $t_{CL}$ | 0.7 | | 50 | μs | |
| Event input frequency ($P0_0$) | $f_{P0}$ | 0 | | 710 | kHz | 50% duty |
| $P0_0$ rise time | $t_{POR}$ | | | 0.2 | μs | |
| $P0_0$ fall time | $t_{POF}$ | | | 0.2 | μs | |
| $P0_0$ pulse width, high | $t_{P0H}$ | 0.7 | | | μs | |
| $P0_0$ pulse width, low | $t_{P0L}$ | 0.7 | | | μs | |
| INT0 high time | $t_{I0H}$ | 10 | | | μs | |
| INT0 low time | $t_{I0L}$ | 10 | | | μs | |
| RESET high time | $t_{RSH}$ | 10 | | | μs | |
| RESET low time | $t_{RSL}$ | 10 | | | μs | |
| RESET setup time | $t_{SRS}$ | 0 | | | μs | |
| RESET hold time | $t_{HRS}$ | 0 | | | μs | |

**Notes:**

(1) Hold the RESET signal at a high level until oscillation becomes stable.

## AC Characteristics, Programming Mode; $V_{DD}$ = 6.0 ± 0.25 V; $V_{PP}$ = 21 ±0.5 V, $V_{SS}$ = 0 V

$T_A$ = 25°C

| Parameter | Symbol | Note 1 | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| Address setup time for MD0 ↓ (Note 2) | $t_{AS}$ | $t_{AS}$ | 2 | | | μs | |
| MD1 setup time for MD0 ↓ | $t_{MIS}$ | $t_{OES}$ | 2 | | | μs | |
| Data setup for MD0 ↓ | $t_{DS}$ | $t_{DS}$ | 2 | | | μs | |
| Address hold time for MD0 ↑ (Note 2) | $t_{AH}$ | $t_{AH}$ | 2 | | | μs | |
| Data hold time for MD0↑ | $t_{DH}$ | $t_{DH}$ | 2 | | | μs | |
| MD0 ↑ to data output float delay time | $t_{DF}$ | $t_{DF}$ | 0 | | 200 | ns | |
| $V_{PP}$ setup time for MD3 ↑ | $t_{VPS}$ | $t_{VPS}$ | 2 | | | μs | |
| $V_{DD}$ setup time for MD3 ↑ | $t_{VDS}$ | $t_{VCS}$ | 2 | | | μs | |
| Initial program pulse width | $t_{PW}$ | $t_{PW}$ | 0.95 | 1.0 | 1.05 | ms | |
| Additional program pulse width | $t_{OPW}$ | $t_{OPW}$ | 0.95 | | 21.0 | ms | |
| MD0 setup time for MD1 ↑ | $t_{MOS}$ | $t_{CES}$ | 2 | | | μs | |
| MD0 ↓ to data output delay time | $t_{DV}$ | $t_{DV}$ | | | 1 (Note 3) | μs | MD0 = MD1 = $V_{IL}$ |
| MD1 hold time for MD0 ↑ | $t_{M1H}$ | $t_{OEH}$ | 2 | | | μs | $t_{M1H} + t_{MIR} \geq 50$ μs |
| MD1 recovery time for MD0 ↓ | $t_{M1R}$ | $t_{OR}$ | 2 | | | μs | |
| Program counter reset time | $t_{PCR}$ | | 10 | | | μs | |
| CL1 input low- and high-level widths | $t_{XH}$, $t_{XL}$ | | 0.7 | | | μs | |
| CL1 input frequency | $f_X$ | | | | 710 | kHz | |
| Initial mode set time | $t_I$ | | 2 | | | μs | |
| MD3 setup time for MD1 ↑ | $t_{M3S}$ | | 2 | | | μs | |
| MD3 hold time for MD1 ↓ | $t_{M3H}$ | | 2 | | | μs | |
| MD3 setup time for MD0 ↓ | $t_{M3SR}$ | | 2 | | | μs | During program memory read |
| Address to data output delay time (Note 2) | $t_{DAD}$ | $t_{ACC}$ | 2 | | | μs | |
| Address to data output hold time (Note 2) | $t_{HAD}$ | $t_{OH}$ | 0 | | 300 | ns | |
| MD3 hold time for MD0 ↑ | $t_{M3HR}$ | | 2 | | | μs | |
| MD3 ↓ to data output float delay time | $t_{DFR}$ | | 2 | | | μs | |

**Notes:**

(1) Symbol of the corresponding μPD27C256.

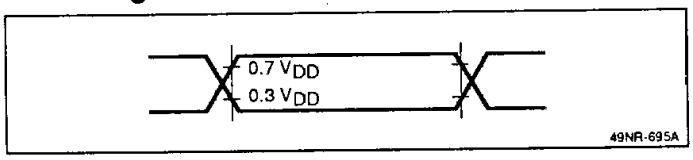
(2) "1" is added to the internal address signal at the rising edge of the third CL1 input. The signal is not input to the pin.

(3) During CMOS output.

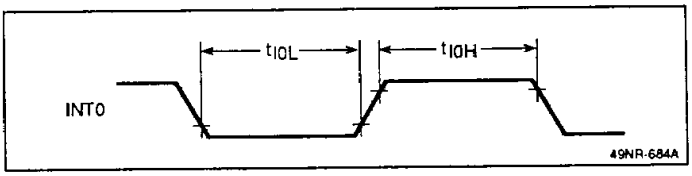
3

## Timing Waveforms

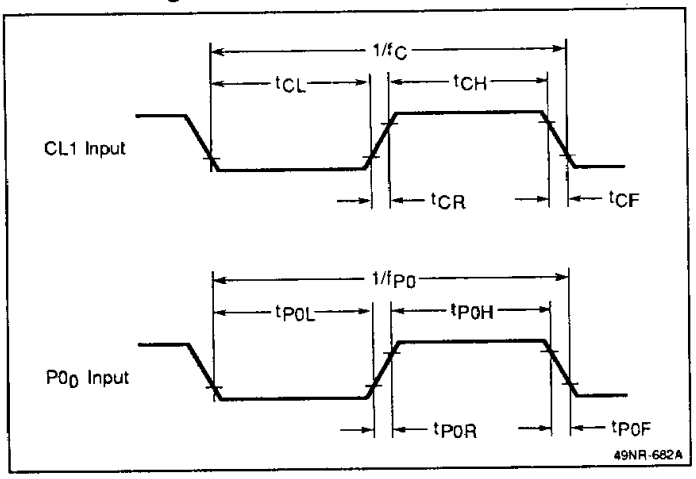
### AC Timing Measurement Points



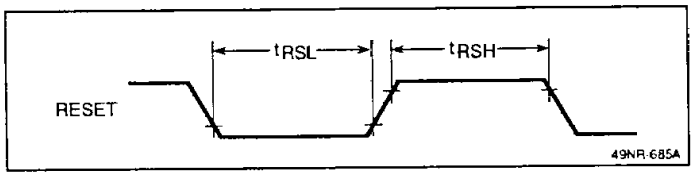

### Test Input Timing




### Clock Timing

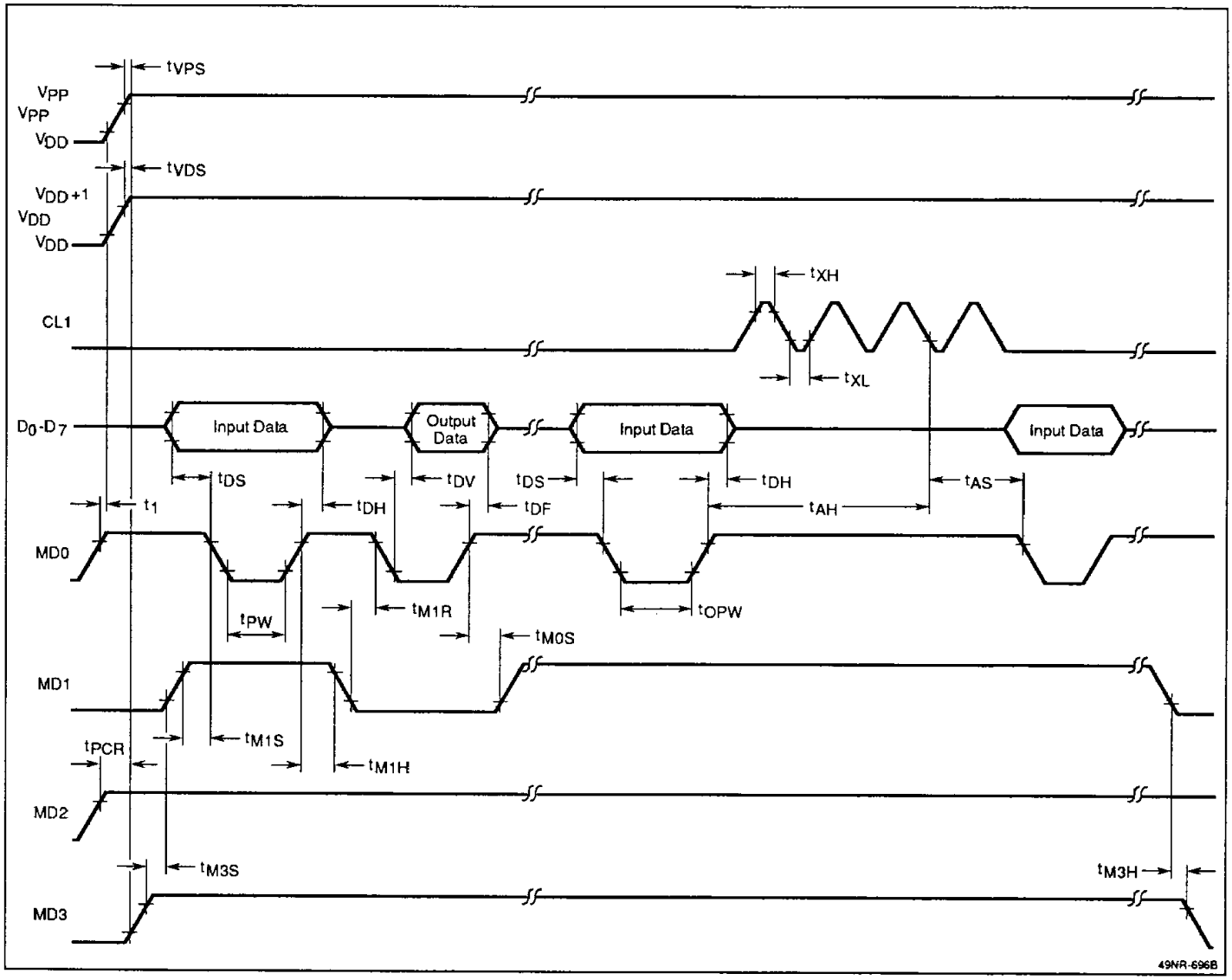



### RESET Timing



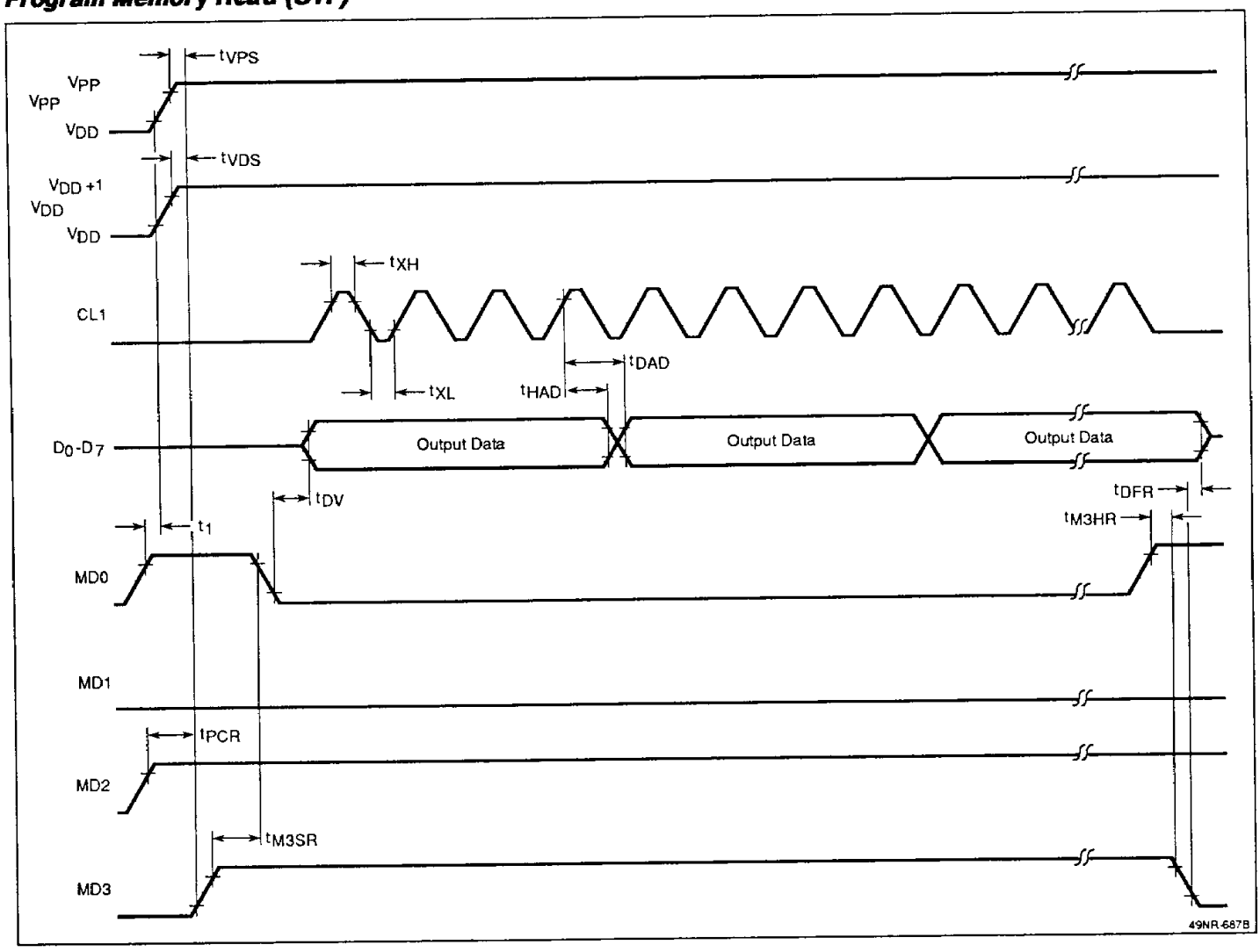
## Timing Waveforms (cont)

### *Program Memory Write (OTP)*



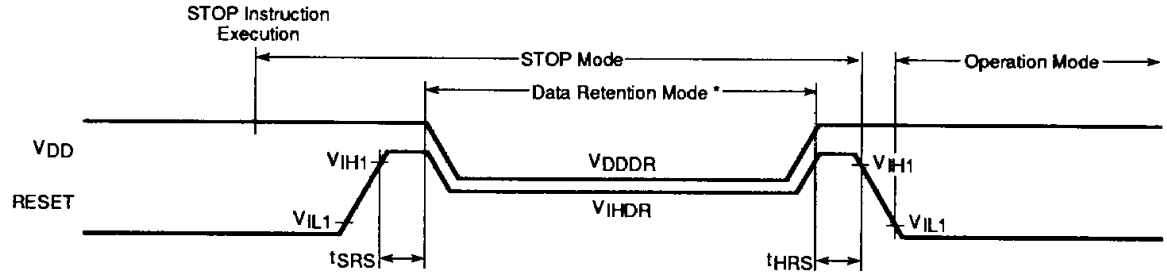
## Timing Waveforms (cont)

### *Program Memory Read (OTP)*



## Timing Waveforms (cont)

### *Data Retention Timing μPD75P56*




* In the data retention mode, set all inputs to a value smaller than $V_{DDDR}$.

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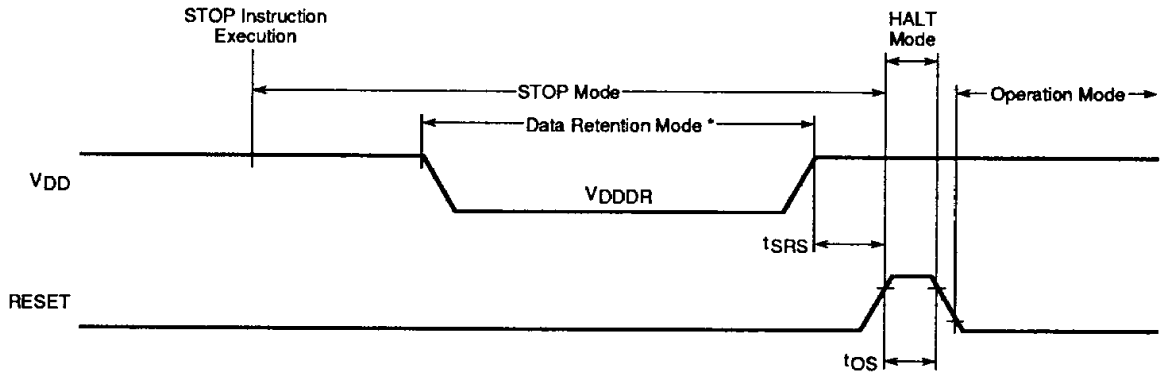
### *Data Retention Timing μPD75P66*




* In the data retention mode, set all inputs to a value smaller than $V_{DDDR}$.

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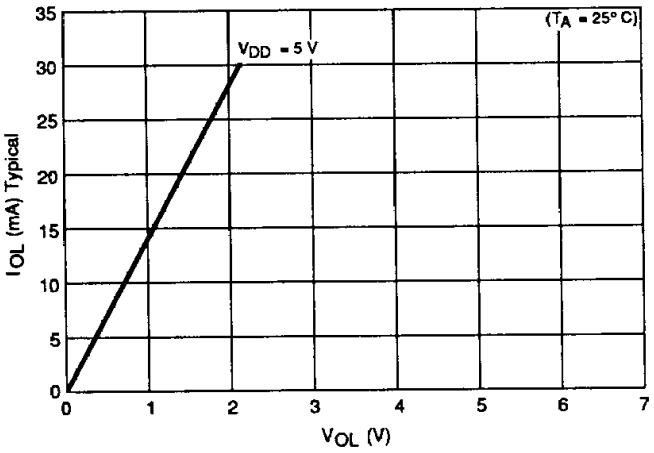
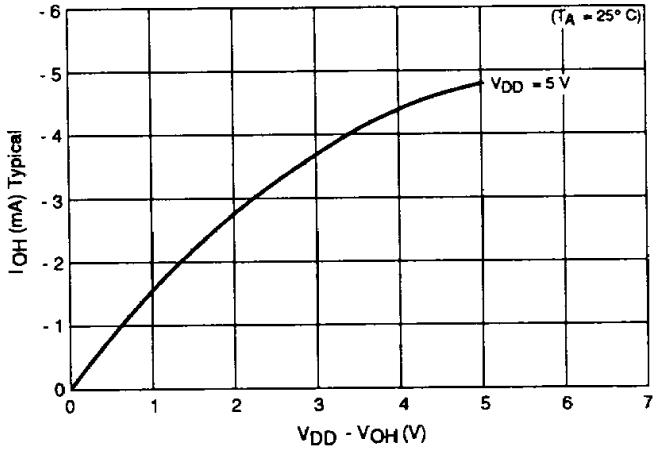
## Operating Characteristics

$I_{OL}$ vs $V_{OL}$ (Ports 8, 9)



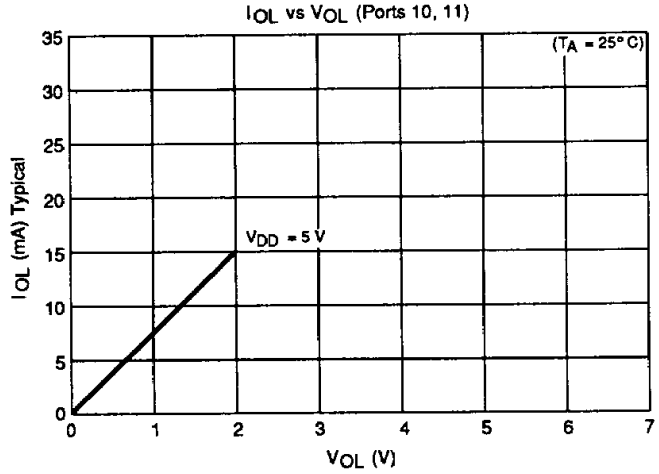

* The absolute maximum rating is 30 mA per pin.

$I_{OH}$ vs $V_{OH}$



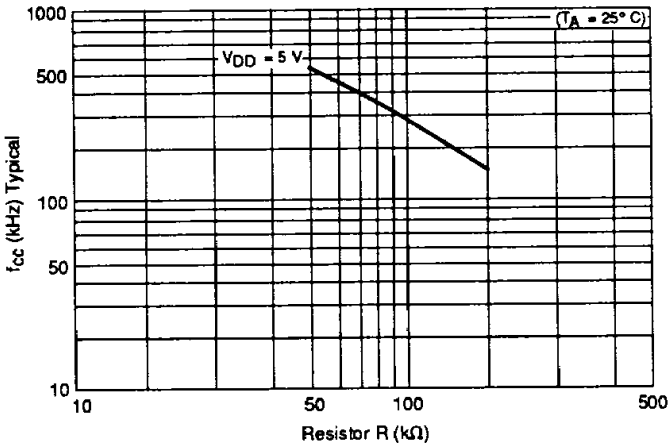

* The absolute maximum rating is -5 mA per pin.

$I_{OL}$ vs $V_{OL}$ (Ports 10, 11)




* The absolute maximum rating is 15 mA per pin.

$f_{CC}$ vs R




* This curve shows a device characteristic example and does not guarantee the ratings.

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