Motherboard Clock Generator for 440BX Type with 133MHz FSB

FEATURES

- Generates all clock frequencies for PentiumIII systems with INTEL 440BX or VIA Apollo Pro133 or Promedia chip sets, requiring multiple CPU clocks and high speed SDRAM buffers.
- Support 2 CPU clocks, 6PCI and 13 high-speed SDRAM buffers for 3-DIMM applications.
- One 24MHz clock and one 48MHz clock.
- One 2.5V IOAPIC clock.
- Two14.318MHz reference clocks.
- Power management control to stop CPU, PCI, SDRAM and IOAPIC clocks.
- Support 2-wire I2C serial bus interface with built-in Vendor ID, Device ID and Revision ID.
- Single byte micro-step linear Frequency Programming via I2C with Glitch free smooth switching.
- Spread Spectrum ±0.25% center.
- 50% duty cycle with low jitter.
- Available in 300 mil 48 pin SSOP.

PIN CONFIGURATION

PLL202-01

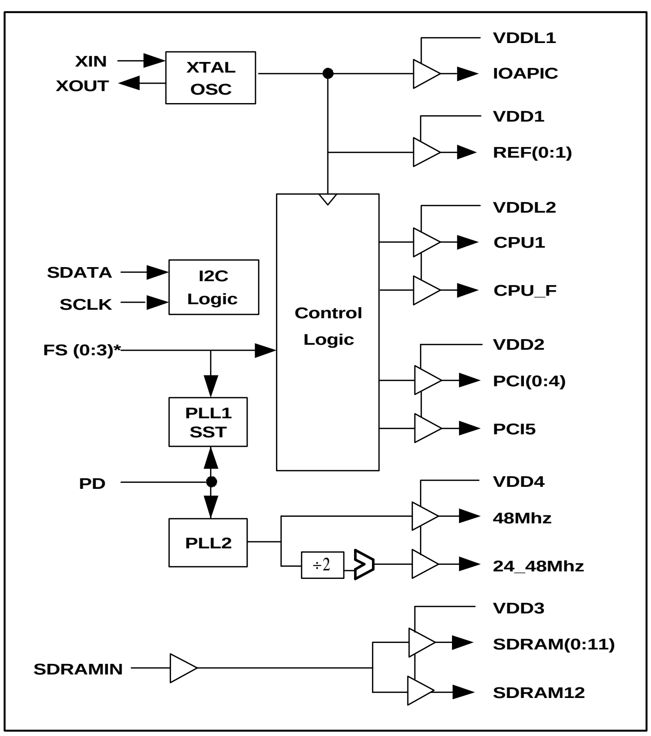
VDD1	1	48	VDDL1
REF0//PCI_STOP#^	2	47	IOAPIC
GND	3	46	REF1/FS2*^
XIN	4	45	GND
XOUT	5	44	CPU_F
VDD2	6	43	CPU_1
PCI_F/MODE*^	7	42	VDDL2
PCI0/FS3*^v	8	41	CPU_STOP#*^
GND	9	40	SDRAM_F
PCI1	10	39	GND
PCI2	11	38	SDRAM0
PCI3	12	37	SDRAM1
PCI4	13	36	VDD3
VDD2	14	35	SDRAM2
SDRAMIN	15	34	SDRAM3
GND	16	33	GND
SDRAM11	17	32	SDRAM4
SDRAM10	18	31	SDRAM5
VDD3	19	30	VDD3
SDRAM9	20	29	SDRAM6
SDRAM8	21	28	SDRAM7
GND	22	27	VDD4
SDATA	23	26	48MHz/FS0*^
SCLK	24	25	24MHz/FS1*^

Note: **^**: Pull up, **#**: Active Low
*****: Bi-directional latched at power-up

I/O MODE CONFIGURATION

MODE (Pin 7)	PIN 2
1 (OUTPUT)	REF0
0 (INPUT)	PCI_STOP

BLOCK DIAGRAM



POWER GROUP

- VDD1: REF, XIN, XOUT, PLL CORE
- VDD2: PCI_F, PCI(0:4)
- VDD3: SDRAM_F, SDRAM(0:11)
- VDD4: 48MHz, 24MHz, SDATA, SCLK
- VDDL1: IOAPIC VDDL2: CPU_F, CPU1

KEY SPECIFICATIONS

- CPU Cycle to Cycle jitter: 250ps.
- PCI Cycle to Cycle jitter: 250ps.
- SDRAM to SDRAM skew: 500ps.
- PCI to PCI skew: 500ps.
- CPU to CPU skew 250ps
- CPU to PCI skew: 1 ~ 4ns, typical 2ns
- SDRAMIN to SDRAM skew: 3 ~ 4ns, typical 3.5ns.

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PIN DESCRIPTIONS

Name	Number	Type	Description
VDD1	1	P	Power supply for REF0, REF1, and crystal oscillator.
VDD2	6,14	P	Power supply for PCI_F, PCI(0:4).
VDD3	19,30,36	P	Power supply for SDRAM(0:11), SDRAM_F.
VDD4	27	P	Power supply for 24MHz and 48MHz.
VDDL1	48	P	Power supply for IOAPIC (2.5V).
VDDL2	42	P	Power supply for CPU_F and CPU1 (2.5V).
GND	3,9,16,22, 33,39,45	P	Ground.
XIN	4	I	14.318MHz crystal input to be connected to one end of the crystal.
XOUT	5	O	14.318MHz crystal output.
PCI0/F3* REF1/F2* 24MHz/F1* 48MHz/F0*	8,46,25,26	B	At power up, these pins are input pins and will determine the CPU clock frequency. After input sampling, these pins will generate output clocks. FS0, FS1 and FS2 have internal pull up (high by default) while FS3 has internal pull down (low by default).
PCI_F, PCI(0:4)	7,8,10,11,12, 13	O	PCI clocks with frequencies defined by Frequency Table. These pins except PCI_F will be LOW when PCI_STOP is LOW.
CPU_F, CPU1	44,43	O	CPU clocks with frequencies defined by Frequency Table. These pins are LOW when CPU_STOP is LOW except CPU_F.
SDRAM (0:11), SDRAM_F	38,37,35,34,32, 31,29,28,21,20, 18,17,40	O	Buffer output from SDRAMIN pin. These pins are LOW when CPU_STOP is LOW except SDRAM_F is free running output.
SDATA	23	B	Serial data input for serial interface port.
SCLK	24	I	
REF0//PCI_STOP	2	B	Multiplexed pin controlled by MODE signal. PCI_STOP will stop PCI clock except PCI_F when LOW.
CPU_STOP	41	I	CPU_STOP input will stop CPU1, IOAPIC and SDRAM(0:11) when LOW.
PCI_F/MODE	7	B	At power-on, MODE function will be activated. When MODE is Low, Pin 2 is input for PCI_STOP. When high, Pin2 is output for REF0. After input data latched, this pin will generate free running PCI bus clock.
48MHz	26	B	48MHz output for USB after input data latched during power-on.
24MHz	25	B	24MHz output for SUPER I/O after input data latched during power-on.
REF1/FS2	46	B	Buffered reference clock output after input data latched during power-on.
SDRAMIN	15	I	Buffer input pin: The signal provided to this input pin is buffered to 13 SDRAM outputs.
IOAPIC	47	O	2.5V Buffered reference clock. This pin will be LOW when CPU_STOP is low.

POWER MANAGEMENT

CPU_STOP	PCI_SOTP	CPU1	PCI	PCI_F,CPU_F,SDRAM_F	SDRAM	IOAPIC	XTAL,VCO
1	1	Running	Running	Running	Running	Running	Running
0	1	Low	Running	Running	Low	Low	Running
1	0	Running	Low	Running	Running	Running	Running

FREQUENCY (MHz) SELECTION TABLE

I2C Byte0 Bit2	FS3	FS2	FS1	FS0	CPU	PCI
0 (default)	0	0	0	0	80	40.0
	0	0	0	1	75	37.5
	0	0	1	0	83.3	41.7
	0	0	1	1	66.8	33.4
	0	1	0	0	103	34.3
	0	1	0	1	112	37.3
	0	1	1	0	68	34.0
	0	1	1	1	100.2	33.4
	1	0	0	0	120	40.0
	1	0	0	1	115	38.3
	1	0	1	0	110	36.3
	1	0	1	1	105	35.0
	1	1	0	0	140	35.0
	1	1	0	1	150	37.5
	1	1	1	0	124	31.0
	1	1	1	1	133.3	33.3
1	0	0	0	0	135	33.8
	0	0	0	1	130	32.5
	0	0	1	0	126	31.5
	0	0	1	1	118	39.3
	0	1	0	0	116	38.4
	0	1	0	1	95	31.7
	0	1	1	0	90	30.0
	0	1	1	1	85	28.3
	1	0	0	0	166	41.5
	1	0	0	1	160	40.0
	1	0	1	0	155	38.8
	1	0	1	1	148	37.0
	1	1	0	0	146	36.5
	1	1	0	1	144	36.0
	1	1	1	0	142	35.5
	1	1	1	1	138	34.5

I2C BUS CONFIGURATION SETTING

Address Assignment	A6 A5 A4 A3 A2 A1 A0 R/W 1 1 0 1 0 0 1 _
Slave Receiver/Transmitter	Provides both slave write and readback functionality
Data Transfer Rate	Standard mode at 100kbits/s
Serial Bits Reading	The serial bits will be read or sent by the clock driver in the following order Byte 0 Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N Bits 7, 6, 5, 4, 3, 2, 1, 0
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in **Write Mode:** the **Command Byte** and **Byte Count Byte must be sent by the master** but ignored by the slave, in **Read Mode:** the **Byte Count Byte** will be **read by the master** then all other **Data Byte**. **Byte Count Byte** default at power-up is = (0x09).

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	8	0	FS3 (see Frequency selection Table)
Bit 6	46	0	FS2 (see Frequency selection Table)
Bit 5	25	0	FS1 (see Frequency selection Table)
Bit 4	26	0	FS0 (see Frequency selection Table)
Bit 3	-	0	Frequency selection control bit 1=Via I2C, 0=Via External jumper
Bit 2	-	0	I2C Selection (see Frequency selection Table)
Bit 1	-	0	0=Normal 1=Spread Spectrum enable, $\pm$0.25% Center Spread
Bit 0	-	0	0=Normal 1=Tristate Mode for all outputs

2. BYTE 1: CPU Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	46	X	Inverted Power on latched FS2 value (Read only)
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	40	1	SDRAM_F (Active/Inactive)
Bit 2	-	1	Reserved
Bit 1	43	1	CPU1 (Active/Inactive)
Bit 0	44	1	CPU_F (Active/Inactive)

3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	7	1	PCI_F (Active/Inactive)
Bit 5	-	1	Reserved
Bit 4	13	1	PCI4 (Active/Inactive)
Bit 3	12	1	PCI3 (Active/Inactive)
Bit 2	11	1	PCI2 (Active/Inactive)
Bit 1	10	1	PCI1 (Active/Inactive)
Bit 0	8	1	PCI0 (Active/Inactive)

4. BYTE 3: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	26	X	Inverted Power on latched FS0 value (Read only)
Bit 5	26	1	48MHz
Bit 4	25	1	24MHz
Bit 3	-	1	Reserved
Bit 2	21,20,18,17	1	SDRAM (8:11) (Active/Inactive)
Bit 1	32,31,29,28	1	SDRAM (4:7) (Active/Inactive)
Bit 0	38,37,35,34	1	SDRAM (0:3) (Active/Inactive)

5. BYTE 4: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	25	X	Inverted Power on latched FS1 value (Read only)
Bit 2	-	1	Reserved
Bit 1	8	X	Inverted Power on latched FS3 value (Read only)
Bit 0	-	1	Reserved

6. BYTE 5: Peripheral Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	47	1	IOAPIC (Active/Inactive)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	46	1	REF1 (Active/Inactive)
Bit 0	2	1	REF0 (Active/Inactive)

7. BYTE 6: Revision ID and Vendor ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Revision ID Bit 3*
Bit 6	-	0	Revision ID Bit 2*
Bit 5	-	0	Revision ID Bit 1*
Bit 4	-	0	Revision ID Bit 0*
Bit 3	-	0	Vendor ID Bit 3*
Bit 2	-	0	Vendor ID Bit 2*
Bit 1	-	1	Vendor ID Bit 1*
Bit 0	-	1	Vendor ID Bit 0*

Note: *: Default value at power-up

8. BYTE 7: Linear Programming (M) Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Linear programming sign bit (0 is +, 1 is −)
Bit 6	-	0	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0	Linear programming magnitude bit 5
Bit 4	-	0	Linear programming magnitude bit 4
Bit 3	-	0	Linear programming magnitude bit 3
Bit 2	-	0	Linear programming magnitude bit 2
Bit 1	-	0	Linear programming magnitude bit 1
Bit 0	-	0	Linear programming magnitude bit 0 (LSB)

9. BYTE 8: Device ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Reserved
Bit 6	-	0	Device ID Bit 6*
Bit 5	-	0	Device ID Bit 5*
Bit 4	-	0	Device ID Bit 4*
Bit 3	-	0	Device ID Bit 3*
Bit 2	-	0	Device ID Bit 2*
Bit 1	-	0	Device ID Bit 1*
Bit 0	-	0	Device ID Bit 0*

Note: ***:** Default value at power-up

PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL202-01 device incorporates SMART-BYTE technology with a single byte programming via I2C to better optimize clock jitter and spread spectrum performance. Detail of PLL202-01's dual mode frequency programming method is described below:

1. **ROM-table Frequency Programming:**

   The pre-defined 32 frequencies found in Frequency table can be accessed either through 5 external jumpers or by setting internal I2C register in BYTE0.

2. **Micro-step Linear Frequency Programming:**

   CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency change. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha\ (=0.22) * M$$

Where:
1. M is magnitude factor defined in I2C Byte 7.bit(0:6)
2. $\pm$ (sign bit) of M is defined in I2C Byte7.bit 7
3. α is a constant
   $\alpha = 0.22$

FREQUENCY PROGRAMMING EXAMPLE:

1. **Procedures to program target CPU frequency to 139.0 Mhz:**

   A. Locate the closest CPU frequency from Frequency-ROM table: 135
   B. $\alpha = 0.22$
   C. Solve M (Linear Magnitude factor) in integer:

$$\begin{aligned} M &= (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha \\ &= (139 - 135) / 0.22 \\ &= 18 \end{aligned}$$

   D. Program I2C register:

Setting of I2C.BYTE0

7	6	5	4	3	2	1	0
0	0	0	0	**1**	1	0	0
FS3	FS2	FS1	FS0	CTR	FS4		

Setting of M = +18 in I2C.BYTE7

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
Sign	M6	M5	M4	M3	M2	M1	M0

F_{CPU} = 135 + (0.22) * 18 = 138.96 (% of frequency increased = 2.9 %)
F_{PCI} = 33.8 * (1+2.9%) = 34.8

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC/DC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	uA
Input Low Current	I_{IL1}	VIN = 0V; Inputs with no pull-up resistors	-5			uA
Input Low Current	I_{IL2}	VIN = 0V; Inputs with pull-up resistors	-200			uA
Pull-up resistor	R_{Pu}	Pin 2,7,25,26,41,46		240		Kohm
Pull-down resistor	R_{Pd}	Pin 8				
Input frequency	F_I	V_{DD} = 3.3V	12	14.318	16	Mhz
Input Capacitance	C_{IN}	Logic Inputs			5	PF
	C_{INX}	XIN & XOUT pins	27	36	45	PF

2. Output Buffer Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU_F, CPU1	Measured @ 0.4V ~ 2.0V, C_L=10-20pf, 2.5V±5%	1		4	V/ns
		REF, 48MHz, 24MHz	Measured @ 0.4V ~ 2.4V, C_L=10-20pf	1		4	
		SDRAM, SDRAM_F, PCI_F,PCI	Measured @ 0.4V ~ 2.4V, C_L=10-30pf	1		4	
		IOAPIC	Measured @ 0.4V ~ 2.0V, C_L=10-30pf, 2.5V±5%				
Output Fall time	T_{OF}	CPU_F, CPU1	Measured @ 2.0 ~ 0.4V, C_L=10-20pf, 2.5V±5%	1		4	V/ns
		REF, 48MHz, 24MHz	Measured @ 2.4V ~ 0.4V, C_L=10-20pf	1		4	
		SDRAM, SDRAM_F, PCI_F, PCI	Measured @ 2.4V ~ 0.4V, C_L=10-30pf	1		4	
		IOAPIC	Measured @ 2.0V ~ 0.4V, C_L=10-30pf, 2.5V±5%				
Duty Cycle	D_T	CPU_F,CPU1,SDRAM, PCI_F,PCI, 48MHz, 24MHz	Measured @ 1.5V C_L=20pf	45	50	55	%
		IOAPIC,REF	Measured @ 1.5V, C_L=20~30pf	40		60	
Clock Skew	T_{SKEW}	CPU to CPU	Measured @ 1.5V, equal loads			250	ps
		SDRAM to SDRAM				250	
		PCI to PCI				500	
		CPU to SDRAM				250	
		SDRAMIN to SDRAM		3		5	ns
		CPU to PCI		1		4	
Output Impedance	Z_0	CPU_F,CPU1	V_{DD}=3.3V(2.5V)±5%		30		Ohm
		REF0,48MHz,24MHz, PCI_F,PCI	V_{DD}=3.3V±5%		25		
		SDRAM,SDRAM_F, REF1			20		
		IOAPIC	V_{DD}=3.3V(2.5V)±5%		20		

2. Output Buffer Electrical Specifications, continued

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Current	I_{OH}	SDRAM,SDRAM_F	V_{OH} = 1.5V	70	90	120	mA
		PCI_F,PCI		70	90	120	
		REF		40	50	65	
		48MHz,24MHz		40	50	65	
		CPU_F,CPU1	V_{OH} = 1.25V (V_{DD} = 2.5V±5%)	45	60	80	
		IOAPIC		60	80	105	
Output Low Current	I_{OL}	SDRAM,SDRAM_F	V_{OL} = 1.5V	70	90	120	mA
		PCI_F,PCI		70	90	120	
		REF		40	50	65	
		48MHz,24MHz		40	50	65	
		CPU_F,CPU1	V_{OH} = 1.25V (V_{DD} = 2.5V±5%)	45	60	80	
		IOAPIC		60	80	105	
Jitter, One Sigma	J_{sigma}	CPU	Measured @ 1.25V			150	ps
		IOAPIC				500	
		PCI	Measured @ 1.5V			150	
		REF,48MHz,24MHz				500	
Jitter, Absolute	J_{Abs}	CPU	Measured @ 1.25V	-0.25		0.25	ns
		IOAPIC		-1		1	
		PCI	Measured @ 1.5V	-0.5		0.5	
		REF,48MHz,24MHz		-1		1	
Jitter (cycle to cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		PCI	Measured @ 1.5V			500	

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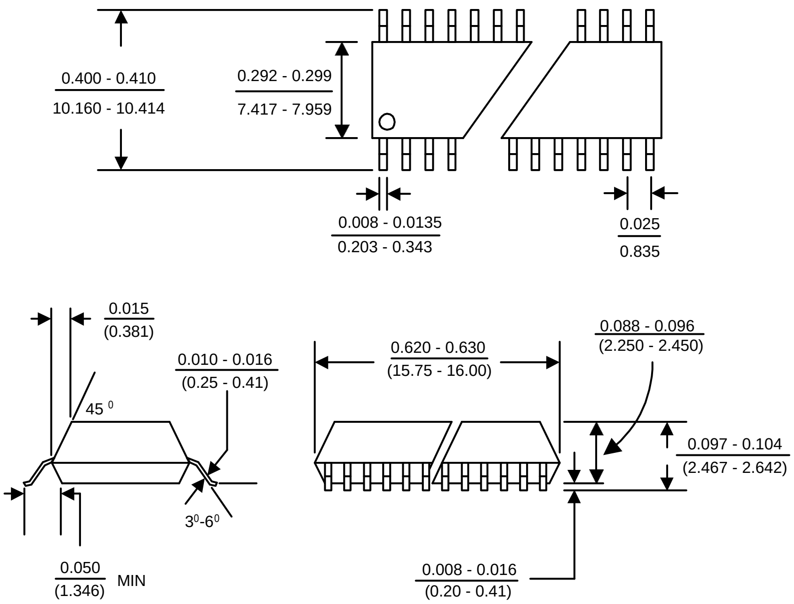
PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range

PLL202-01 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP

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