ZR36055

PRELMINARY

Motion JPEG Controller

Features

- Implements the control logic for a robust, low-cost motion JPEG compression and expansion system for video capture boards, based on the ZR36050 JPEG Image Compression Processor
- Two speed grades available: 21 MHz, 29.5 MHz
- Performs real-time JPEG compression or expansion of NTSC and PAL square pixel or CCIR video formats in the following resolutions:
  - Full resolution
  - Half resolution with vertical decimation
  - Half resolution with horizontal decimation
  - Quarter resolution
- User defined active video area, enables compression of a cropped region of the input video
- In expansion, supports internal or external video synchronization
- Supports fast still-image compression and expansion for video editing
- Implements one-pass compression with the ZR36050's exclusive bit rate control feature. Automatically keeps the compressed data rate virtually constant
- In compression, interfaces directly to the digital video and sync outputs of a YUV 4:2:2 digital video format decoder (e.g., the Philips SAA7110 for square pixel, the SAA7111 for CCIR format or any other compatible decoder or digital video source)
- In expansion, outputs the same YUV 4:2:2 video format, and interfaces directly to the digital video and sync input of common video overlay controllers, such as the Trident PCView+, MCT MVM121/MVP131, AuraVision VxP500/501, and common digital video encoders such as the Fuji MD0207, Philips SAA7188 and SAA7199, and others
- I/O-mapped ISA bus interface to strip buffer, code buffer and control registers
- Software support includes a Windows DLL and sample Video for Windows Capture and Codec drivers
- 160-pin PQFP package
- Low-power CMOS, 5V

Applications

- Full-motion video capture and playback on personal computers
- Video conferencing over local area and wide area networks
- Security systems
- Digital VCR
- Low-cost video editing systems

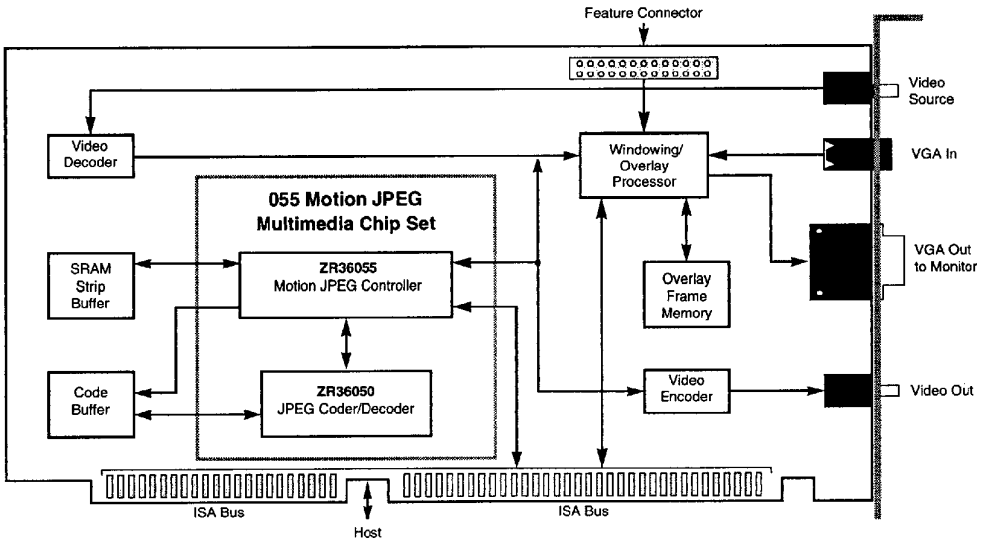

Figure 1. Typical PC Video System Block Diagram

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INTRODUCTION

The ZR36055 Motion JPEG Controller integrates the control logic for the ZR36050 JPEG Processor, needed to implement a low-cost, low-parts-count motion JPEG capture and playback subsystem on the PC. A ZR36050 and ZR36055, together with the associated memory for strip buffers and code buffers, is known as the "055 subsystem." This subsystem adds a highly effective compression capability to a video capture board, by significantly increasing the image resolution and frame rate that can be supported in a typical PC system. A system based on the 055 Motion JPEG Multimedia Chip Set (ZR36050+ZR36055; for brevity, the "055 Chip Set") supports the YUV 4:2:2 digital video data format of the Philips SAA7110, SAA7111 or compatible live video decoders. In addition, for compatibility with a previous Zoran product, the 045 Motion JPEG Multimedia Chip Set, it supports expansion of motion JPEG images compressed using YUV 4:1:1 subsampling. An 055 Chip Set-based system performs real-time JPEG compression and expansion at up to the full resolution of PAL and NTSC digital video standards, for both CCIR and square pixel formats. In addition, the 055 Chip Set supports high speed still image compression and expansion in compliance with the JPEG baseline standard.

The 055 Chip Set makes use of a unique and patented feature built into the ZR36050 JPEG Image Compression Processor: Zoran Bit Rate Control. With this feature, a nearly constant bit rate is maintained along the video sequence with only small variations around the desired bit rate. In the worst case situation of a scene cut, i.e., when there is an abrupt change in the statistics of the sequence, the 055 Chip Set indicates that such an event occurred, enabling the control software to drop a field if necessary, and conceal the anomaly by duplicating the previous field. Only one field must be duplicated, thus ensuring continuity of the video.

There are two versions of the ZR36055: the ZR36055-21 and the ZR36055-29.5. The ZR36055-21 with ZR36050-21 comprise the "Low-End" 055 Chip Set or, with associated memory, "Low-End" 055 subsystem, which supports half resolution with horizontal decimation and quarter resolution. The ZR36055-29.5 with ZR36050-29.5 comprise the "High-End" 055 Chip Set or, with associated memory, "High-End" 055 subsystem, which supports all the resolutions (See Table 2).

Note that the -21 designation of the ZR36055-21 only signifies that it is intended to be used in conjunction with the ZR36050-21; it does not indicate the master clock frequency rating of the ZR36055. The ZR36055 in both the Low End and the High End chip sets operates with the same master clock frequency, of twice the video pixel frequency. The difference between them is that the ZR36055-21 is rated to operate only in the SLOW mode (see the description of Command Register 0 on page 10), whereas the ZR36055-29.5 is rated to operate in both the FAST and SLOW modes. Only the SLOW mode is suitable for use with the ZR36050-21.

A block diagram of a typical multimedia add-in board for video display, capture and playback employing the 055 Chip Set is shown in Figure 1. Analog video (PAL or NTSC) from a video source (camcorder, VCR or any other video source) is input to a video decoder. The digital video from the video decoder is transferred simultaneously to the windowing/overlay device and the video encoder for display, and to the ZR36055 for compression. The ZR36055 then performs, when required, horizontal decimation followed by raster to block conversion. Next, YUV blocks are routed to the ZR36050 where each 8x8 sample block is compressed according to the JPEG baseline algorithm, yielding the coded image. The compressed JPEG data is subsequently stored in the code buffer, from where it is read by the ZR36055 and transferred across the ISA bus to the system memory and from there to the hard disk. Repetition at 50/60 fields (25/30 frames) per second yields full motion real time video capture capability. The parameters needed for compression of the next field are automatically updated by the ZR36050 after the completion of the current field, thus controlling the bit rate of the compressed video sequence.

For motion video playback, the inverse operation is performed, with the expanded image being routed to the windowing/overlay processor for display on the PC monitor. Simultaneously, the expanded image may be routed to a video encoder for recording by a VCR or for display on a video monitor.

For still image compression, the image is input to the ZR36055 through the ISA bus in block order: the control software must perform color space conversion, if needed, and the raster to block operation. The ZR36055 transfers these blocks to the ZR36050 which performs the JPEG baseline compression, yielding the coded image. The compressed JPEG bit stream is stored in the code buffer, from where it is transferred by the host software across the ISA bus to the system memory. For still image expansion, the inverse operation is performed by the 055 Chip Set and the control software.

FUNCTIONAL OVERVIEW

The ZR36055 Motion JPEG controller performs the following functions:

- Interfacing to a YUV 4:2:2 format digital video decoder (e.g., Philips SAA7110 or SAA7111).
- Interfacing to a standard overlay processor (e.g., devices supplied by Trident, MCT, Auravision, or compatible), and standard video encoder (e.g., Fuji MD0207, Philips SAA7199 or SAA7188).
- Interfacing to a standard ISA bus
- Interfacing to an external VRAM (the "code buffer," for compressed data)
- Interfacing to an external SRAM (the "strip buffer," for pixel data)
- Control of the ZR36050 JPEG Image Compression Processor
- Raster to block and block to raster conversions of YUV 4:2:2 digital video.
- Optional video sync generation, in expansion, for display devices (e.g., video encoders and overlay processors)
- Raster to raster conversion, enabling support for fast still compression and expansion (with appropriate software support)
- Horizontal decimation, with optional filtering, of the input image
- Horizontal interpolation, with optional filtering, of the reconstructed image
- Vertical interpolation of the reconstructed image, by field duplication
- Conversion of YUV 4:1:1 format reconstructed pictures into YUV 4:2:2 format digital video, in order to support YUV 4:1:1 playback (for compatibility with a previous Zoran product, the 045 Chip Set)

The ZR36055 supports (i.e., accepts in compression and outputs in expansion) digital video in CCIR 601 or square pixel formats, following either NTSC or PAL video standard. The parameters of these formats are summarized in the following table:

Table 1: Formats Supported by the ZR36055

Pixel format	Video standard	Pixel Rate	Image size	Frame rate
CCIR	PAL	13.5 MHz	720x576	25 fr/sec.
	NTSC	13.5 MHz	720x480	30 fr/sec.
Square Pixel	PAL	14.75 MHz	768x576	25 fr/sec.
	NTSC	12.2727 MHz	640x480	30 fr/sec.

For each of the above mentioned formats, the 055 Chip Set can be configured to compress or expand the following resolutions:

Table 2: Resolutions Supported by the ZR36055

	CCIR601		Square Pixel	
Resolution	**PAL**	**NTSC**	**PAL**	**NTSC**
Full	720 x 576	720 x 480	768 x 576	640 x 480
Half Horizontal	360 x 576	360 x 480	384 x 576	320x 480
Half Vertical	720 x 288	720 x 240	768 x 288	640 x 240
Quarter	360 x 288	360 x 240	384 x 288	320 x 240

When performing horizontal decimation or interpolation, in the Half Horizontal and Quarter resolution modes, the ZR36055 supports optional filtering.

Figure 2 depicts the ZR36055 functional block diagram.

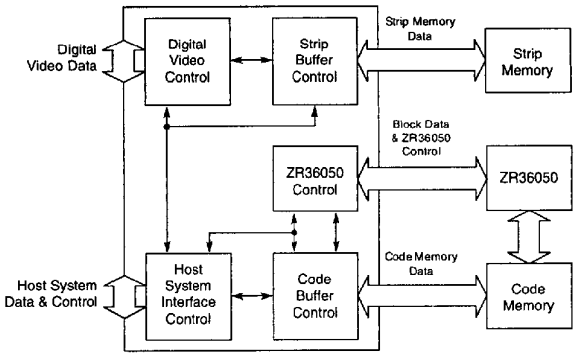


Figure 2. Conceptual Block Diagram of ZR36055 Including Major External Components of an 055 Subsystem

The ZR36055 can be conceptually partitioned into five major functional blocks:

- Digital Video Control
- Strip Buffer Control
- ZR36050 Control
- Code Buffer Memory Control
- Host System Interface Control

Digital Video Control

The Digital Video Control block is responsible for controlling the flow of data on the Digital Video interface, and generating timing and control signals for other modules based on the incoming clocks and syncs from the video decoder. In compression, it detects the incoming vertical and horizontal sync signals and provides the appropriate timing information to the Strip Buffer Control module. In expansion, when the optional internal sync mode is used, it acts as a vertical and horizontal sync signal generator, whereas in external sync mode, the ZR36055 outputs the digital video in synchronization with the sync signals of an external source. Other tasks performed by the module are conversion to and from the time multiplexed chrominance data format, and horizontal decimation and interpolation of the video, with optional filtering.

Strip Buffer Control

The Strip Buffer Control block manages the strip buffer SRAM memory, which stores two strips (one strip = 8 lines) of the image for the raster to block conversion. By suitably addressing the strip memory, the strip buffer memory control performs the conversions between raster and block data organization, as required for JPEG compression and expansion. For still compression and expansion a raster to raster mechanism is implemented. Thus, for still compression or expansion the raster to block operation must be done in software.

ZR36050 Control

The ZR36050 Control block implements the control signals and handshake required by the ZR36050. It also controls the flow of coded (compressed) data between the ZR36050 and the code buffer.

Code Buffer Control

The Code Buffer Control block manages the code buffer VRAM memory. It implements a code buffer consisting of four individual buffer "pages" in compression, and two buffer "pages" in expansion. In compression, each of the four pages contains one compressed field, and the software is responsible for reading every compressed field or every other compressed field, in accordance with whether the chosen resolution requires vertical decimation or not. In expansion, each of the two pages contains either a compressed field or a compressed frame (that is, two fields), in accordance with the setting of the Vertical Decimation bit (see Command Register 1 - Table 11), depending on the vertical decimation mode of the encoder that was used to code these files. Host system access to the code memory is mediated by this module, which arbitrates between host accesses, VRAM transfer cycles, and code memory refresh cycles.

Host System Interface

The Host System Interface block provides an interface to the host (ISA) bus and software. It contains the control registers that allow the host to set the operating modes and obtain status information. It decodes addresses for the various resources accessible by the host, and generates a "frame ready" interrupt signal in compression.

Interface Signal Descriptions

Table 3: Host System Interface

Name	Type	Description
HD(15:0)	I/O	16-bit bidirectional data bus, used for: - accessing the internal registers of the ZR36055, - accessing the code buffer, - accessing the strip buffer in still image compression or expansion.
$\overline{\text{MEMW}}$	I	Memory write strobe. Should be connected directly to the ISA signal $\overline{\text{MEMW}}$. Since the host accesses to the ZR36055 are all I/O, this signal is used only to prevent the ZR36055 from adding wait states during memory cycles on the Host (ISA) bus.
$\overline{\text{MEMR}}$	I	Memory read strobe. Should be connected directly to the ISA signal $\overline{\text{MEMR}}$. Since the host accesses to the ZR36055 are all I/O, this signal is used only to prevent the ZR36055 from adding wait states during memory cycles on the Host (ISA) bus.
$\overline{\text{IOCS16}}$	O	I/O chip select 16, indicates a 16 bit I/O access cycle.
H_ALE	I	Host address latch enable. Should be connected to ISA bus BALE.
AEN	I	Address enable. Differentiates between I/O and DMA cycles. Should be connected to ISA bus AEN. 0 - Valid I/O cycle 1 - DMA cycle The ZR36055 responds to the host access only when AEN is LOW
$\overline{\text{IORDY}}$	O	I/O ready. Indicates to the host that the current cycle should be extended with wait states. (e.g, when the host is trying to access the code buffer while it is busy).
HA(3:0)	I	The four (4) LSBs of the host address bus, used to select the internal resource accessed.
HA(9:4)	I	The six (6) MSBs of the host address bus, used for decoding access to the ZR36055, thus determining the I/O base address for the ZR36055.
IOBASE(1:0)	I	Two bits which select the I/O base address for the ZR36055.
$\overline{\text{REFRESH}}$	I	Refresh signal. Commands the ZR36055 to generate a refresh cycle to the code buffer VRAM.
$\overline{\text{IOR}}$	I	I/O read strobe.
$\overline{\text{IOW}}$	I	I/O write strobe.
$\overline{\text{IRQ}}$	O	Interrupt request line. The width of the $\overline{\text{IRQ}}$ pulse is in the range 390 ns to 500 ns.
H_RESET	I	Host reset. When active, causes the ZR36055 to immediately three-state all bidirectional drivers and enter the reset condition. (Active HIGH).
$\overline{\text{HDOE}}$	O	Host data output enable. Enables the external data bus transceivers. This signal is active during host access to the ZR36055.
$\overline{\text{IACS}}$	O	Internal memory address latch chip select. Strobe signal for an external latch, to latch the ZR36050 address for host access to its internal memory.
$\overline{\text{EXTCS}}$	I	External chip select. Used in cases where it is required to decode more than 10 host address bits to determine the base address of the ZR36055.

Table 4: Digital Video Interface

Name	Type	Description
VCLKX2	I	Clock input, at double the frequency of the video data clock. The frequency depends on the format and standard chosen: 29.5 MHz, square pixel PAL 24.5454 MHz, square pixel NTSC 27 MHz, CCIR PAL and NTSC This is the master clock for the ZR36055, in compression and expansion.
VCLK	I	Video data clock, at half the frequency of VCLKX2. 14.75 MHz, square pixel PAL 12.2727 MHz, square pixel NTSC 13.5 MHz, CCIR PAL and NTSC This is the pixel clock, in compression and expansion.
VSYNC	I/O	Vertical synchronization. Indicates the vertical position of the picture. Active high pulse.
HREF	I/O	Horizontal reference. Indicates active image data on the digital YUV bus. The positive edge marks the beginning of a new active line. Normally active (high) for 768 Y samples in square pixel PAL, 640 Y samples in square pixel NTSC, or for 720 Y samples for CCIR. HREF is also present during the vertical blanking.
HSYNC	O	Horizontal synchronization. Indicates the horizontal position of the picture. Active high pulse, generated in expansion in internal sync mode.
$\overline{\text{FEOUT}}$	O	Fast enable output. In compression (or IDLE) enables the digital video source bus. In expansion disables the digital video source bus by forcing the decoder to set its Y and UV outputs to the high impedance state.
$\overline{\text{VBUSEN}}$	O	Video bus enable. Enable signal for external transceivers on the Y and UV digital data buses.
Y(7:0)	I/O	8-bit luminance data. Input in compression, output in expansion.
UV(7:0)	I/O	8-bit multiplexed chrominance data. Input in compression, output in expansion.

Table 5: Strip Buffer Interface

Name	Type	Description
SMD(15:0)	I/O	16-bit strip memory data bus.
SMA(13:0)	O	14-bit strip memory address bus.
$\overline{\text{SMR}}$	O	Strip memory read strobe.
$\overline{\text{SMW}}$	O	Strip memory write strobe.

Table 6: Code Memory Interface

Name	Type	Short Description
CMD(7:0)	I/O	8-bit code memory data bus.
CMA(8:0)	O	9-bit code memory address bus.
CME_WE	O	Code memory mask enable/write enable. High during a code memory read cycle, low during a write cycle.
CTR_OE	O	Code memory transfer enable/output enable. High during a transfer cycle, low during a read cycle.
$\overline{\text{CCAS}}$	O	Code memory $\overline{\text{CAS}}$.
$\overline{\text{CRAS}}$	O	Code memory $\overline{\text{RAS}}$.
$\overline{\text{CSE}}$	O	Code memory serial clock enable.
CSC	O	Code memory serial clock.

Table 7: ZR36050 Interface

Name	Type	Short Description
CKEN	O	Clock enable. Enables the data clock and the internal PLL of the ZR36050. Must be connected to the CLKEN pin of the ZR36050.
DCLK	O	Data clock. Must be connected to CLK_IN of the ZR36050. The frequency is determined by the video standard and pixel format, and the FAST bit of Command Register 0.
$\overline{END}$	I	End of process. Indicates the end of a frame encoding or decoding. Must be connected to the $\overline{END}$ pin of the ZR36050.
$\overline{C\_RESET}$	O	ZR36050 RESET. The ZR36055 issues a RESET to the ZR36050 when H_RESET or the GRESET bit in Command Register 0 is active. Must be connected to the $\overline{RESET}$ pin of the ZR36050.
$\overline{STOP}$	I/O	Stop sending/receiving image data. In Compression - input from the ZR36050, indicating to the ZR36055 that it should stop transferring data to the ZR36050 at the end of the current block. In Expansion - output to the ZR36050 indicating that the raster to block module is busy and expects the ZR36050 to stop delivering image data at the end of the current block. Must be connected to the $\overline{STOP}$ pin of the ZR36050.
PDATA(7:0)	I/O	Pixel data bus of the ZR36050. In Compression - output from the ZR36055 to the ZR36050. In expansion - input from the ZR36050.
$\overline{DSYNC}$	I/O	Data synchronization pulse. The pulse width is one DCLK cycle. In compression - output signal indicating to the ZR36050 the start of an 8x8 block. It appears one DCLK before the first image data of a block. In expansion - input from the ZR36050 that appears one DCLK before the first data sample of a block. Must be connected to the $\overline{DSYNC}$ pin of the ZR36050.
$\overline{EOS}$	I/O	End of scan pulse. The pulse width is one DCLK cycle. In Compression - output signal indicating the last image data sample of each scan entering the ZR36050. In expansion - input from the ZR36050 indicating the last image data sample of each scan. Must be connected to the $\overline{EOS}$ pin of the ZR36050.
$\overline{CBUSY}$	O	Compressed data memory busy. Must be connected to the $\overline{CBUSY}$ pin of the ZR36050.
$\overline{CCS}$	I	Code memory chip select. Indicates that a data read or write operation between the ZR36050 and the code memory is in progress. Must be connected to the $\overline{CCS}$ pin of the ZR36050.
$\overline{CRD}$	O	ZR36050 internal memory read. Must be connected to the $\overline{RD}$ pin of the ZR36050.
$\overline{CWR}$	O	ZR36050 internal memory write. Must be connected to the $\overline{WR}$ pin of the ZR36050.

Table 8: Power & Test

Name	Type	Short Description
Test	I	Factory Test pin. In normal operation must be connected to ground potential (V_{SS}).
V_{DD}	Power	5 Volt power supply.
V_{SS}	Power	Power supply ground.

INTERFACES

Host System Interface

The ZR36055 Host System Interface is designed to support the ISA bus with minimal glue logic. All host accesses to the ZR36055 internal resources (the control registers), and to the external resources controlled by the ZR36055 (internal memory of the ZR36050, the code buffer, and the strip buffer) are mapped into the ISA bus I/O space. The Base Address of the ZR36055, decoded from HA[9:4], can be assigned by the two input pins IOBASE(1:0) according to Table 9.

Table 9: I/O Base Address

IOBASE 1	IOBASE 0	Base Address
0	0	200h
0	1	280h
1	0	300h
1	1	380h

The ZR36055 consumes 16 consecutive addresses in the ISA bus I/O space, starting from the Base Address.

Host accesses are 8 bits or 16 bits wide, depending on the resource accessed. When an access to one of the 16-bit resources is decoded, $\overline{\text{IOCS16}}$ is driven low by the ZR36055. Note that since $\overline{\text{IOCS16}}$ is not an open-drain output, an external buffer is needed to drive the ISA bus.

Ten ISA bus address bits are decoded by the ZR36055 to provide a glueless interface to the ISA bus. Decoding of the ISA address bits is done only while $\overline{\text{EXTCS}}$ is active (LOW), and AEN is LOW. In cases where more than ten bits must be decoded to determine the base address, the $\overline{\text{EXTCS}}$ pin can be used as a qualifier, generated by external decoding of higher address bits.

Under the assumption that the host data bus of the ZR36055 is connected to the system data bus by means of bidirectional transceivers, the ZR36055 generates a transceiver enable signal, $\overline{\text{HDOE}}$. $\overline{\text{HDOE}}$ is activated when $\overline{\text{EXTCS}}$ is active and AEN is LOW, one of the I/O commands ($\overline{\text{IOW}}$ or $\overline{\text{IOR}}$) is active, and the Base Address is decoded on HA[9:4].

$\overline{\text{IORDY}}$ is driven low only during host accesses to the code memory, if the code memory is temporarily unavailable. $\overline{\text{IORDY}}$ goes low after the falling edge of H_ALE. The ZR36055 cannot, however, distinguish between an I/O and a memory access cycle at this point, so if $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$ goes active, $\overline{\text{IORDY}}$ is immediately driven high. $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ have no function in the ZR36055 other than this. $\overline{\text{IORDY}}$, like $\overline{\text{IOCS16}}$, is not an open drain output, so an external buffer is needed to drive the ISA bus.

The $\overline{\text{IRQ}}$ output has to be connected to the selected interrupt request line of the ISA bus, through an external buffer. It is an active LOW signal which indicates that the compression of a field has been completed. The $\overline{\text{IRQ}}$ signal pulse width ranges between 390 ns and 500 ns.

Digital Video Interface

The Digital Video Interface of the ZR36055 conforms to the de-facto standard established by the Philips SAA7110 and SAA7111 decoders.

In compression, it can interface directly to the data and sync outputs of these decoders, or any other decoder or digital video source that provides equivalent clock, synchronization and video signals. VSYNC, the vertical sync signal, and HREF, the horizontal blanking signal, are inputs to the ZR36055 in compression.

In expansion, the ZR36055 can work in two synchronization modes, internal sync mode, and external sync mode. In internal sync mode, the ZR36055 generates data and sync signals that emulate those of the video decoder, and can therefore drive directly the video input of any scaling, display-overlay or composite video encoding device that accepts signals in this format. The exact periods of the synchronization signals (HREF, HSYNC and VSYNC) can be programmed to match the format used (CCIR or Square pixel, PAL or NTSC). VSYNC is driven high at the start of each field, for a period equivalent to six video lines. HREF is driven high during the active-pixels interval of each line; the exact interval is programmable to correspond to the pixel format and video standard being used. HSYNC, the horizontal synchronization signal, is a programmable output signal generated in internal sync mode; this signal is required by some of the overlay processors. In external sync mode, the ZR36055 outputs the data in synchronization with the sync signals provided by an external device (e.g., the video decoder or a video encoder).

VCLKX2 and VCLK provide the reference for digital video interface signal timing. Both of these clock signals are required inputs in compression and in expansion.

$\overline{\text{FEOUT}}$ and $\overline{\text{VBUSEN}}$ are output signals that can be used to control external three-state buffers and bidirectional data transceivers for the digital video and sync signal lines. The truth table for these signals is shown in Table 10.

Table 10: Truth Table for $\overline{\text{FEOUT}}$ and $\overline{\text{VBUSEN}}$

Operating Mode	$\overline{\text{FEOUT}}$	$\overline{\text{VBUSEN}}$ [1]
Compression	Low	Low
Expansion	High	Low

1. $\overline{\text{VBUSEN}}$ is in the HIGH state after activation of H_RESET and before the ZR36055 is commanded to be active by the ACTIVE bit of the COM1 register, and driven LOW only after the ACTIVE command. It is driven high again only by activation of H_RESET.

FEOUT and VBUSEN change state at most 5 VCLKX2 periods after the falling edge of IOW in the write cycle to the COM0 or COM1 register that caused the change.

The form of the component digital video signal expected in compression and output in expansion is shown in Figure 3.

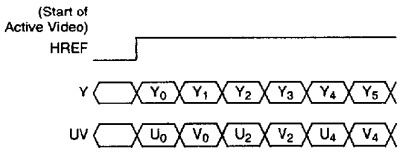


Figure 3. Digital Video Component Sequence

Strip Memory Interface

The Strip Memory Interface supports an 8KWord strip memory composed of 2 x 8K x 8 SRAM for a system based on the ZR36055-21 (Low End system), and a 32KWord strip memory consisting of 2 x 32K x 8 SRAM for a system based on the ZR36055-29.5 (High End system). The timing of the interface signals is consistent with the specification of typical SRAMs of 15ns or faster speed (for example, Micron Technologies MT5C2568-15). The strip buffer interface is composed of a 13-bit address bus for the Low End systems and a 14-bit address bus for the High End systems, a 16-bit data bus, and read and write control signals. The raster-to-block and block-to-raster operations are performed by suitable addressing of the SRAM address bus, along with appropriate read or write commands.

Code Memory Interface

The Code Memory Interface supports a 128Kbyte code memory consisting of a 128K x 8 VRAM (with 128K x 8 DRAM and 256 x 8 SAM) for the Low End subsystem based on the ZR36055-21, and a 256KByte code memory consisting of a 256K x 8 VRAM (with 256K x 8 DRAM and 512 x 8 SAM) for the High End subsystem based on the ZR36055-29.5. The timing of the interface signals is consistent with the specifications of typical VRAMs (such as Micron Technologies MT42C8128 or MT42C8256) of 70ns or faster speed. The VRAM used must have bidirectional serial ports.

The serial port of the VRAM is used for the compressed data flowing between the code memory and the ZR36050. The parallel port is used for accesses to the code memory by the host system. Since the host system bus is 16 bits wide and each host access translates to two code memory accesses to sequential locations in the same page, the parallel port accesses are always implemented as fast page mode cycles. Note that the ZR36055 does not require Extended Data Out (EDO) in page mode reads.

In compression, the ZR36055 performs a "Write Transfer (SAM-to-DRAM Transfer)" cycle to transfer the Serial Access Memory to a page of DRAM. In expansion, the ZR36055 performs a "Real Time Read Transfer (DRAM-to-SAM Transfer)" cycle to transfer a DRAM page to the Serial Access Memory.

Code Memory VRAM refresh is timed by the REFRESH input signal of the Host System Interface. Refresh cycles are of the CAS-before-RAS type.

ZR36050 Interface

The ZR36050 interface performs the following operations: It produces the clocks and general control signals for the ZR36050, handles the ZR36050 internal memory access, controls the image data transfer between the ZR36055 and ZR36050, and controls the ZR36050 access to the compressed data memory (code buffer).

The ZR36050 clocks and general control signals are:

- DCLK, the data clock of the ZR36050 (connected to its CLK_IN pin) is produced by the ZR36055.
- CLKEN (enabling the internal ZR36050 PLL) is controlled by the host through the COM1 register.
- C_RESET resets the ZR36050 during the initialization stage.
- END coming from the ZR36050 signals the end of a compression or expansion process. During continuous compression or expansion, activation of END initiates the next GO to the ZR36050.

A special mechanism in the ZR36055 allows the host to access the ZR36050's internal memory. Two of the control ports implemented by the ZR36055 are dedicated to providing the control signals for the data and address paths, which are external to the ZR36055. When the host performs a write access to the ZR36050_Address port, the host data bus is latched into an external address register by the IACS control signal. When the host subsequently accesses the ZR36050_Data port, the ZR36055 drives CRD or CWR as appropriate, to perform a host read or write access to the ZR36050 internal memory at the address stored in the external address register.

The Pixel interface of the ZR36050 is handled by the ZR36055 as follows:

- In compression, the PDATA bus is used to transfer the image data into the ZR36050. The DSYNC (Data Synchronization) signal preceding each block is produced, as well as the EOS (End Of Scan) signal at the end of the image, together with the last pixel of the last block of the image. The ZR36055 checks that the STOP signal of the ZR36050 is not active before sending out a block.
- In expansion, DSYNC and EOS change from output to input signals, and STOP changes from an input to an output signal. The ZR36055 receives the image data a block at a time on the PDATA bus. Each block is preceded by a DSYNC, and the last pixel of the last block of the image is accompanied by the EOS signal. STOP is activated when the ZR36055 is not ready to accept any more blocks.

The ZR36050 access (Read or Write) to the compressed data is controlled using the $\overline{CCS}$ and $\overline{CBUSY}$ signals. In compression, an active $\overline{CCS}$ signal initiates a write cycle to the code buffer VRAM serial port. Note that the CODE bus of the ZR36050 must be programmed to work during compression at 1 clock per write cycle (CFIS=0). During expansion, an active $\overline{CCS}$ signal initiates a read cycle from the code buffer VRAM serial port. The CODE bus of the ZR36050 must be programmed to work during expansion at 2 clocks per read cycle (CFIS=1). $\overline{CBUSY}$ is activated when the code buffer VRAM is not available to the ZR36050 (during refresh or transfer cycles for example).

CONTROL REGISTERS

This section describes the ZR36055's control registers and control ports, which consist of:

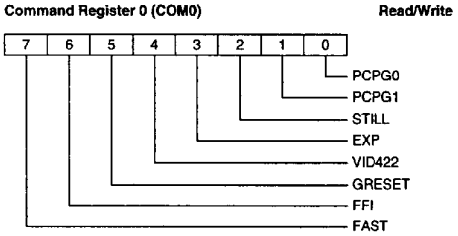
- Three Command registers, used by the host to set the operating mode of the ZR36055 and to control its operation. Command Register 2 is a hybrid, in that it also contains a readable hard-coded "ZR36055 ID" field.
- One Status register, typically read after each frame is processed (in either expansion or compression), indicates the process status.
- Three Information registers, read after each frame is processed (in either expansion or compression), provide information needed by the software to track the operation of the subsystem.
- Two ZR36050 access ports provide a means for the host software to access the internal memory and registers of the ZR36050.
- Two ZR36055 data registers, used to transfer information between the host and the ZR36055.
- An indexed array of registers known collectively as the SIZE register, hold numerical data used to control operation of the ZR36055.

Table 11 lists the control registers of the ZR36055 along with their address offsets relative to the I/O base address, read/write accessibility, and widths.

Table 11: Host Access Address Map

Accessed Resource	Offset Address	Read/ Write	Width
Command Register 0, COM0	09 h	R/W	8-bit
Command Register 1, COM1	0A h	R/W	8-bit
Command Register 2, COM2	08 h	R/W	8-bit
Status Register, STATUS0	05 h	R	8-bit
Field Count, FCNT	0B h	R	8-bit
Length Register 0, LEN0	06 h	R	8-bit
Length Register 1, LEN1	07 h	R	8-bit
ZR36050_Data	04 h	R/W	8-bit
ZR36050_Address	02 h	W	16-bit
Strip buffer Data	0C h	R/W	16-bit
Code buffer Data	00 h	R/W	16-bit
SIZE	0E h	W	16-bit

Command Register 0 (COM0), Read/Write



Field	Name	Description	Reset state
FAST[1]	ZR36050 clock speed range	0: SLOW clock (12.27,13.5,14.75 MHz for square pixel NTSC, CCIR, square pixel PAL respectively). 1: FAST clock (24.5,27,29.5 MHz for square pixel NTSC, CCIR, square pixel PAL respectively)	1
FFI	First Field ID	0: The first expanded field is field II 1: The first expanded field is field I (field II is the field in which the trailing edge of VSYNC falls in the middle of a line) Not applicable for compression mode	1
GRESET	Global Reset	0: Resets the internal ZR36055 circuits, activates the C_RESET signal to reset the ZR36050	0
VID422	Digital video format	0: Expand YUV 411 digital video format 1: Expand YUV 422 digital video format Not applicable for compression mode	1
EXP	Compression or Expansion Mode	0: Compression mode 1: Expansion mode	0
STILL	Still image mode	0: Continuous compression or expansion 1: Still compression or expansion	0
PCPG[1:0]	Code buffer page selected by host	Using this field, the Host selects the code buffer page to load in expansion or unload in compression. In compression mode, both bits are used; the code buffer is partitioned into 4 pages. In expansion, only PCPG0 is used; the code buffer is partitioned into 2 pages Note: the ZR36055 will not compress into or expand from the code buffer page selected by PCPG.	0 0

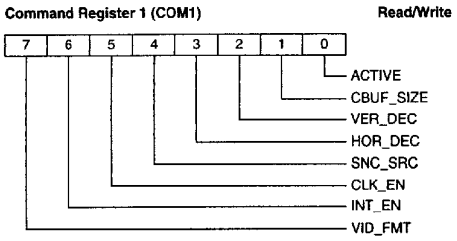
1. The FAST bit determines the frequency of DCLK, the data clock for the ZR36050. When 1 (FAST clock), the frequency of DCLK is the same as that of VCLKX2, and when 0 (SLOW clock), the frequency of DCLK is one half that of VCLKX2.

   FAST clock can be used with the high-end 055 chip-set in all resolution, decimation and cropping modes.

   SLOW clock can be used only if it is known that the ZR36050 is able to process the image when operating at this clock frequency. Generally, this means that SLOW clock can be used only if the compressed image width is equal to or smaller than one-half of the full digitized image width, that is, in Quarter or Half Horizontal resolution:
   • when the image is decimated horizontally (HOR_DEC of COM1 is 1), or
   • when the image is cropped to half the original width or smaller.

   SLOW clock must be used with the low-end chip-set (ZR36050-21 and ZR36055-21).

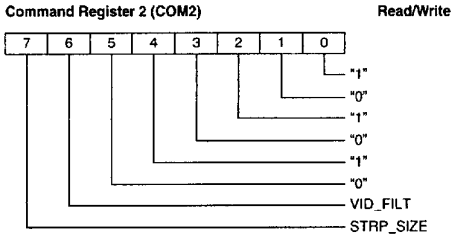
Command Register 1 (COM1), Read/Write



Field	Name	Description	Reset state
VID_FMT	Video Format	Determines the sync signals structure in expansion mode with internal sync 0: PAL video format 1: NTSC video format	1
INT_EN	Interrupt Enable	Enables the ZR36055 interrupt line 0: Disable, 1: Enable	0
CLK_EN	Clock Enable	Enables the ZR36050 clock 0: Disable, 1:Enable This bit directly controls the CKEN pin	0
SNC_SRC	Sync Source	Synchronization source in Expansion 0: External Synchronization, 1: Internal Synchronization	0
HOR_DEC	Horizontal Decimation, Interpolation	In compression mode- selects 2:1 horizontal decimation In expansion mode- selects 1:2 horizontal interpolation 0: no decimation or interpolation, 1: with decimation or interpolation	0
VER_DEC	Vertically Decimated Frame	In compression mode - not applicable [1] In expansion mode - defines 1:2 vertical decimation (i.e., defines whether the expanded frame contains 1 or 2 fields) 0: not decimated (2 fields) 1: decimated (1 field) If 1, the ZR36055 expands each field twice, on average	0
CBUF_SIZE	Code Buffer Size	Defines the code buffer and page sizes 0: code buffer size=128KBytes VRAM, page size= 32 KBytes in compression, 64KBytes in expansion 1: code buffer size=256KBytes VRAM, Page size= 64 KBytes in compression 128 KBytes in expansion	1
ACTIVE	Active	0: Activated by the software, to initiate a compression or expansion sequence. 1: Inactive	1

1. In continuous compression mode, the 055 subsystem always compresses every field. Vertical decimation (for quarter and half vertical resolutions), is accomplished entirely by the host software, by skipping every other code buffer page. The data in the unwanted pages is not read out by the host, and is not transferred through the host data bus. (The host must, however, read out the status information of each page.)

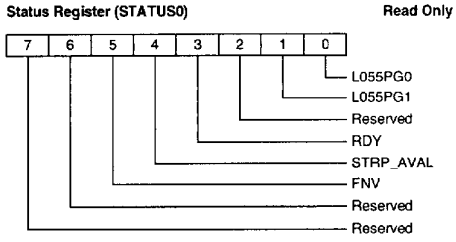
Command Register 2 (COM2), Read/Write



Field	Name	Description	Reset state
STRP_SIZE	Strip Size	Defines the strip buffer size 0: 8KBytes SRAM 1: 32 KBytes SRAM	1
VID_FILT	Video Filter	Defines optional filter when doing Horizontal Decimation/Interpolation [1] 0: no filtering 1: use internal filters	1
Bits 5:0	ID	ZR36055 ID field, 15 hex	

1. The decimation filter is a 3-tap filter with coefficients (0.25, 0.5, 0.25). The first pixel in a line is copied as is. The interpoation filter is a 2-tap filter with coefficients (0.5, 0.5). The last pixel in a line is duplicated.

Status Register (STATUS0), Read Only



Field	Name	Description	Reset state
FNV	Field Not Valid	When 1, indicates that the last compressed field was invalid (i.e., its size exceeded the size of a page in the code buffer or when the data in the strip buffer was overwritten).	0
STRP_AVAL	Strip Buffer Available	Used only in still compression or expansion mode: when 1, indicates that the ZR36055 is ready for a strip to be written or read by the host.	0
RDY	Ready	Active High: Set when the ZR36050 asserts the END (end of process) signal. Cleared when the host reads Length Register 1 (LEN1).	0
L055PG[1:0]	Last 055 Page	Reflects the number of the last code buffer page processed by the ZR36055 in compression or expansion. In expansion, since there are only two code buffer pages, L055PG1 can be ignored.	0 0

Information Registers

Name	Description
FCNT	Fields/Pages counter register, 8 bit, Read only. Provides a running modulo 256 count of fields compressed or code buffer pages expanded, enabling the host software to keep track of dropped or skipped frames.
LEN0	Low byte of the code buffer page length, 8 bit, read only.
LEN1	High byte of the code buffer page length, 8 bit, read only. LEN1 and LEN0 indicate the actual size in bytes of the compressed field in the code buffer page defined by the L055PG field of the STATUS0 register.

ZR36050 Access Ports

Name	Description
ZR36050_ Address	ZR36050 internal memory address port, 16 bit, write only. The access to this port activates the $\overline{IACS}$ signal to latch the host data bus in an external register connected to the ZR36050 host address bus.
ZR36050_Data	ZR36050 internal memory data port, 8 bit, read/ write. Accesses to this port are directed to the ZR36050 host data port.

ZR36055 Data Registers

Name	Description
Strip Buffer Data	Strip buffer data, 16 bit, read only in expansion, write only in compression. The ZR36055 automatically increments the strip buffer address on successive accesses to this port.
Code Buffer Data	Code buffer compressed data, 16 bit, read only in compression, write only in expansion. The ZR36055 automatically increments the code buffer address on successive accesses to this port.

When accessing the 16-bit Code Buffer Data register, the earlier byte of the JPEG stream is on the lower byte (bits 7:0) of the data bus. Similarly, when accessing the Strip Buffer Data register, the earlier sample is on the lower byte of the data bus.

SIZE Registers

This indexed array of registers defines the desired size of the processed image, numerical data used by the internal sync generator, and the background color when images smaller then the full resolution image are displayed. The register index is specified by the 4 MSBs, while the value is defined by the 11 LSBs. Bit 11 is not used in most of the SIZE registers; in the background color registers it extends the index, while in the NBLK register it indicates the last strip.

Table 12: SIZE Register Description [1] [2] [3] [4] [5] [6] [7]

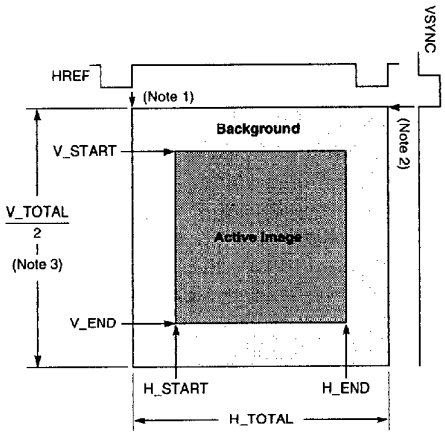
Name	Bits (15:12) (Index)	Bit 11	Bits (10:0)	Reset state
Horizontal Image START [8] (H_START)	0 h	X	Value (Pixels)	0
Horizontal Image END (H_END)	1 h	X	Value (Pixels)	0
Horizontal Image TOTAL (H_TOTAL)	2 h	X	Value (Pixels)	0
Hsync START (HS_START)	3 h	X	Value (Pixels)	0
Hsync END (HS_END)	4 h	X	Value (Pixels)	0
BLANK_ START	5 h	X	Value (Pixels)	0
Vertical Image START (V_START)	8 h	X	Value (Lines)	0
Vertical Image END (V_END)	9 h	X	Value (Lines)	0
Vertical Image TOTAL [9] (V_TOTAL)	A h	X	Value (Lines)	0
Number of MCU's per line - 1 (NMCU)	C h	X	Value	0
Number of blocks per strip - 1 (NBLK)	D h	last strip =1 not last strip = 0	Value	0
Y component Background (YBG)	E h	0	Value	11001000 (200 decimal)
U/V component Background (UVBG)	E h	1	Value	10110100 (180 decimal)

1. In continuous compression mode, H_START, H_END, H_TOTAL, V_START, V_END, V_TOTAL and NMCU are required.
2. In continuous expansion mode, H_START, H_END, H_TOTAL, V_START, V_END, V_TOTAL and NMCU are required. HS_START, HS_END and BLANK_START are required only in internal sync mode.
3. In still compression and expansion modes, only NBLK is required.
4. H_START, H_END, BLANK_START, HS_START and HS_END are measured from the rising edge of HREF.
5. V_START and V_END are measured from the falling edge of VSYNC.
6. In compression, (H_END - H_START) must be a multiple of 16 pixels if horizontal decimation is not used, and a multiple of 32 pixels if horizontal decimation is used.

   In expansion, (H_END - H_START) must equal the compressed image width if horizontal interpolation is not used, and twice the compressed image width if horizontal interpolation is used. The compressed image width must be a multiple of 16 if the format is YUV 4:2:2, or a multiple of 32 if the format is YUV 4:1:1.
7. In compression, (V_END - VSTART) must be a multiple of 8 lines.

   In expansion, (V_END - VSTART) must equal the height of the compressed field, which must be a multiple of 8.
8. H_START must have an even value.
9. V_TOTAL is the number of lines in the full interlaced frame. It must have an odd value.

The following diagrams further describe the video synchronization parameters.



Notes: 1. Rise of HREF signal marks the beginning of a video line.
2. The falling edge of VSYNC marks the beginning of a field, and is the reference point for V_START and V_END.
3. V_TOTAL applies to the full frame size (625 lines for PAL, 525 for NTSC).
4. The diagram depicts the active image portion of each field.

Figure 4. Definition of Active Image and Background Regions

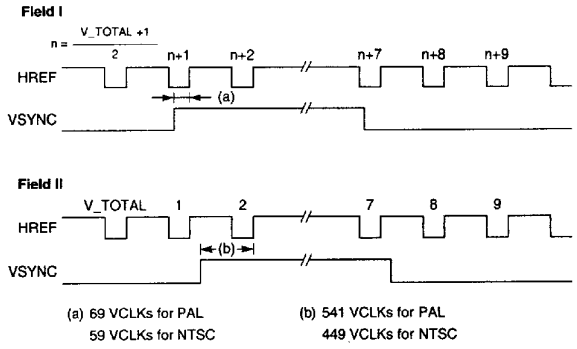


Figure 5. Definition of Field I and Field II

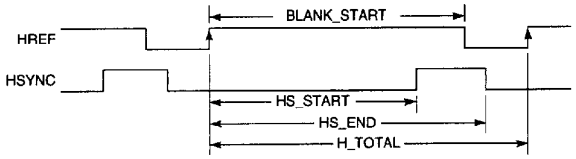


Figure 6. Definition of Horizontal Sync and Blanking Signals in Internal Sync Mode

OPERATING MODES

The 055 Chip Set has four operating modes:

- Continuous compression
- Continuous expansion
- Still compression
- Still expansion

This section describes the operation of the chip set in each of the above modes. An Application Note, giving a more detailed step-by-step account of the procedures the host software must perform, including a specific example, is available. For a detailed description of the registers mentioned in this section, see the Control Registers section.

Continuous Compression (Capture)

An 055 subsystem can compress any video sequence consisting of YUV 4:2:2 video frames, at full, half and quarter resolutions, for both CCIR and square pixel frame sizes. The actual frame size compressed in each of the available resolutions can be reduced from its nominal value by cropping.

After compression is activated (by setting the ACTIVE bit of the COM0 register to 0), the first field to be compressed by the ZR36055 is field II, which is defined to be the field in which the trailing edge of VSYNC falls in the middle of a line.

The ZR36055 receives the YUV 4:2:2 digital video through the digital video bus, and performs, when required, horizontal decimation with optional filtering. Next, the raster to block conversion is performed using the external double strip buffer. The ZR36055 then routes the YUV blocks to the ZR36050, where each 8x8 pixel block is compressed according to the JPEG baseline algorithm, yielding the coded (compressed) image. The compressed JPEG data is subsequently stored in the code buffer.

Note that in compression, the code buffer is composed of 4 pages of size equal to 1/4 of the code buffer size. Each page contains 1 compressed field.

At the end of each compression pass by the ZR36050, the ZR36055 detects the $\overline{\text{END}}$ signal, and starts a new compression pass by writing a GO command to the ZR36050. In parallel, it checks the state of the RDY bit in the STATUS0 register. If RDY = 0, indicating that the status and information registers associated with the previously compressed field have been read by the host software, the ZR36055 sets the RDY bit to 1, updates the information registers for the current field, and activates the interrupt to the host. If RDY = 1 when checked, indicating that the host did not respond to the previous interrupt, and the previous status and information registers were not yet read by the host software, the ZR36055 does not perform the update, and does not activate the interrupt. Thus the status information associated with the newly compressed field is lost. Host software can keep track of lost fields of this type by means of the FCNT register.

The RDY bit is cleared when the host has read the complete set of status and information registers (STATUS0, FCNT, LEN0, LEN1, in this order).

The host software reads out the contents of a code buffer page by setting the PCPG field in the COM0 register to the selected buffer page number; the selected page is mapped to an ISA bus I/O port. Normally, the ZR36055 fills the code buffer pages sequentially; however, if the next page in sequence is currently selected by PCPG, the ZR36055 does not advance to this page and overwrites the previous page instead. To prevent this, the host must keep up with the ZR36055 by responding to the interrupts and reading the code buffer in a timely manner.

Continuous Expansion (Playback)

An 055 subsystem can expand a JPEG Baseline compressed video sequence consisting of frames of any supported resolution in YUV 4:2:2 format. In addition, for backward compatibility with the 045 Chip Set, the 055 Chip Set supports expansion of YUV 4:1:1 format JPEG compressed video, at up to Quarter resolution. The sequence is not required to have been compressed by the 055 subsystem, as long as each compressed frame is fully JPEG compliant, and its size does not exceed the code buffer page size (Code buffer page size limit is 128 KBytes for the High End ZR36055-29.5 chip set and 64KBytes for the Low End ZR36055-21 chip set respectively).

In expansion, the code buffer is partitioned into two pages, each equal to one half of the code buffer memory size. Each page can contain either one field or two fields, depending on whether the compressed frames consist of one field (Quarter and Half Vertical resolutions) or two fields (Full and Half Horizontal resolutions) each.

To expand a compressed video sequence, the host software loads the compressed data a frame at a time, via the ZR36055, into the two available code buffer pages, and the 055 subsystem automatically expands them alternately. When expansion of a frame is complete, the ZR36055 checks the PCPG field of the COM0 register to determine whether the other code buffer page is available, that is, not selected by PCPG. If it is available, it starts expanding the new frame, otherwise, it expands the previous page again (In full or half horizontal resolution, it re-expands both fields of the compressed frame before checking PCPG again. In half vertical or quarter resolution it checks PCPG after each re-expansion of the field). In parallel, it sets the RDY bit of the STATUS0 register to 1. The host software must poll the RDY bit to determine when a code buffer page is ready for a new frame to be written into it. The RDY bit is cleared by the ZR36055 as soon as the host has acknowledged the ready indication by reading the complete set of status and information registers.

Each expanded field is transferred onto the digital video bus for display. In case of Half Vertical and Quarter resolution modes,

each compressed frame comprises one field, and therefore each page in the code buffer contains one field; each field is expanded twice on average, yielding a 50 or 60 fields per second output video sequence.

When the reconstructed image line length is less than or equal to half of the original line length of each video standard and format (see Table 1), optional horizontal interpolation with or without filtering may by used. Thus, the expanded frames are transformed by the ZR36055 back to their original format (CCIR 601 or square pixel at the desired resolution).

For a coded bit stream originating from a YUV 4:1:1 sequence, the ZR36055 interpolates the chrominance components, thus generating a YUV 4:2:2 digital video output.

In expansion, horizontal blanking, horizontal sync, and vertical sync signals may be generated by the ZR36055 when working in internal sync mode, or horizontal blanking and vertical sync can be supplied by an external source in external sync mode.

After it has finished expanding a frame, the 055 subsystem expands the next valid frame in the code buffer. If there are no more valid frames, owing to the host system lagging behind, the 055 subsystem repeats expansion of the last valid frame, and continues to do so until a new frame is written into the code buffer by the host. Thus, the 055 subsystem transparently handles expansion of a sequence that was recorded at a frame rate of less than the standard 25 or 30 frames per second, or one in which frames were dropped at arbitrary intervals.

Still Compression

In the Still Compression mode of operation, the image to be compressed is provided to the ZR36055 through the host interface, rather than through the video interface. The ZR36055 does not perform raster-to-block reordering of the pixels in this case, rather, it transfers the data samples to the ZR36050 in the order they are received from the host. For this reason, the still compression mode of operation of the ZR36055 can also be used to implement lossless compression (with some additional circuitry), component interleave, compression of more than three color components and larger resolutions, in the ZR36050.

When using the still compression mode for JPEG baseline compression, the raster-to-block operation, and color space conversion if needed, must be performed by the host software.

The host feeds the image data to the ZR36055 a strip at a time, with handshake based on host software polling of the STRP_AVAL status bit. The last strip of the image is handled as a special case: if bit 11 of the NBLK SIZE register is 1, the ZR36055 activates $\overline{EOS}$ to the ZR36050 at the end of the strip. At the end of the process, the compressed image resides in the code buffer. When the ZR36050 activates $\overline{END}$, the ZR36055 generates an interrupt to the host indicating that the image can be read from the code buffer.

Still Expansion

As is the case for Still Compression, in the Still Expansion mode of operation the ZR36055 does not perform the block to raster function, and provides the expanded data to the host in the block format supplied by the ZR36050. The host software must perform the block-to-raster reordering of the pixels, as well as color space conversion, if necessary.

The ZR36055 controls the operation by allowing the ZR36050 to expand a strip at a time. As in the case of Still Compression, the STRP_AVAL status bit indicates when a new strip is ready to be read out by the host. Note that the host software must identify the last data word of the last strip by calculation based on the image size.

Note: *When the ZR36055 is operated in still compression or expansion mode, a square-pixel video decoder must be programmed for PAL mode rather than NTSC, to provide the highest possible clock frequency to the ZR36055. Otherwise there is a possibility of timing violations on the ISA bus interface to the strip buffer, causing incorrect data transfers.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65 C to +150 C
Supply Voltage to Ground ..... -0.5V to +7.0V
DC Output Voltage ..... -0.5V to VCC+0.5V
DC Input Voltage ..... -0.5V to VCC+0.5V
DC Input Current, any single input ..... -25 mA to +25 mA
DC Output Current, any single output ..... -25 mA to +25 mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above those limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Ambient Temperature ..... 0 C to +70 C
Supply Voltage ..... 4.75V to 5.25V

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4 mA, all outputs except VCLK and VCLKX2
						I_{OL} = 16 mA, VCLK and VCLKX2
V_{OH}	Output High Voltage	3.7			V	I_{OH} = -4 mA, all outputs except VCLK and VCLKX2
						I_{OH} = -16 mA, VCLK and VCLKX2
I_{LI}	Input Leakage Current			±20	µA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Output Leakage Current			±20	µA	$V_{OUT} = V_{CC}$ or GND, output disabled
C_{IN}	Input Capacitance			10	pF	
C_{IO}	Output and I/O capacitance			15	pF	
I_{CC}	Power Supply Current			390 290	mA mA	29.5MHz 21MHz

AC CHARACTERISTICS

Digital Video Interface, Clocks

Input Requirements

Symbol	Parameter	Min	Max	Unit	
TA1	VCLKX2 period	32		ns	40% to 60% duty cycle
TA2	VCLK period	2 * TA1			
TA3	VCLK after VCLKX2 skew	1	8	ns	

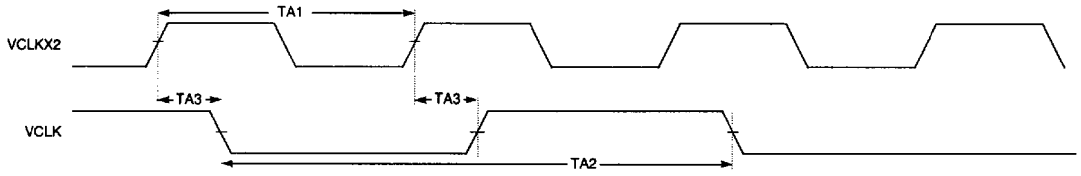


Figure 7. Digital Video Interface, VCLK and VCLKX2

Digital Video Interface, Compression, Input mode

Input Requirements

Symbol	Parameter	Min	Max	Unit	
TA4	VSYNC, HREF setup to VCLKX2	4		ns	
TA5	VSYNC, HREF hold from VCLKX2	8		ns	
TA6	YD, UV setup to VCLKX2	4		ns	
TA7	YD, UV hold from VCLKX2	8		ns	

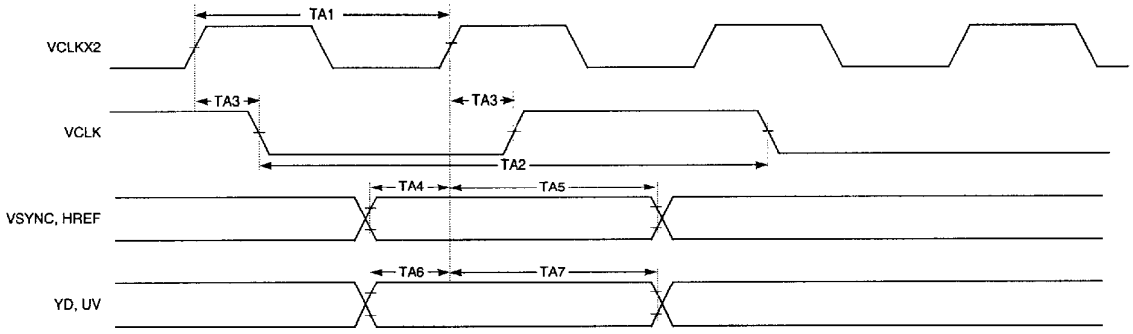
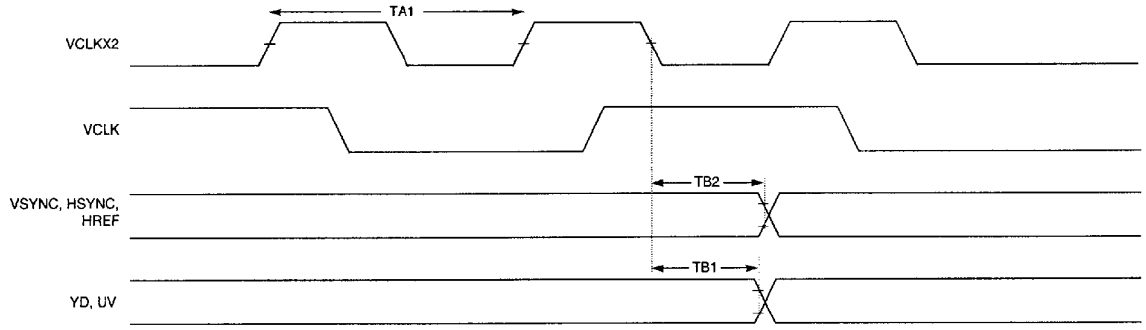


Figure 8. Digital Video Interface, Compression

Digital Video Interface, Expansion, VSYNC and HREF in Output Mode

Output Characteristics

Symbol	Parameter	Min	Max	Unit	notes
TB1	VCLKX2 to Y, UV output delay	0	29	ns	
TB2	VCLKX2 to VSYNC, HSYNC, HREF output delay	0	29	ns	



Note: The video and sync outputs are actually driven out on the falling edge of VCLKX2 that occurs when VCLK is high. This is done to allow reliable sampling of the outputs by the rising edge of VCLK.

Figure 9. Digital Video Interface, Expansion

Digital Video Interface, FEOUT and VBUSEN

Output Characteristics

Symbol	Parameter	Min	Max	Unit	notes
TY1	State change delay of FEOUT and VBUSEN		5 * TA1	ns	From falling edge of IOW

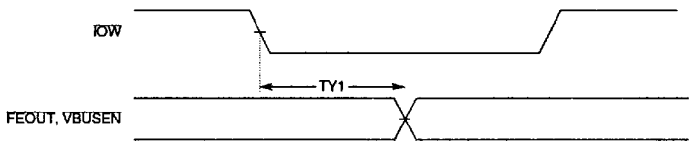


Figure 10. FEOUT and VBUSEN

ISA Interface I/O Read and Write Cycles

Input Requirements: VCLKX2 frequency = 29.5 MHz

Symbol	Parameter	Min	Max	Unit	Notes
TC1	H_ALE pulse width	48		ns	
TC2	delay from IOR/IOW disable to next H_ALE pulse	33		ns	
TC3	AEN active to H_ALE falling edge	100		ns	
TC4	AEN rise after IOR/IOW disable	30		ns	
TC5	HA setup to H_ALE falling edge	26		ns	
TC6	HA hold to IOR/IOW disable	40		ns	
TC7	IOR, IOW delay after HA	23		ns	
TC8	IOR, IOW pulse width	147		ns	16 bit
		509		ns	8 bit
TC9	I/O recovery time [1]	152 (188)		ns	
TC10	Write data valid delay after IOW falling edge		0	ns	16 bit
			61	ns	8 bit
TC11	Write data hold	25		ns	
TC18	IORDY inactive to IOR/IOW rising edge	120		ns	
TC19	EXTCS delay from HA		15	ns	

1. For read cycles from the strip buffer memory in still expansion mode, the minimum requirement for TC9, I/O Recovery Time, is 188 ns. For all other operating modes, the minimum requirement is 152 ns.

Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
TC12	Read data valid delay after IOR falling edge		103	ns	16 bit
			310	ns	8 bit
TC13	Read data hold	0		ns	
TC14	IOCS16 delay from valid HA		95	ns	
TC15	IOCS16 hold after HA change	0		ns	
TC16	IORDY delay from IOR/IOW falling edge		54	ns	
TC17	IORDY active pulse width	120	840	ns	
TC20	HDOE delay from I/O command active	7	24	ns	
TC21	HDOE hold after I/O command inactive	7	20	ns	

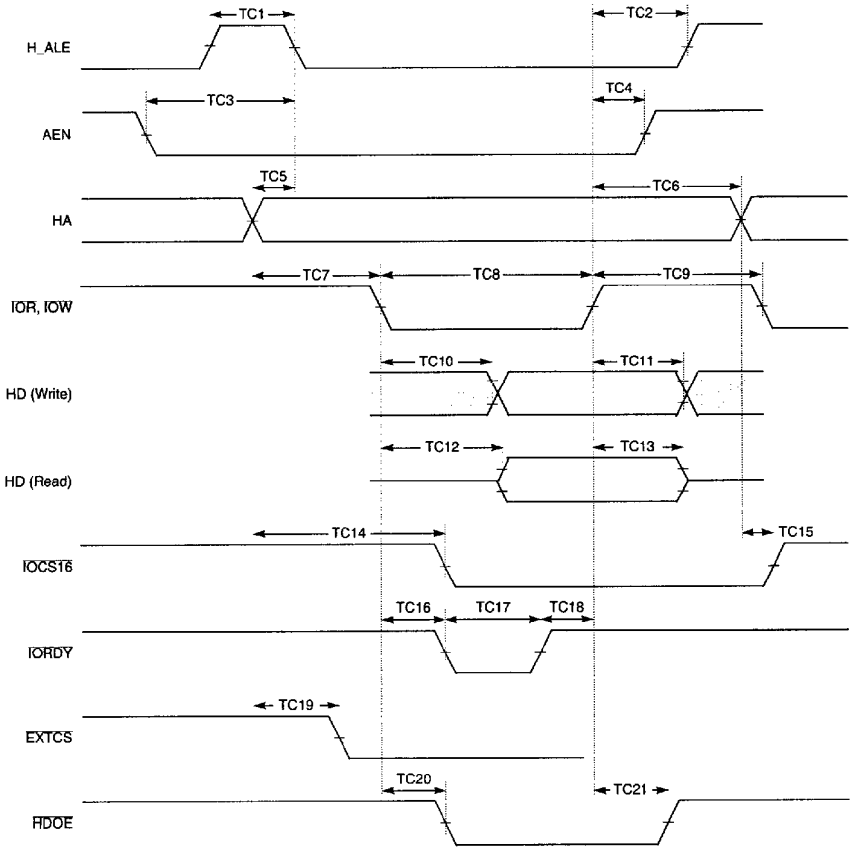


Figure 11. ISA Interface I/O Read and Write Cycles

Code Buffer VRAM Read Cycle, Compression (Fast Page Mode)

Input Requirements: VCLKX2 frequency = 29.5 MHz

Symbol	Parameter	Min	Max	Unit	
TJ9	CD valid delay from $\overline{CCAS}$		20	ns	
TJ10	CD valid delay from CTR/OE		20	ns	
TJ11	CD hold after $\overline{CCAS}$	3		ns	

Output Characteristics

Symbol	Parameter	Min	Max	Unit	
TJ1	$\overline{CRAS}$ width		15	us	
TJ2	$\overline{CRAS}$ to $\overline{CCAS}$ delay	68		ns	
TJ3	$\overline{CCAS}$ width	32		ns	
TJ4	$\overline{CCAS}$ precharge time	34		ns	
TJ5	Row address setup	34		ns	
TJ6	Row address hold	34		ns	
TJ7	Column address setup	33		ns	
TJ8	Column address hold	33		ns	
TJ12	$\overline{CRAS}$ precharge time	68		ns	
TJ13	Read cycle time	68		ns	
TJ14	CTR/OE hold after $\overline{CRAS}$ falling edge	68		ns	

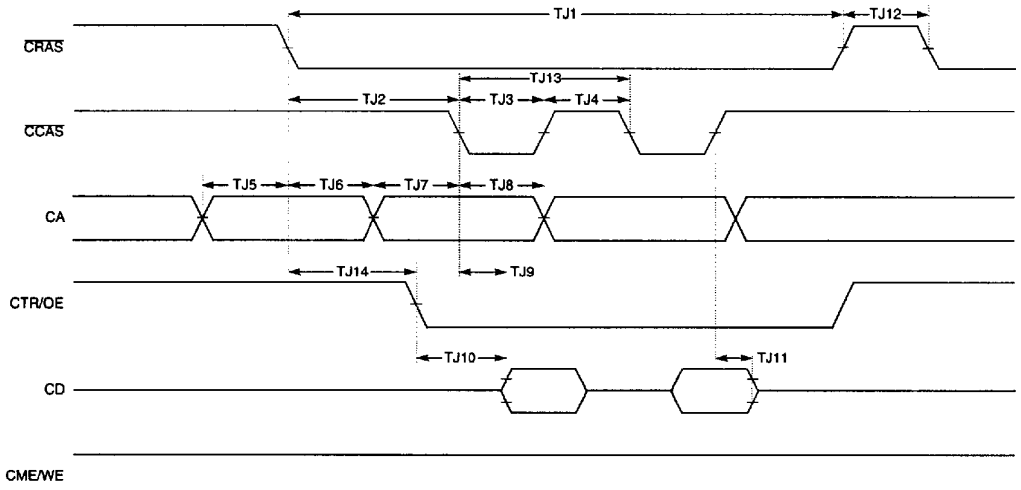


Figure 12. Code Buffer VRAM Read Cycle, Compression (Fast Page Mode)

Code Buffer VRAM Write Cycle, Expansion (Fast Page Mode)

Output Characteristics: VCLKX2 frequency = 29.5 MHz

Symbol	Parameter	Min	Max	Unit	
TK1	$\overline{CRAS}$ width		15	us	
TK2	$\overline{CRAS}$ to $\overline{CCAS}$ delay	68		ns	
TK3	$\overline{CCAS}$ width	32		ns	
TK4	$\overline{CCAS}$ precharge time	34		ns	
TK5	Row address setup	34		ns	
TK6	Row address hold	34		ns	
TK7	Column address setup	34		ns	
TK8	Column address hold	33		ns	
TK9	CME/WE setup before $\overline{CCAS}$	34		ns	
TK10	CD setup before $\overline{CCAS}$	26		ns	
TK11	CD hold after $\overline{CCAS}$	34		ns	
TK12	$\overline{CRAS}$ precharge time	68		ns	
TK13	Write cycle time	68		ns	
TK14	CTR/OE hold time after $\overline{CRAS}$	68		ns	
TK15	CME/WE setup time to $\overline{CRAS}$	0		ns	
TK16	CME/WE hold time after $\overline{CRAS}$	34		ns	

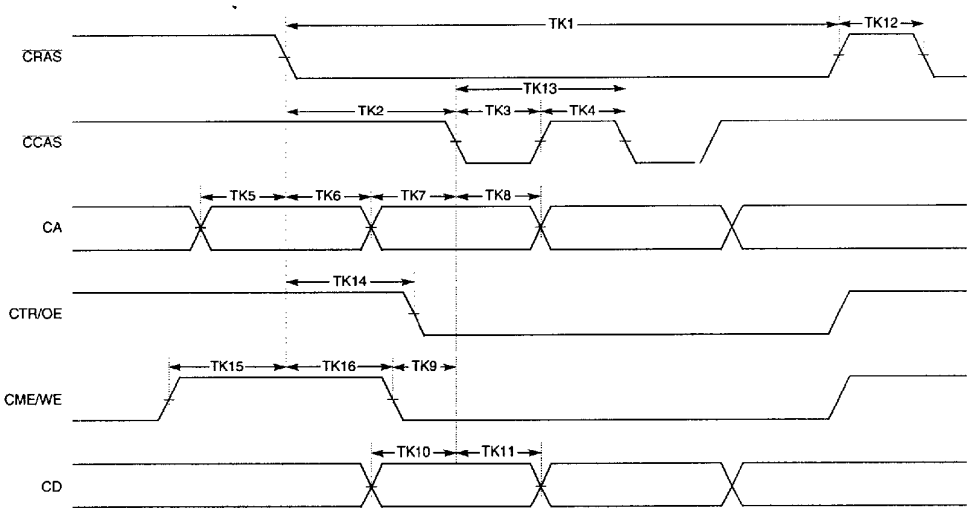


Figure 13. Code Buffer VRAM Write Cycle, Expansion (Fast Page Mode)

Code Buffer VRAM Transfer Cycle

Output Characteristics: VCLKX2 frequency = 29.5 MHz

Symbol	Parameter	Min	Max	Unit	
TL1	$\overline{CRAS}$ width	100		ns	
TL2	$\overline{CRAS}$ to $\overline{CCAS}$ delay	68		ns	
TL3	$\overline{CCAS}$ width	32		ns	
TL4	Row address setup	32		ns	
TL5	Row address hold	35		ns	
TL6	Column address setup	38		ns	
TL7	Column address hold	34		ns	
TL8	CTR/OE setup before $\overline{CRAS}$	33		ns	
TL9	CTR/OE hold after $\overline{CRAS}$	101		ns	
TL10	CME/WE setup before $\overline{CRAS}$	33		ns	
TL11	CME/WE hold after $\overline{CRAS}$	33		ns	
TL12	$\overline{CRAS}$ precharge time	102		ns	

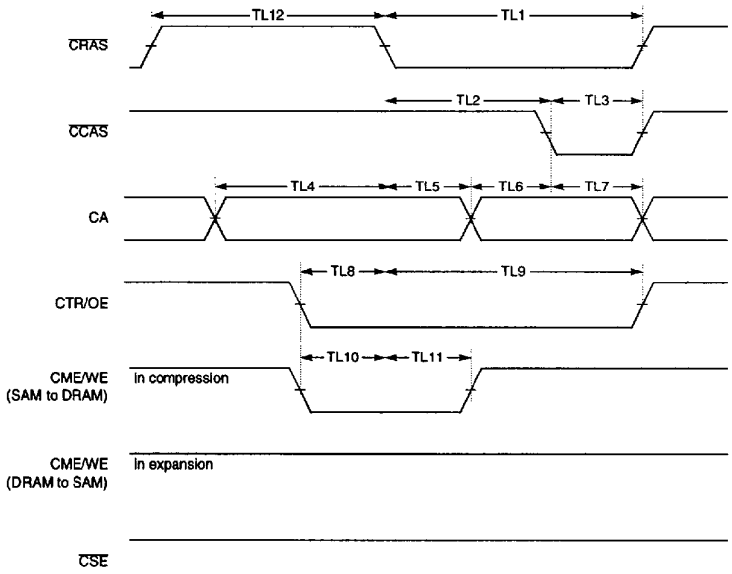


Figure 14. Code Buffer VRAM Transfer Cycle

Code Buffer VRAM Refresh Cycle

Output Characteristics: VCLKX2 frequency = 29.5 MHz

Symbol	Parameter	Min	Max	Unit	
TM1	$\overline{CRAS}$ to $\overline{CCAS}$ precharge time	34		ns	
TM2	$\overline{CCAS}$ precharge time	68		ns	
TM3	$\overline{CRAS}$ width	100		ns	
TM4	$\overline{CCAS}$ setup before $\overline{CRAS}$	33		ns	
TM5	$\overline{CCAS}$ hold after $\overline{CRAS}$	33		ns	

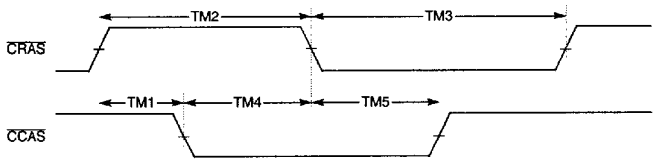


Figure 15. Code Buffer VRAM Refresh Cycle

Codec Interface, Control Signals Timing

Output Requirements

Symbol	Parameter	Min	Max	Unit	
TP1	DCLK Period, Compression	TA1		ns	FAST mode
		2*TA1		ns	SLOW mode

Codec Interface, Control Signals Timing, compression

Input Requirements

Symbol	Parameter	Min	Max	Unit	
TP2	Input Setup Time	12		ns	$\overline{STOP}$
		22		ns	$\overline{END}$, $\overline{CCS}$
TP3	Input Hold Time	1		ns	

Output Requirements

Symbol	Parameter	Min	Max	Unit	
TP4	Output Delay - FAST mode	2	15	ns	$\overline{EOS}$, $\overline{DSYNC}$
		5	11	ns	$\overline{CBUSY}$
TP4	Output Delay - SLOW mode	25	36	ns	$\overline{EOS}$, $\overline{DSYNC}$
		2	25	ns	$\overline{CBUSY}$

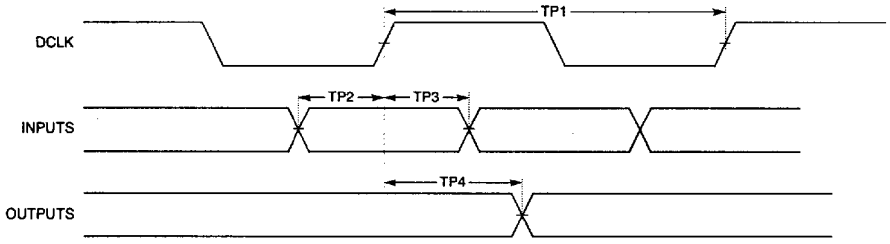


Figure 16. Codec Interface - Control Signal Timing, Compression

Codec Interface, Control Signals Timing, Expansion

Input Requirements

Symbol	Parameter	Min	Max	Unit	
TP5	Input Setup Time	12		ns	DSYNC, EOS
		22		ns	END, CCS
TP6	Input Hold Time	1		ns	

Output Requirements

Symbol	Parameter	Min	Max	Unit	
TP7	Output Delay - FAST mode	2	16	ns	STOP
		5	11	ns	CBUSY
TP7	Output Delay - SLOW mode	25	36	ns	STOP
		2	25	ns	CBUSY

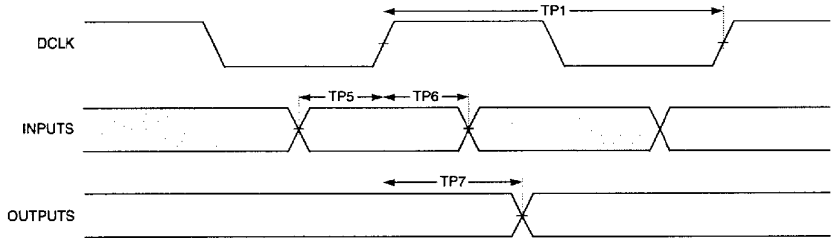


Figure 17. CODEC Interface - Control Signal Timing, Expansion

ZR36050 internal memory access control timing

Output Requirements

Symbol	Parameter	Min	Max	Unit	
TX1	CWR, CRD signal width	102		ns	
TX2	IACS activation delay	TA1 + 10		ns	
TX3	IACS deactivation delay	2 * TA1	3*TA1 + 10	ns	

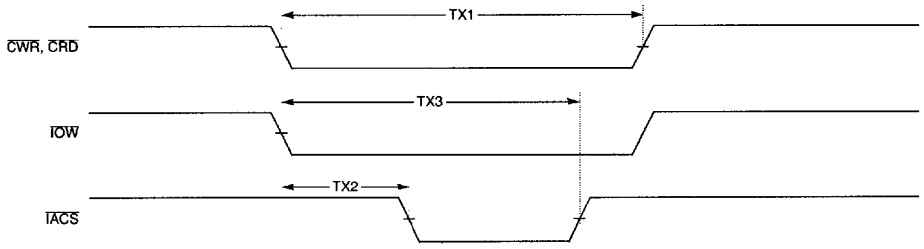


Figure 18. ZR36050 Internal Memory Access Control

Code Buffer VRAM Serial Output, Expansion

Input Requirements: VCLKX2 frequency = 29.5 MHz

Symbol	Parameter	Min	Max	Unit	
TQ4	Serial data hold after rising edge of CSC	0		ns	
TQ5	Access time from rising edge of CSC		25	ns	

Output Requirements

Symbol	Parameter	Min	Max	Unit	
TQ1	CSC Pulse Width	32		ns	
TQ2	CSC precharge time - FAST mode	32		ns	
	CSC precharge time - SLOW mode	100		ns	
TQ3	CSC cycle time - FAST mode	68		ns	
	CSC cycle time - SLOW mode	136		ns	

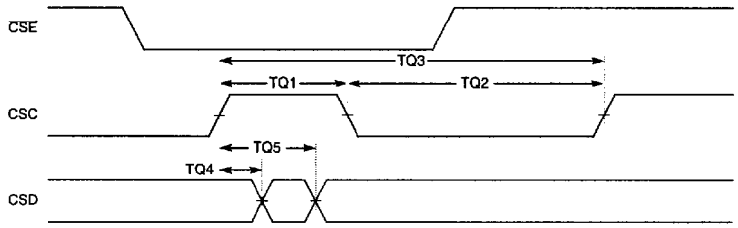


Figure 19. Code Buffer VRAM Serial Output, Expansion

Code Buffer VRAM Serial Input, Compression

Input Requirements: VCLKX2 frequency = 29.5 MHz

Symbol	Parameter	Min	Max	Unit	
TY1	CSC pulse width - FAST mode	16	18	ns	
	CSC pulse width - SLOW mode	32	36	ns	
TY2	CSC precharge time - FAST mode	16	18	ns	
	CSC precharge time - SLOW mode	32	36	ns	
TY3	Serial data setup time			ns	TBD
TY4	Serial data hold time			ns	TBD

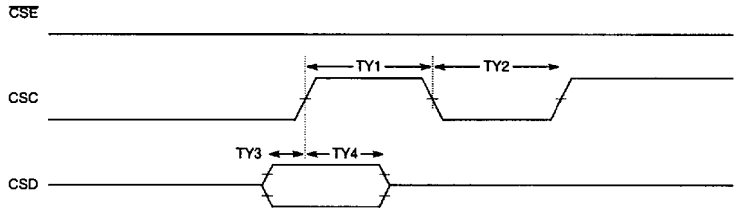


Figure 20. Code Buffer VRAM Serial Input, Compression

SRAM Interface, Control Signals Timing

Output Characteristics		Min	Max	Unit	
TN1	$\overline{SMR}$ active time	33		ns	
TN2	SMA setup to $\overline{SMR}$ rise	32		ns	
TN3	SMA delay after $\overline{SMR}$ rise	-0.8		ns	
TN6	$\overline{SMW}$ active time	16		ns	
TN7	SMD setup to $\overline{SMW}$ rise	11		ns	
TN8	SMD hold to $\overline{SMW}$ rise	1.5		ns	
TN9	SMA setup to $\overline{SMW}$ fall	17		ns	
TN10	SMA hold to $\overline{SMW}$ rise	0.6		ns	

Input Requirements		Min	Max	Unit	
TN4	SMD Setup to $\overline{SMR}$ rise	11		ns	
TN5	SMD Hold to $\overline{SMR}$ rise	0		ns	

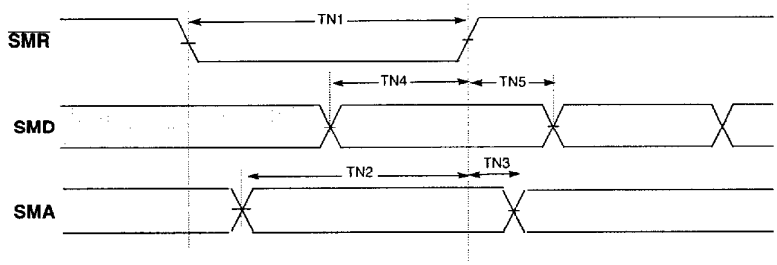


Figure 21. SRAM Interface - Read operation

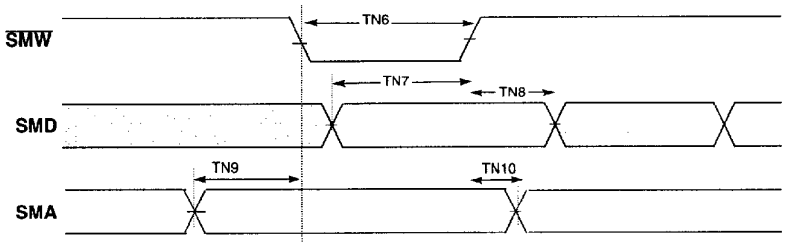


Figure 22. SRAM Interface - Write operation

Package Information

160-Pin Quad Flat Pack Pinout

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VSS	21	HA6	41	IOBASE0	61	VSS	81	VDD	101	HSYNC	121	VBUSEN	141	SMD11
2	HD15	22	HA7	42	IOBASE1	62	CMA0	82	CBUSY	102	FEOUT	122	SMW	142	SMD12
3	HD14	23	HA8	43	HDOE	63	CRAS	83	CCS	103	UV0	123	SMA13	143	SMD13
4	HD13	24	HA9	44	IACS	64	CMD4	84	CKEN	104	UV1	124	SMA8	144	SMD14
5	HD12	25	VDD	45	VDD	65	CMD5	85	DCLK	105	UV2	125	SMA9	145	SMD15
6	HD11	26	VSS	46	VSS	66	CMD6	86	C_RESET	106	UV3	126	SMA11	146	SMD10
7	HD10	27	REFRESH	47	CMA4	67	CMD7	87	PDATA0	107	UV4	127	SMR	147	SMD9
8	HD9	28	IOR	48	CMA5	68	CMD3	88	PDATA1	108	UV5	128	SMA10	148	SMD8
9	HD8	29	IOW	49	CMA6	69	CMD2	89	PDATA2	109	UV6	129	TEST	149	VDD
10	MEMW	30	AEN	50	CMA7	70	CMD1	90	PDATA3	110	UV7	130	EXTCS	150	VSS
11	MEMR	31	IORDY	51	CCAS	71	CMD0	91	PDATA4	111	Y0	131	SMD3	151	SMA0
12	IRQ	32	HD0	52	CME_WE	72	DSYNC	92	PDATA5	112	Y1	132	SMD4	152	SMA1
13	IOCS16	33	HD1	53	CMA8	73	EOS	93	PDATA6	113	Y2	133	SMD5	153	SMA2
14	H_ALE	34	HD2	54	CMA3	74	VSS	94	PDATA7	114	Y3	134	SMD6	154	SMA3
15	HA0	35	HD3	55	CMA2	75	VDD	95	VDD	115	Y4	135	SMD7	155	SMA4
16	HA1	36	HD4	56	CMA1	76	STOP	96	VCLKX2	116	Y5	136	SMD2	156	SMA5
17	HA2	37	HD5	57	CTR_OE	77	END	97	VSS	117	Y6	137	SMD1	157	SMA6
18	HA3	38	HD6	58	CSC	78	CRD	98	VCLK	118	Y7	138	SMD0	158	SMA7
19	HA4	39	HD7	59	CSE	79	CWR	99	VSYNC	119	VDD	139	VSS	159	SMA12
20	HA5	40	H_RESET	60	VDD	80	VSS	100	HREF	120	VSS	140	VDD	160	VDD

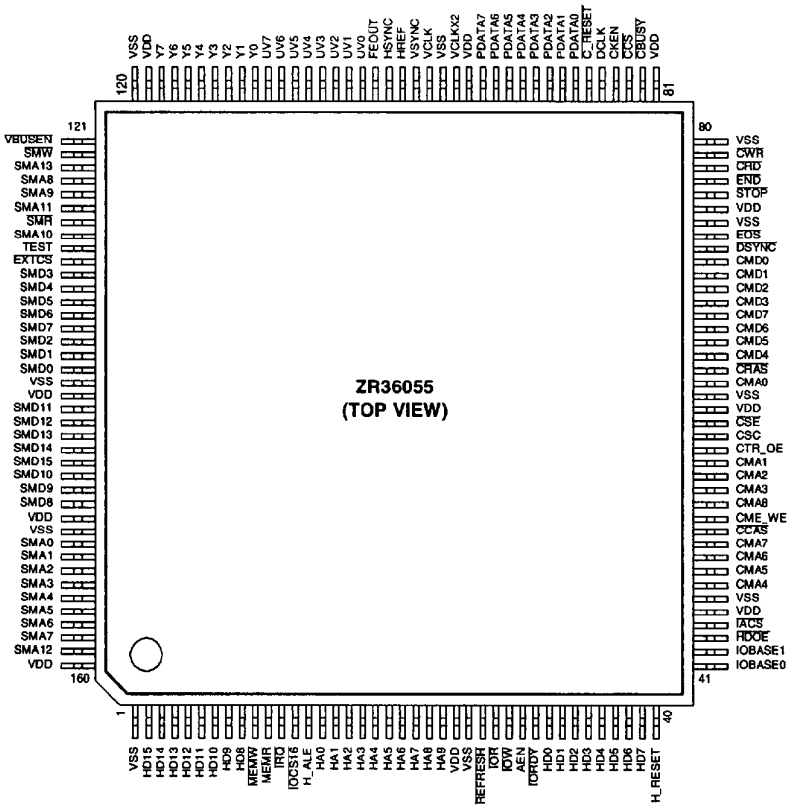
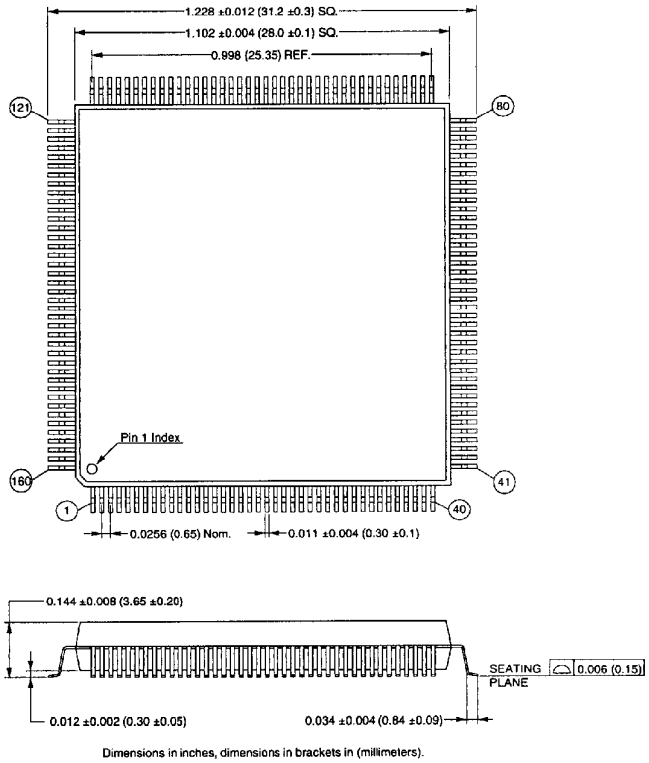


Figure 23. ZR36055 Plastic Quad Flat Pack Pinout

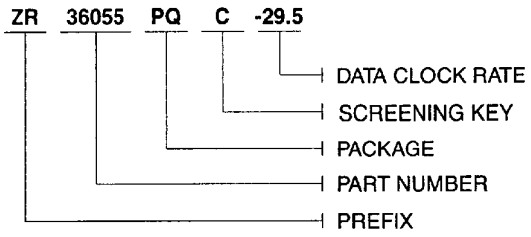
PACKAGE INFORMATION

Figure 24. ZR36055 Plastic Quad Flat Pack Dimensions



Dimensions in inches, dimensions in brackets in (millimeters).

ORDERING INFORMATION



PACKAGE
PQ - Plastic Quad Flat Pack (EIAJ)

DATA CLOCK RATE
-29.5: 29.5 MHz
-21: 21 MHz

SCREENING KEY
C - 0°C to +70°C (V_{CC} = 4.75V to 5.25V)

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